NNDD512512256256BBFF

NAND 512Mb*2 + Mobile SDRAM 256Mb*2

Document Title

Multi-Chip Package MEMORY
512M Bit(64Mx8) Nand Flash*2 / 256M Bit(8Mx8x4Banks) Mobile SDRAM*2

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue. - 1Gb NAND Flash DDP B-Die _ Ver 0.1 - 512Mb Mobile SDRAM DDP F-Die _ Ver 1.0	November 26, 2004	Preliminary
0.1	<Mobile SDRAM> .... Ver 1.1 - Corrected Errata in Capacitance value	July 15, 2005	Revision

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

Multi-Chip Package MEMORY

512M Bit(64Mx8) Nand Flash*2 / 256M Bit(8Mx8x4Banks) Mobile SDRAM*2

FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 107ball FBGA Type - 10.5mmx13mm, 0.8mm pitch

<NAND>
- Power Supply Voltage : 1.7~ 1.95V
- Organization
  - Memory Cell Array : (128M + 4096K)bit x 8 bit
  - Data Register : (512 + 16)bit x 8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- Page Read Operation
  - Page Size : (512 + 16)Byte
  - Random Access : 15µs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back
- Unique ID for Copyright Protection

<Mobile SDRAM>
- Power Supply Voltage : 1.7~1.95V
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - -. CAS latency (1, 2 & 3).
  - -. Burst length (1, 2, 4, 8 & Full page).
  - -. Burst type (Sequential & Interleave).
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- Special Function Support.
  - -. PASR (Partial Array Self Refresh).
  - -. Internal TCSR (Temperature Compensated Self Refresh)
  - -. DS (Driver Strength)
- DQM for masking.
- Auto refresh.
- 64ms refresh period (8K cycle).
- 1/CS Support.

Address configuration

Organization	Bank	Row	Column Address
32M x 16	BA0, BA1	A0 - A12	A0 - A9

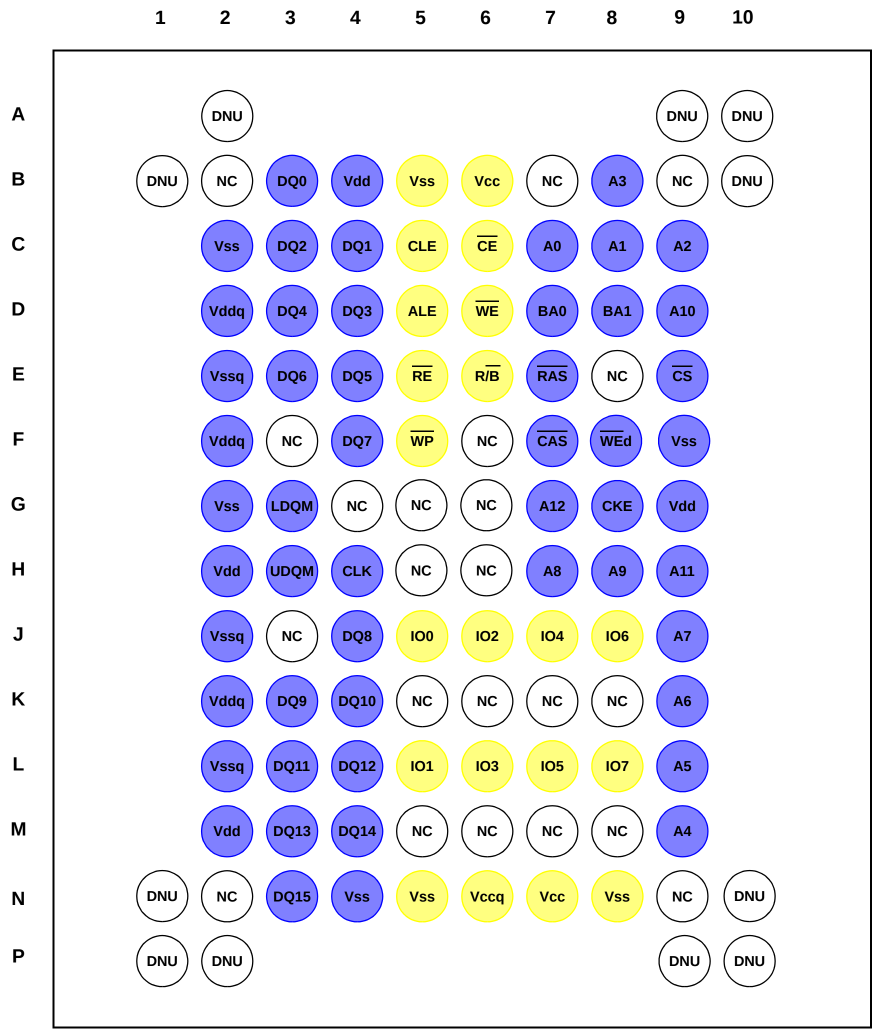
GENERAL DESCRIPTION

The KBE00G003M is a Multi-Chip Package Memory which combines 1Gbit Nand Flash Memory(organized with two pieces of 512Mbit Nand Flash Memory) and 512Mbit synchronous high data rate Dynamic RAM. (organized with two pieces of 256Mbit Mobile SDRAM) 1Gbit NAND Flash memory is organized as 128M x8 bits and 512Mbit Mobile SDRAM is organized as 8M x16 bits x4 banks In 1Gbit NAND Flash, its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typically 200µs on the 528-byte page and an erase operation can be performed in typically 2ms on a 16K-byte block. Data in the data register can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. This device is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

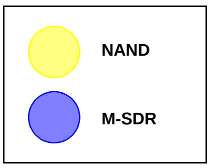
In 512Mbit SDRAM, Synchronous design make a device controlled precisely with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

The KBE00G003A is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 107-ball FBGA Type.

PIN CONFIGURATION



107 FBGA: Top View (Ball Down)



PIN DESCRIPTION

Pin Name	Pin Function(Mobile SDRAM)
CLK	System Clock
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$d	Write Enable
A0 ~ A12	Address Input
BA0 ~ BA1	Bank Address Input
LDQM	Lower Input/Output Data Mask
UDQM	Upper Input/Output Data Mask
DQ0 ~ DQ15	Data Input/Output
Vdd	Power Supply
Vddq	Data Out Power
Vss	Ground
Vssq	DQ Ground

Pin Name	Pin Function(NAND Flash)
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WP}$	Write Protection
$\overline{WE}$	Write Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
R/$\overline{B}$	Ready/Busy Output
IO0 ~ IO7	Data Input/Output
Vcc	Power Supply
Vccq	Data Out Power
Vss	Ground

Pin Name	Pin Function
NC	No Connection
DNU	Do Not Use

ORDERING INFORMATION

KB E 00 G 0 0 3 M - D 411

Samsung
MCP Memory(4chips)

Device Type
NAND + NAND + SDRAM+SDRAM

NOR Flash Density, Voltage, Organization, Bank Size, Boot Block
00 = None

NAND Flash Density, Voltage, Organization
F = 512M+512M, 1.8V/1.8V, x8

UtRAM Density, Voltage, Organization
0 = None

SRAM Density, Voltage, Organization
0 = None

Access Time
411 : NAND Flash 50ns
NAND Flash 50ns
Mobile SDRAM 9ns
Mobile SDRAM 9ns

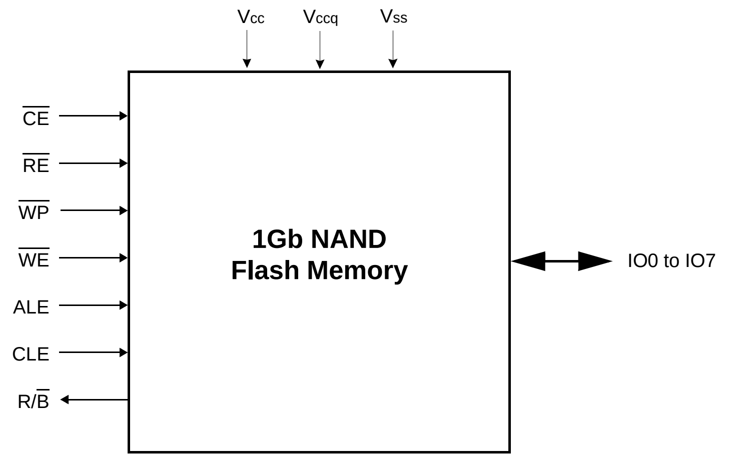
Package
D = FBGA(Lead-Free)

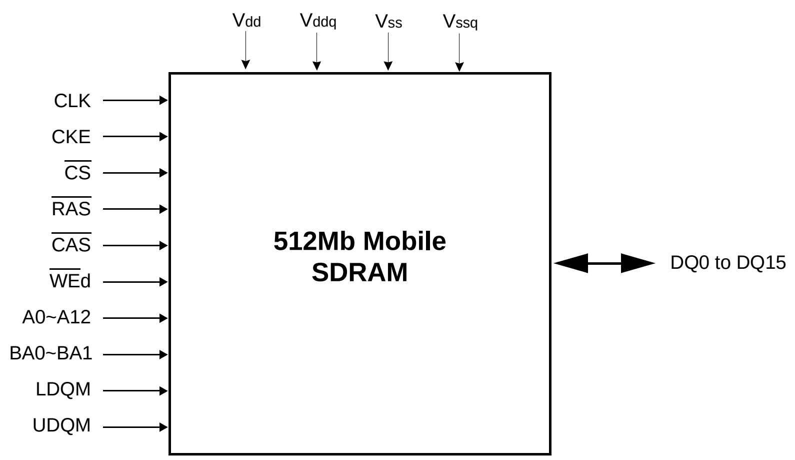
Version
M = 1st Generation

SDRAM Interface, Density, Voltage, Organization, Option
3 = M-SDR, 256M+256M, 1.8V/1.8V, x16

NOTE :
1. Samsung are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in samsung electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

FUNCTIONAL BLOCK DIAGRAM





1Gb(128Mb x 8)
NAND Flash DDP B-Die

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.
CE	**CHIP ENABLE** The CE input is the device selection control. When the device is in the Busy state, CE high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE control during read operation, refer to 'Page read' section of Device operation .
RE	**READ ENABLE** The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one.
WE	**WRITE ENABLE** The WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse.
WP	**WRITE PROTECT** The WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP pin is active low.
R/B	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VccQ	**OUTPUT BUFFER POWER** VccQ is the power supply for Output Buffer. VccQ is internally connected to Vcc, thus should be biased to Vcc.
Vcc	**POWER** Vcc is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.
DNU	**DO NOT USE** Leave it disconnected.

NOTE : Connect all Vcc and Vss pins of each device to common power supply outputs.
Do not leave Vcc or Vss disconnected.

Figure 1. Functional Block Diagram

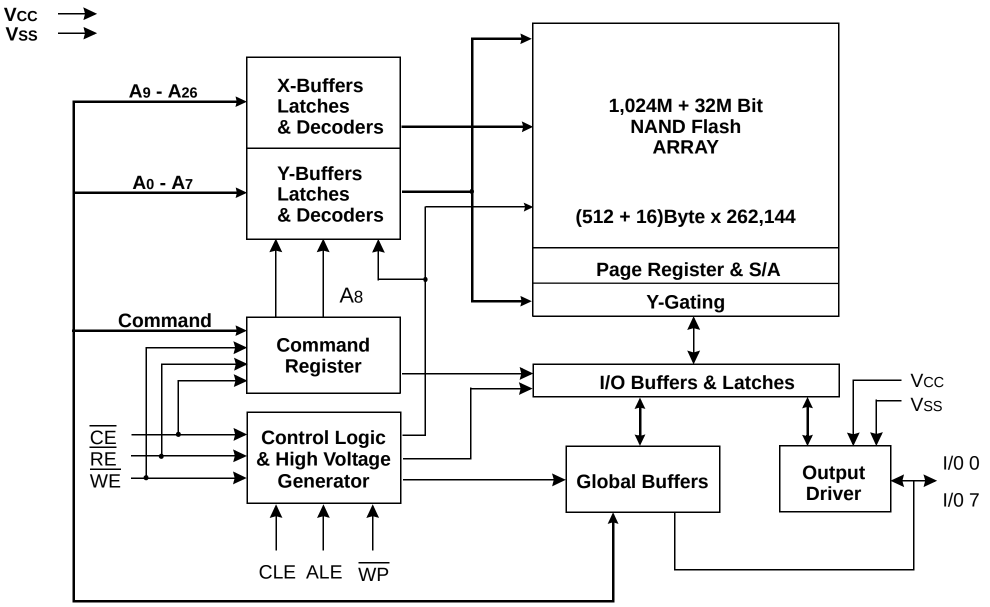
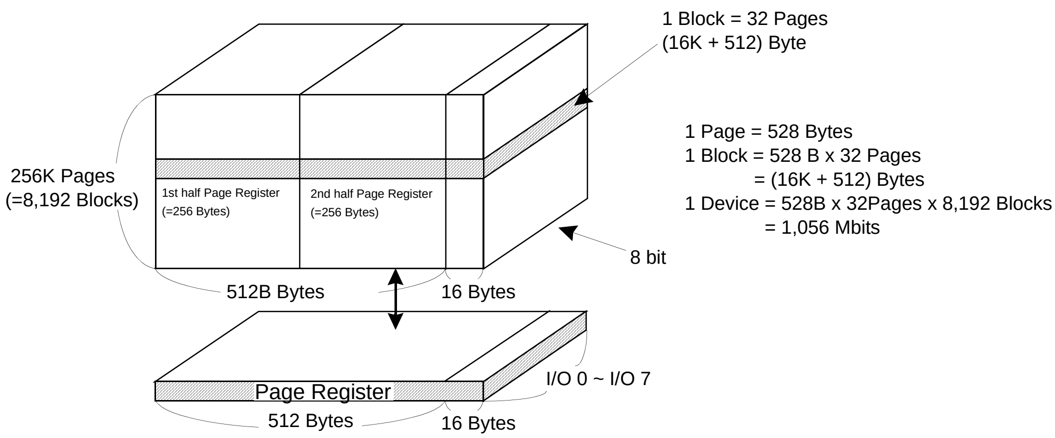


Figure 2. Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address (Page Address)**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	
4th Cycle	A_{25}	A_{26}	*L	*L	*L	*L	*L	*L	

NOTE : Column Address : Starting Address of the Register.
00h Command(Read) : Defines the starting address of the 1st half of the register.
01h Command(Read) : Defines the starting address of the 2nd half of the register.
* A_8 is set to "Low" or "High" by the 00h or 01h Command.
* L must be set to "Low".

Product Introduction

This device is a 1,026Mbit(1,107,296,436 bit) memory organized as 262,144 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 16 cells. Total 135168 NAND cells reside in a block. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 8,192 separately erasable 16K-byte blocks. It indicates that the bit by bit erase operation is prohibited on this device.

This device has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Data is latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. The 128M byte physical space requires 27 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of this device.

The device provides simultaneous program/erase capability up to four pages/blocks. By dividing the memory array into eight 128Mbit separate planes, simultaneous multi-plane operation dramatically increases program/erase performance by 4X while still maintaining the conventional 512 byte structure.
The extended pass/fail status for multi-plane program/erase allows system software to quickly identify the failing page/block out of selected multiple pages/blocks. Usage of multi-plane operations will be described further throughout this document.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another of the same plane without the need for transporting the data to and from the external buffer memory. Since the time-consuming burst-reading and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle	3rd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	-	
Read 2	50h	-	-	
Read ID	90h	-	-	
Reset	FFh	-	-	O
Page Program (True)(2)	80h	10h	-	
Page Program (Dummy)(2)	80h	11h	-	
Copy-Back Program(True)(2)	00h	8Ah	10h	
Copy-Back Program(Dummy)(2)	03h	8Ah	11h	
Block Erase	60h	D0h	-	
Multi-Plane Block Erase	60h---60h	D0h	-	
Read Status	70h	-	-	O
Read Multi-Plane Status	71h(3)	-	-	O

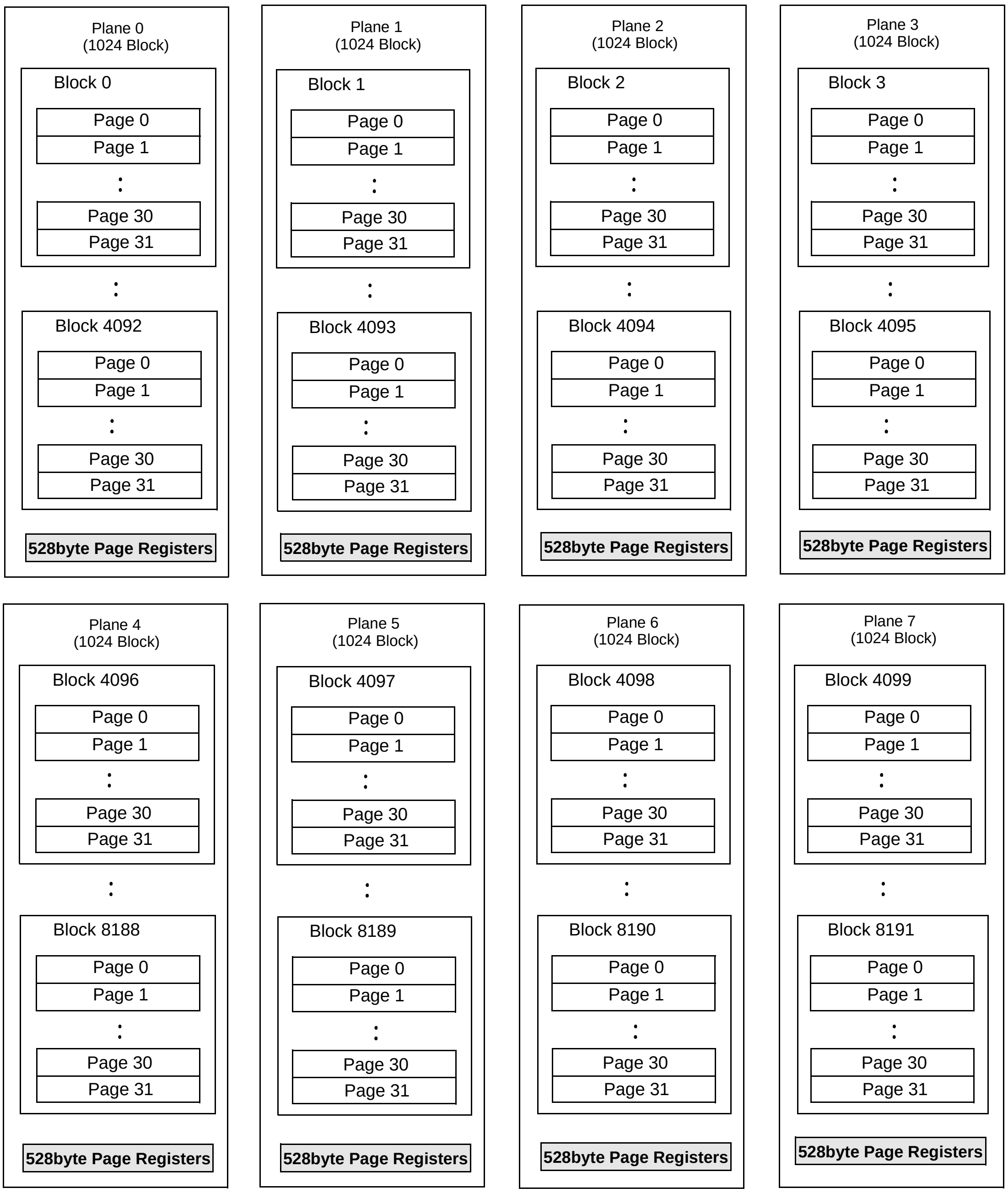
NOTE : 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.
2. Page Program(True) and Copy-Back Program(True) are available on 1 plane operation.
Page Program(Dummy) and Copy-Back Program(Dummy) are available on the 2nd,3rd,4th plane of multi plane operation.
3. The 71h command should be used for read status of Multi Plane operation.
4. Multi plane operation and Copy-Back Program are not supported with 1.8V device.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

Memory Map

The device is arranged in eight 128Mbit memory planes. Each plane contains 1,024 blocks and 528 byte page registers. This allows it to perform simultaneous page program and block erase by selecting one page or block from each plane. The block address map is configured so that multi-plane program/erase operations can be executed for every four sequential blocks by dividing the memory array into plane 0~3 or plane 4~7 separately. For example, multi-plane program/erase operations into plane 2,3,4 and 5 are prohibited.

Figure 3. Memory Array Map



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN/OUT}$	-0.6 to + 4.6	V
	V_{CC}	-0.6 to + 4.6	
	V_{CCQ}	-0.6 to + 4.6	
Temperature Under Bias	T_{BIAS}	-40 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Short Circuit Current	Ios	5	mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC},+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND,T_A=-25 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	1.70	1.8	1.95	V
Supply Voltage	V_{CCQ}	1.70	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Current	Sequential Read	$I_{CC}1$	tRC=50ns, $\overline{CE}$=V_{IL} I_{OUT}=0mA		-	8	20	mA
	Program	$I_{CC}2$	-		-	8	20	
	Erase	$I_{CC}3$	-		-	8	20	
Stand-by Current(TTL)		$I_{SB}1$	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}		-	-	1	
Stand-by Current(CMOS)		$I_{SB}2$	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}		-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)		-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)		-	-	±10	
Input High Voltage		V_{IH}*	I/O pins		V_{CCQ} -0.4	-	V_{CCQ} +0.3	V
			Except I/O pins		V_{CC} -0.4	-	V_{CC} +0.3	
Input Low Voltage, All inputs		V_{IL}*	-		-0.3	-	0.4	
Output High Voltage Level		V_{OH}	I_{OH}=-100µA		V_{CCQ} -0.1	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=100uA		-	-	0.1	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.1V		3	4	-	mA

NOTE : VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	4,026	-	4,096	Blocks

NOTE :
1. The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.
3. Minimum 1004 valid blocks are guaranteed for each contiguous 128Mb memory space.

AC TEST CONDITION

(TA=-25 to 85°C, Vcc=1.65V~1.95V unless otherwise noted)

Parameter	Value
Input Pulse Levels	0V to V_{CCQ}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	$V_{CCQ}/2$
Output Load (V_{CCQ}:1.8V +/-10%)	1 TTL GATE and CL=30pF

CAPACITANCE(T_A=25°C, V_{CC}=1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑ (rising edge)	H	X	Read Mode	Command Input
L	H	L	↑ (rising edge)	H	X		Address Input(4clock)
H	L	L	↑ (rising edge)	H	H	Write Mode	Command Input
L	H	L	↑ (rising edge)	H	H		Address Input(4clock)
L	L	L	↑ (rising edge)	H	H	Data Input	
L	L	L	H	↓ (falling edge)	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

PROGRAM / ERASE CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}(1)	-	200	500	µs
Dummy Busy Time for Multi Plane Program		t_{DBSY}		1	10	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	1	cycle
	Spare Array		-	-	2	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

NOTE : 1.Typical program time is defined as the time within more than 50% of the whole pages are programmed at Vcc of 3.3V and 25'C

AC TIMING CHARACTERISTICS FOR COMMAND / ADDRESS / DATA INPUT

Parameter	Symbol	Min			Max			Unit
CLE setup Time	t_{CLS}	0	0	0	-	-	-	ns
CLE Hold Time	t_{CLH}	10	10	10	-	-	-	ns
$\overline{CE}$ setup Time	t_{CS}	0	0	0	-	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	10	10	-	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	25(1)	25(1)	-	-	-	ns
ALE setup Time	t_{ALS}	0	0	0	-	-	-	ns
ALE Hold Time	t_{ALH}	10	10	10	-	-	-	ns
Data setup Time	t_{DS}	20	20	20	-	-	-	ns
Data Hold Time	t_{DH}	10	10	10	-	-	-	ns
Write Cycle Time	t_{WC}	45	45	45	-	-	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	15	15	-	-	-	ns

NOTE: 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC CHARACTERISTICS FOR OPERATION

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	15	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
RE Pulse Width	t_{RP}	25	-	ns
WE High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	35	ns
$\overline{CE}$ Access Time	t_{CEA}	-	45	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device resetting time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is so called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 517. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 4). Any intentional erasure of the initial invalid block information is prohibited.

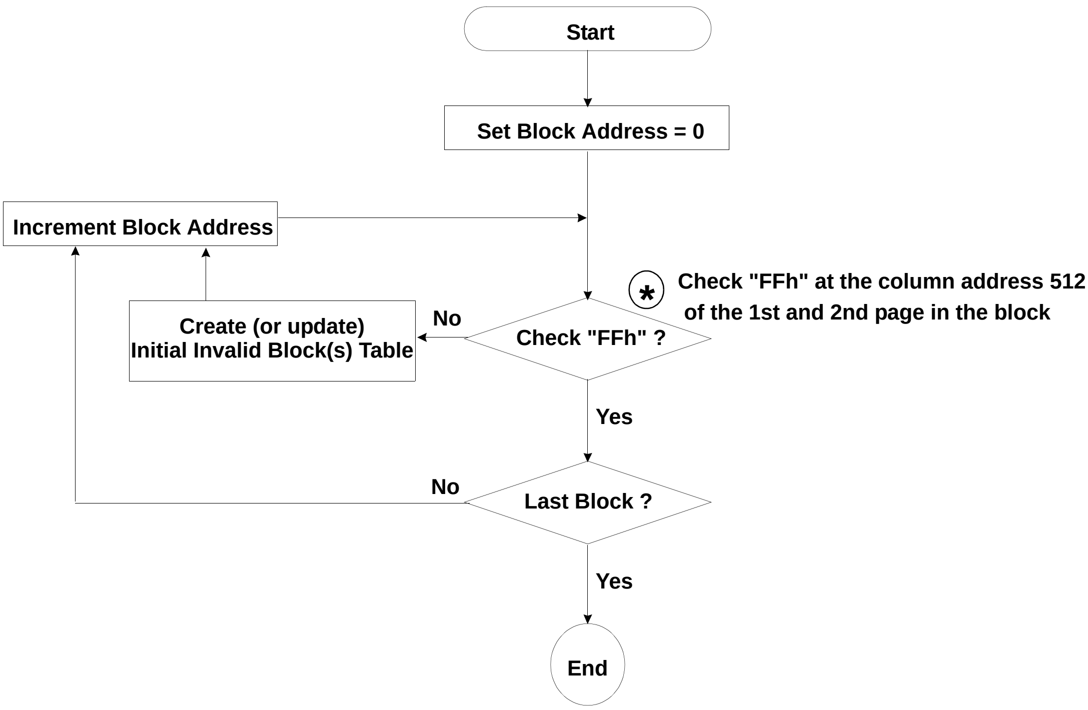


Figure 4. Flow chart to create initial invalid block table.

NAND Flash Technical Notes *(Continued)*

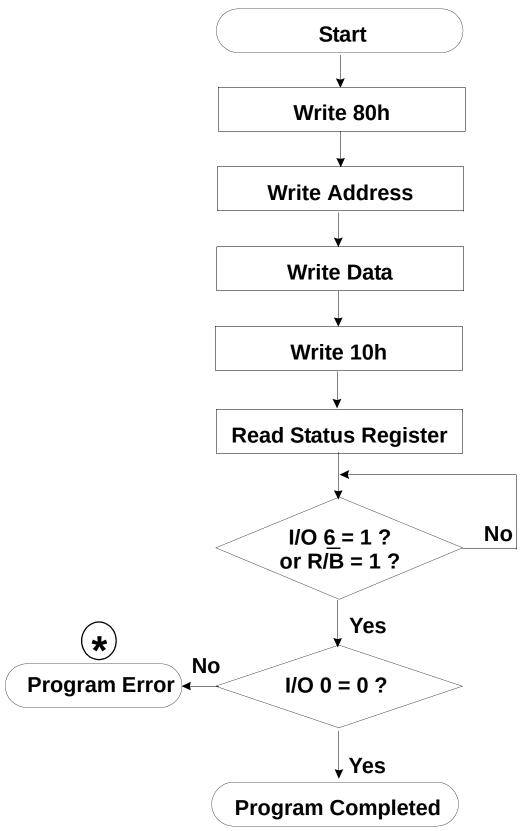
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure ratein the qualification report does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

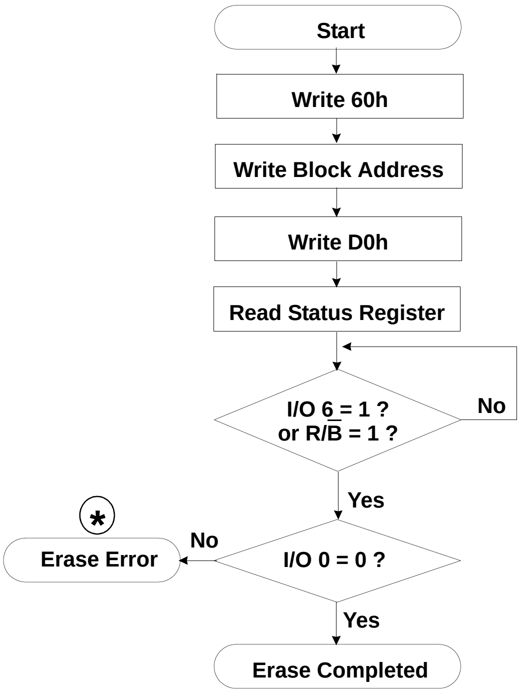
Program Flow Chart



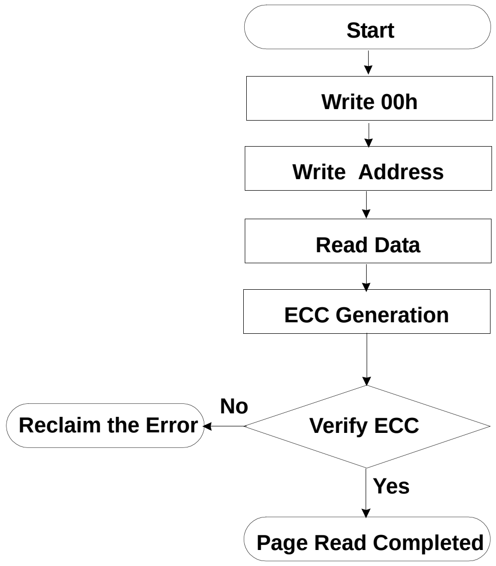
*** : If program operation results in an error, map out the block including the page in error and copy the target data to another block.**

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

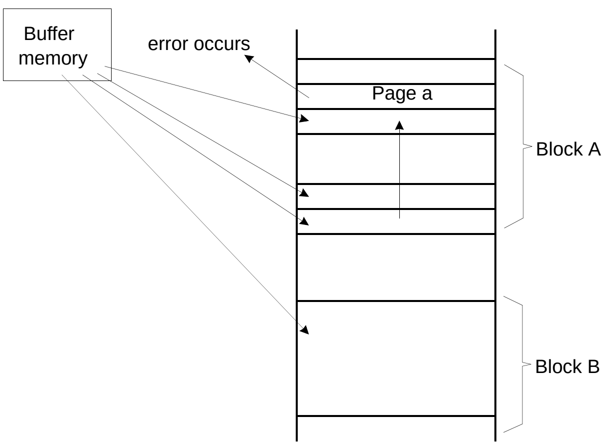


Read Flow Chart



*** : If erase operation results in an error, map out the failing block and replace it with another block.**

Block Replacement



When the error happens with page "a" of Block "A", try to write the data into another Block "B" from an external buffer. Then, prevent further system access to Block "A" (by creating a "invalid block" table or other appropriate scheme.)

Pointer Operation

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

Table 2. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

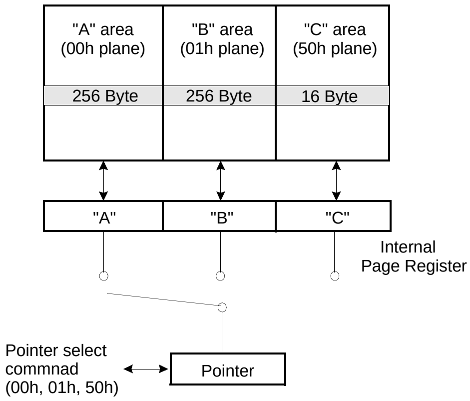
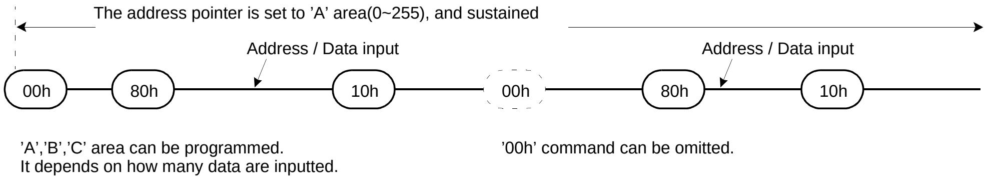
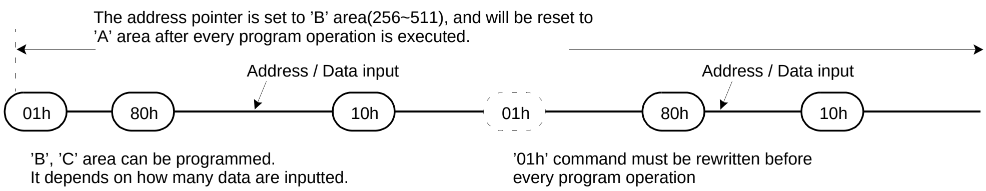


Figure 5. Block Diagram of Pointer Operation

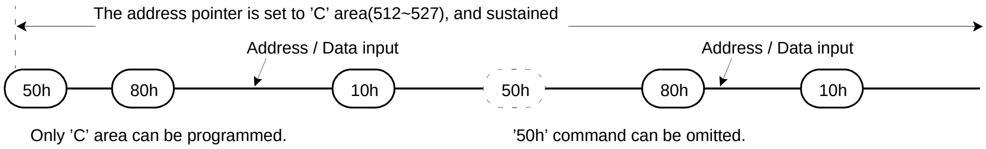
(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



(3) Command input sequence for programming 'C' area



System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 6. Program Operation with $\overline{CE}$ don't-care.

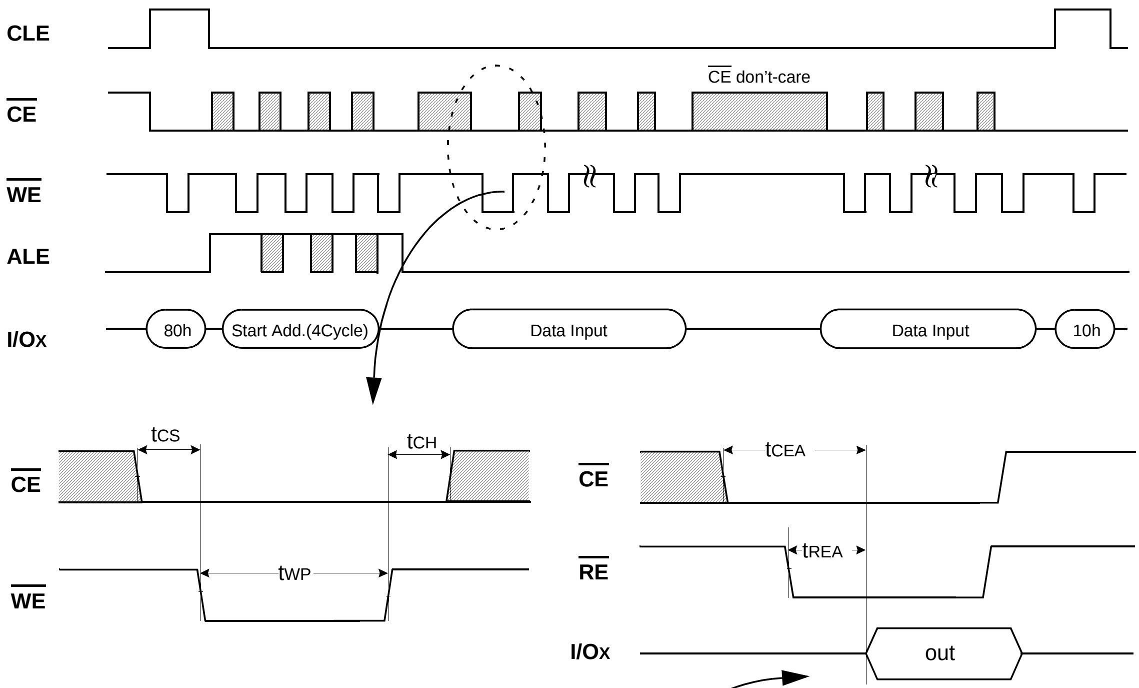
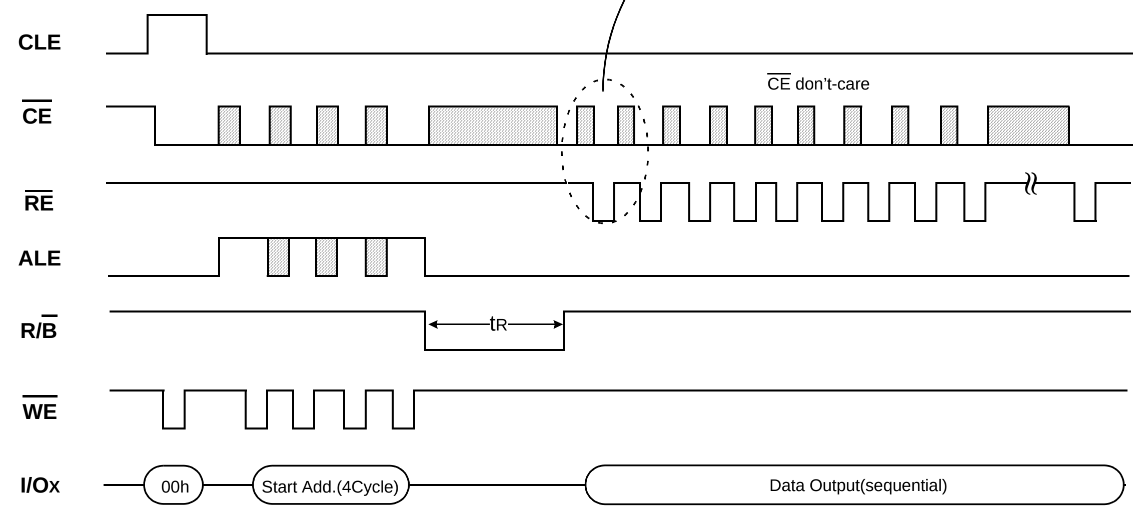
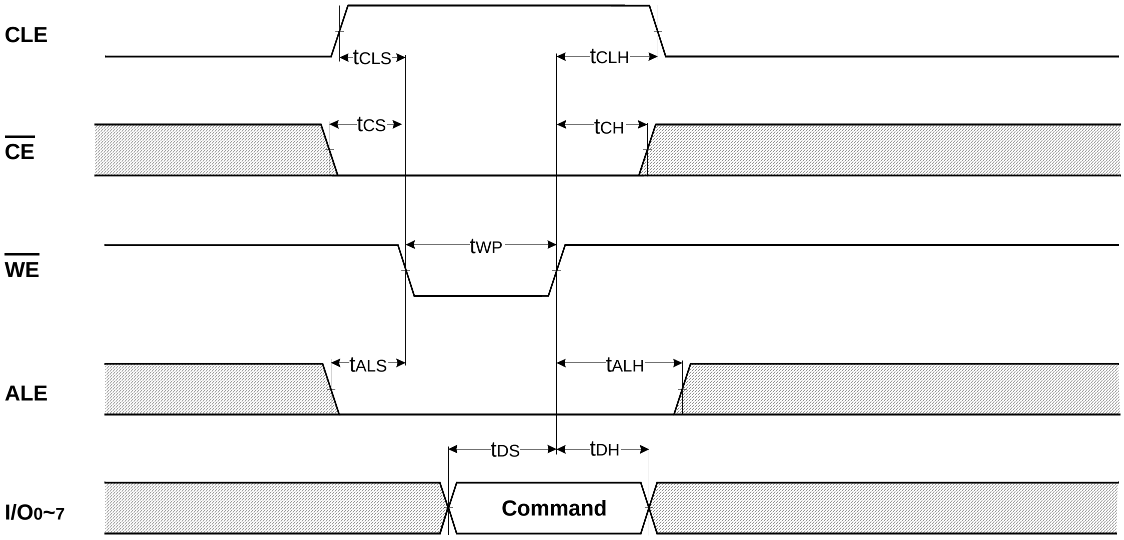


Figure 7. Read Operation with $\overline{CE}$ don't-care.

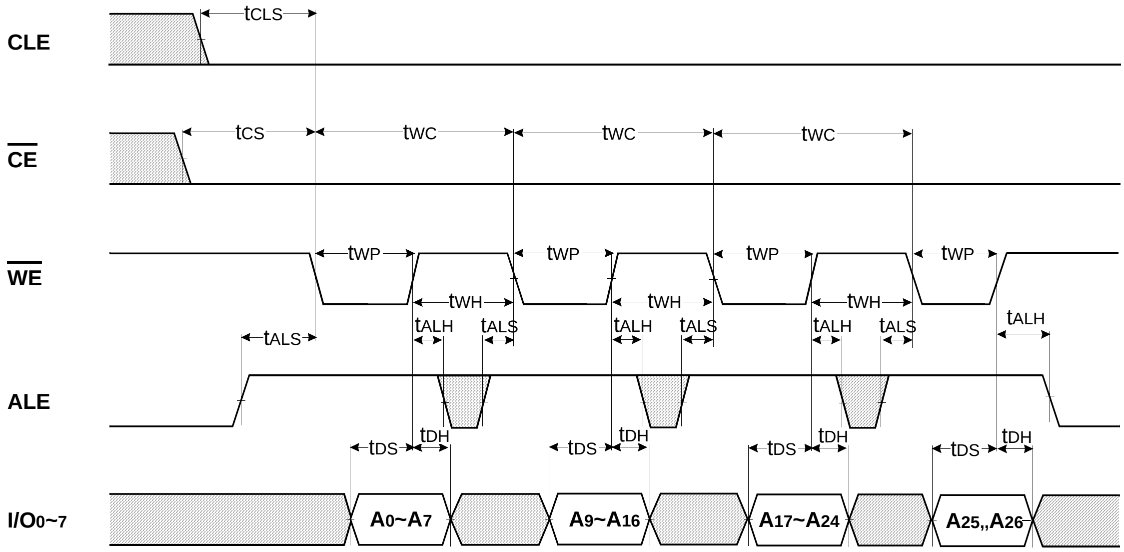


I/O	DATA
I/Ox	**Data In/Out**
I/O 0 ~ I/O 7	~528byte

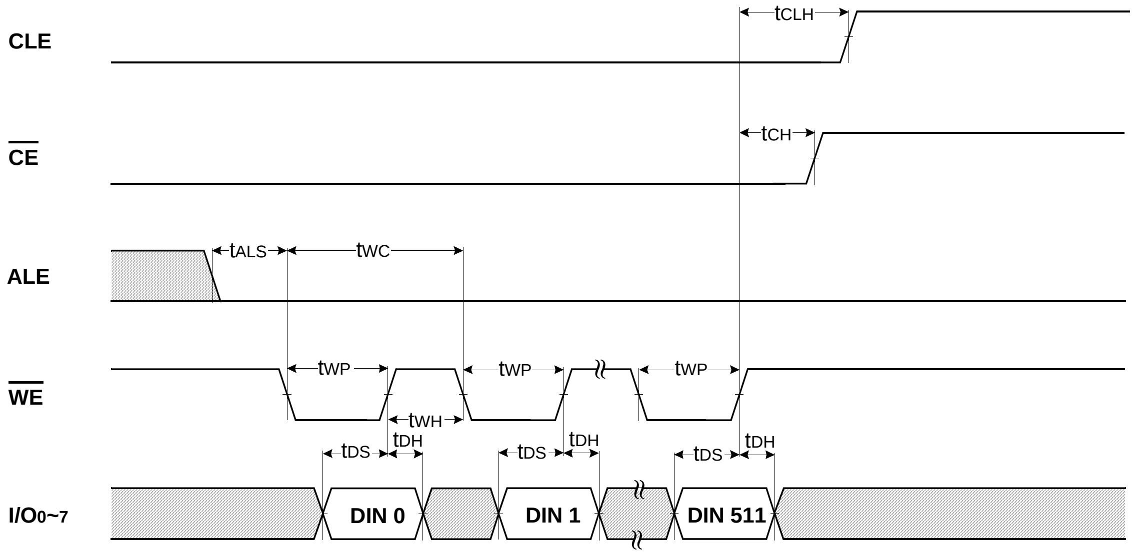
Command Latch Cycle



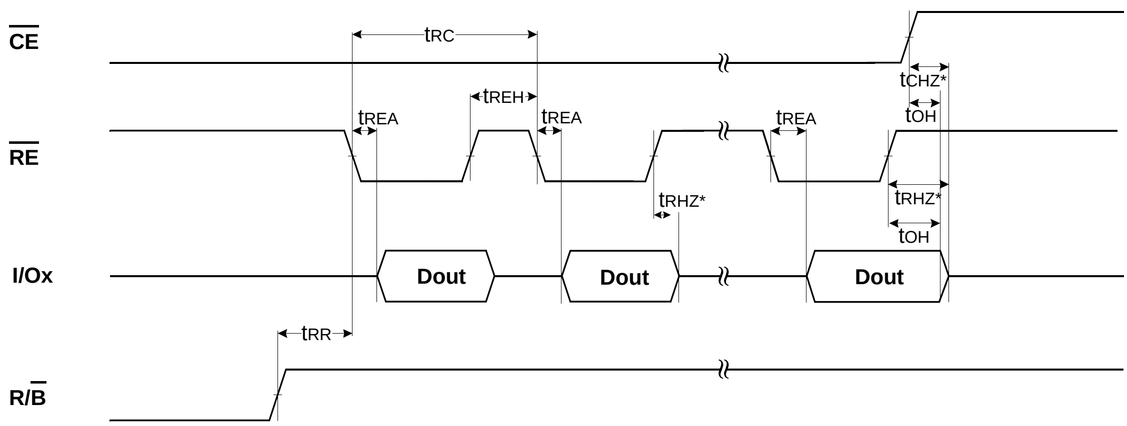
Address Latch Cycle



Input Data Latch Cycle

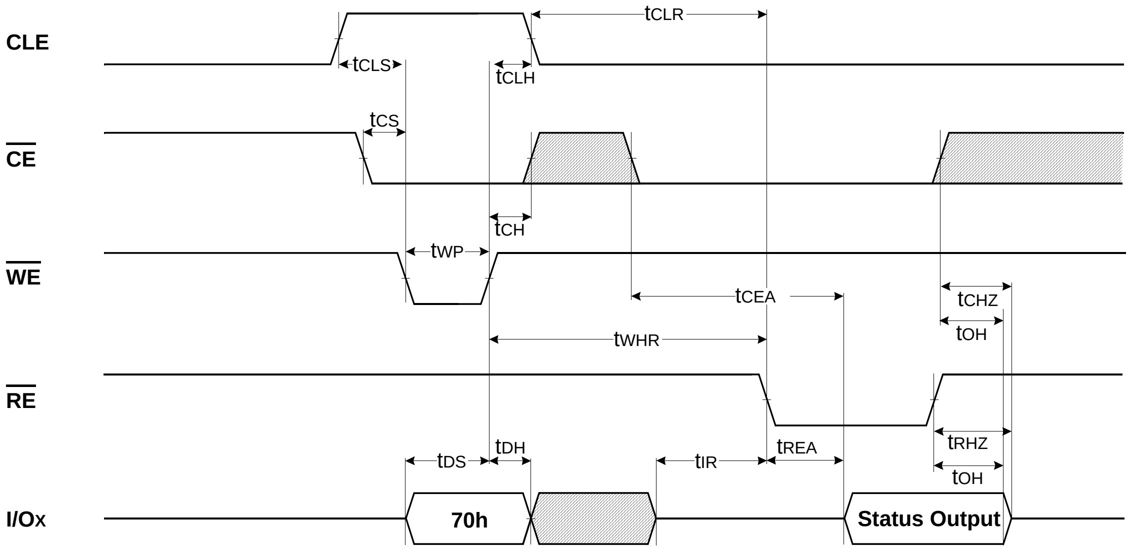


Serial access Cycle after Read(CLE=L, WE=H, ALE=L)

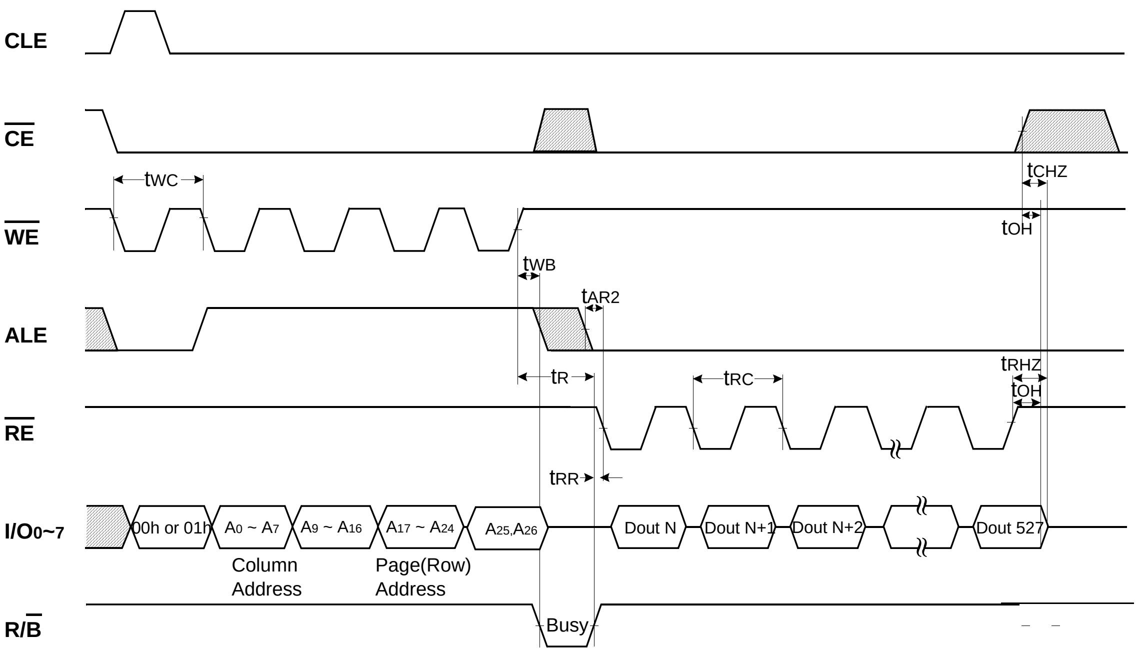


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

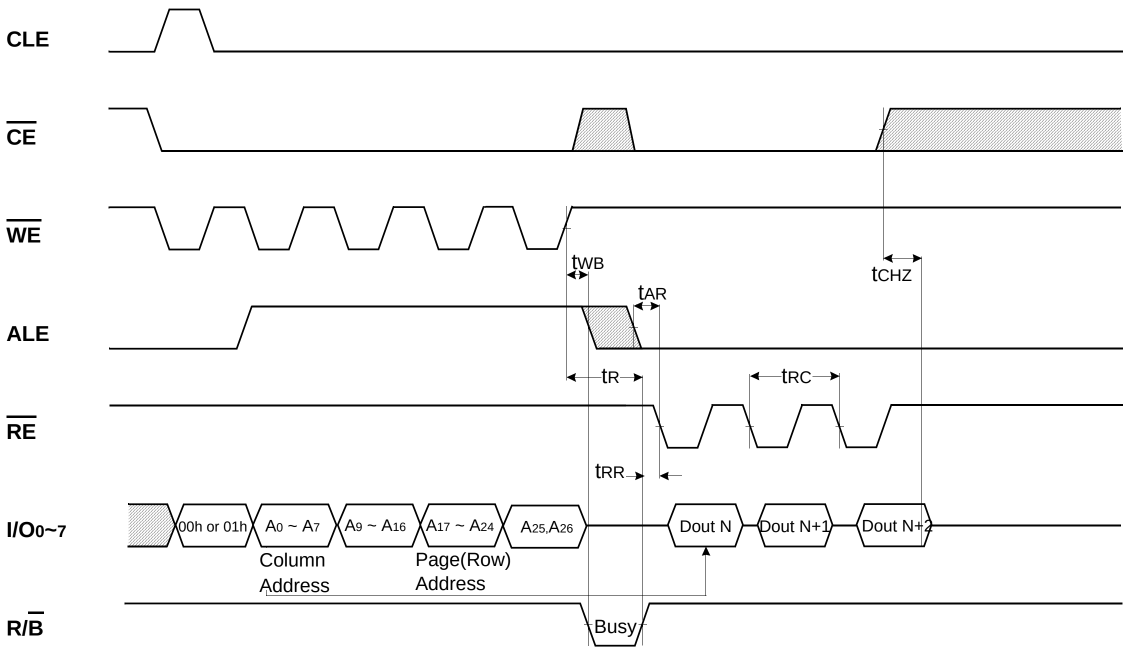
Status Read Cycle



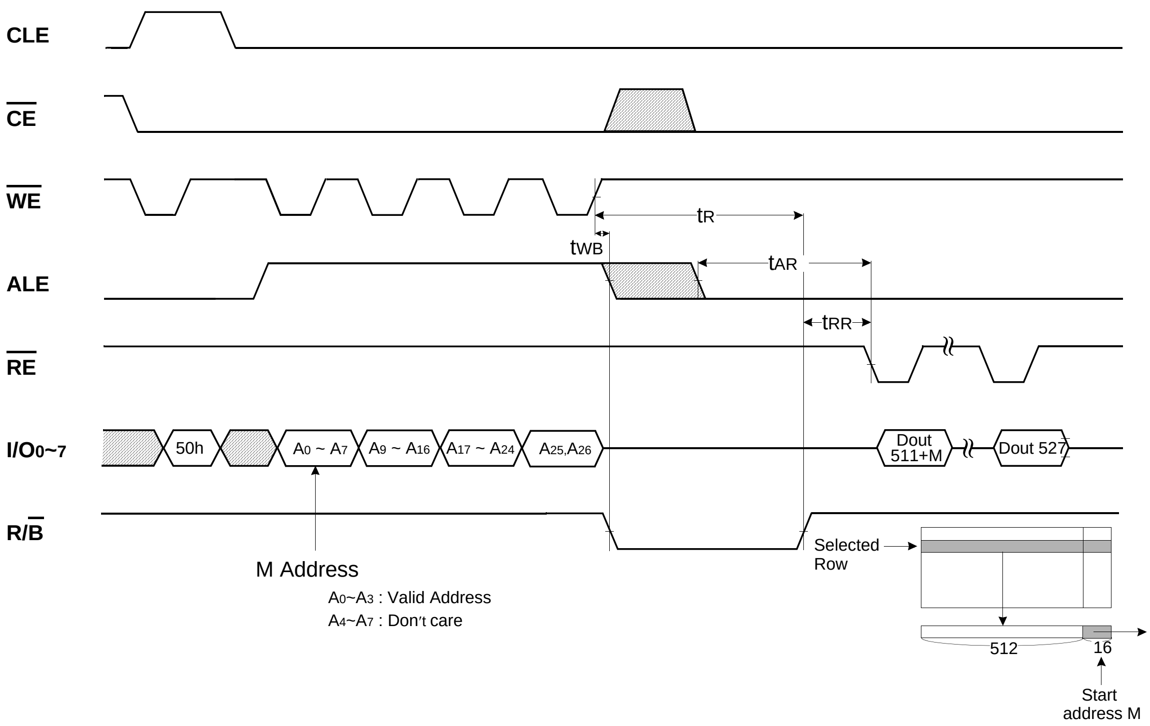
Read1 Operation(Read One Page)



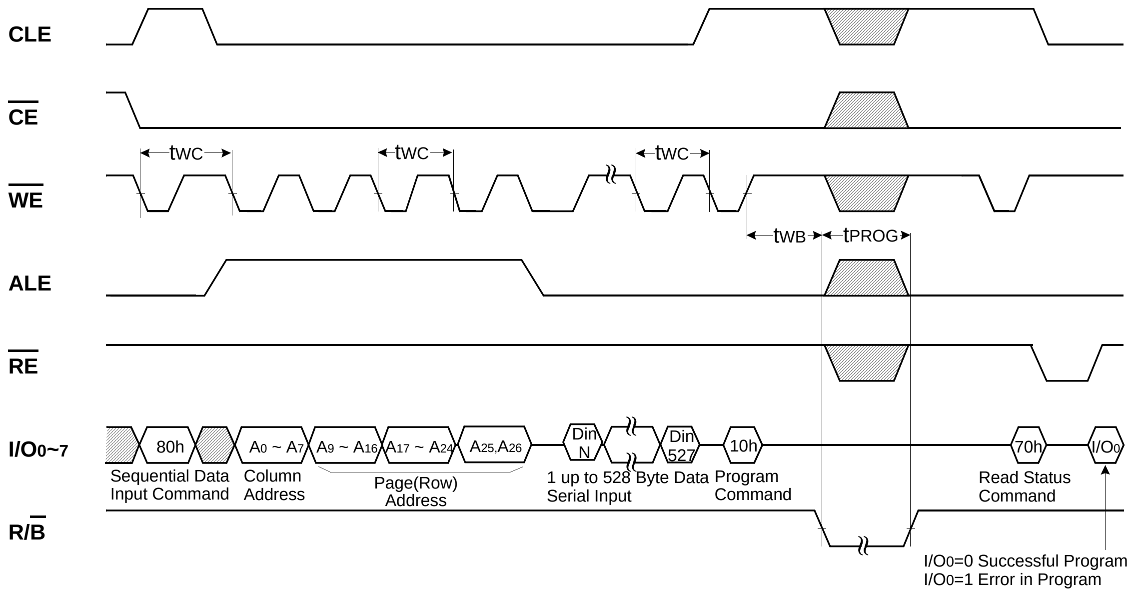
Read1 Operation(Intercepted by $\overline{CE}$)



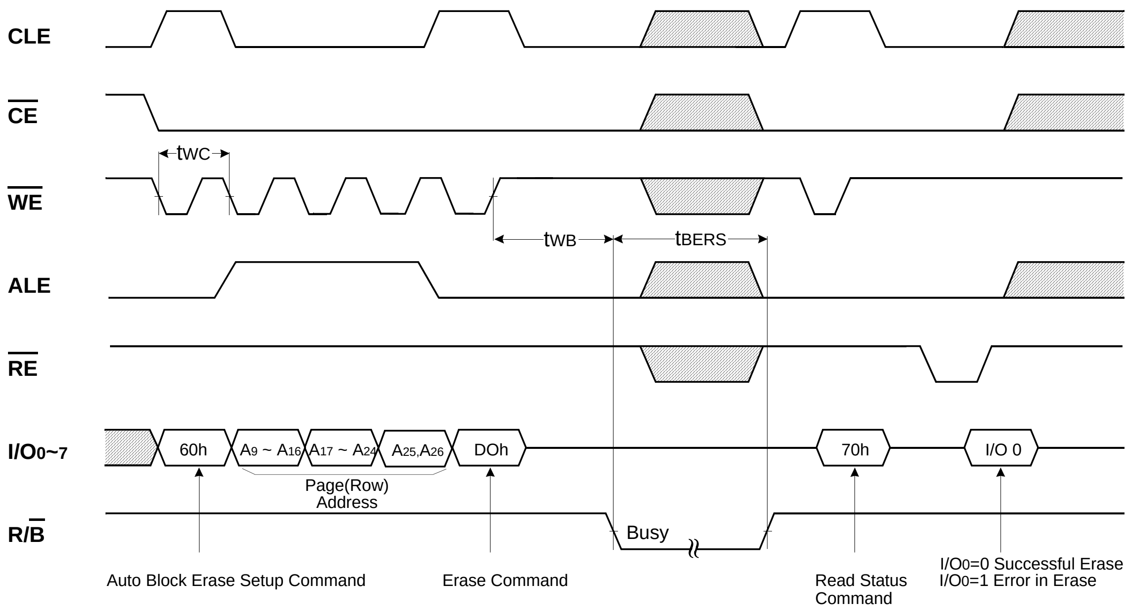
Read2 Operation(Read One Page)



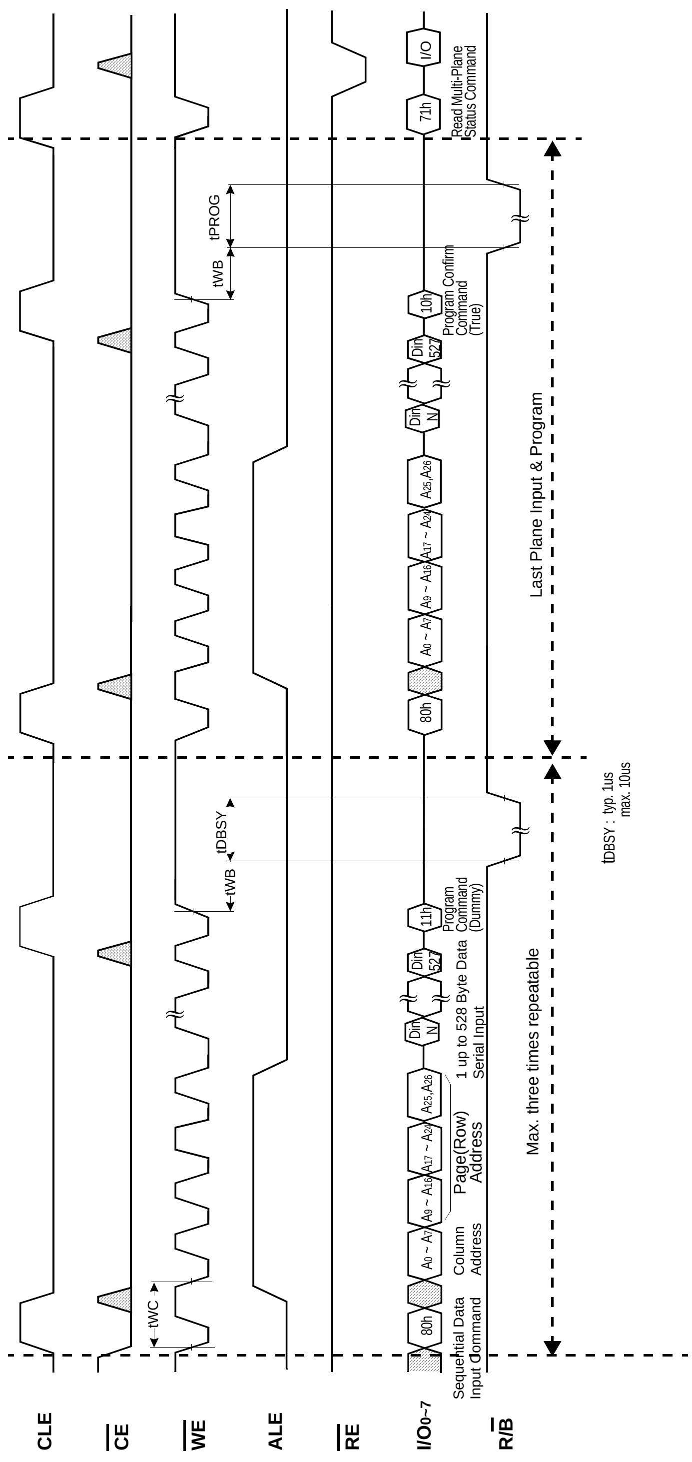
Page Program Operation



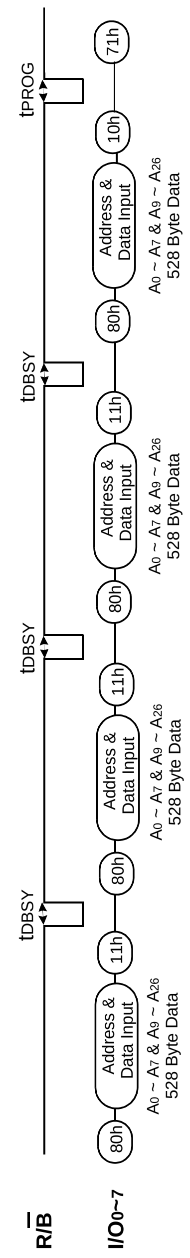
BLOCK ERASE OPERATION (ERASE ONE BLOCK)



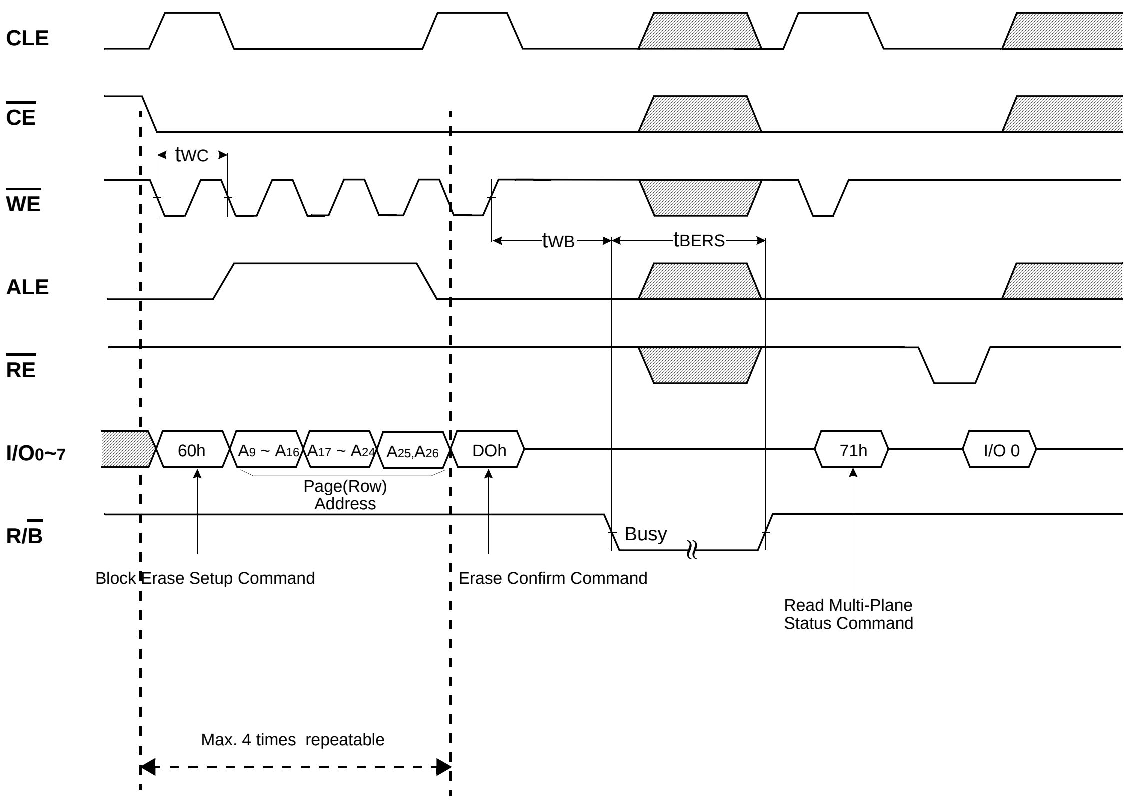
Multi-Plane Page Program Operation



Ex.) Four-Plane Page Program into Plane 0~3 or Plane 4~7

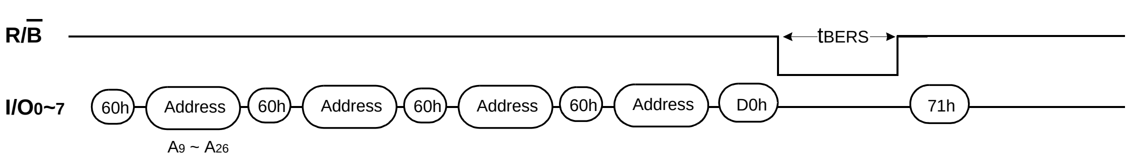


Multi-Plane Block Erase Operation into Plane 0~3 or Plane 4~7

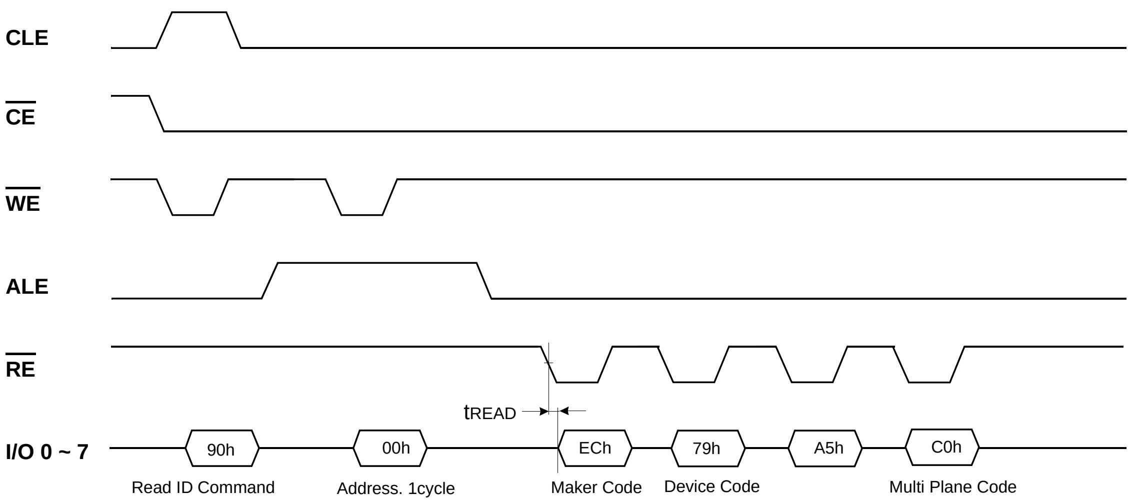


* For Multi-Plane Erase operation, Block address to be erased should be repeated before "D0H" command.

Ex.) Four-Plane Block Erase Operation



Read ID Operation

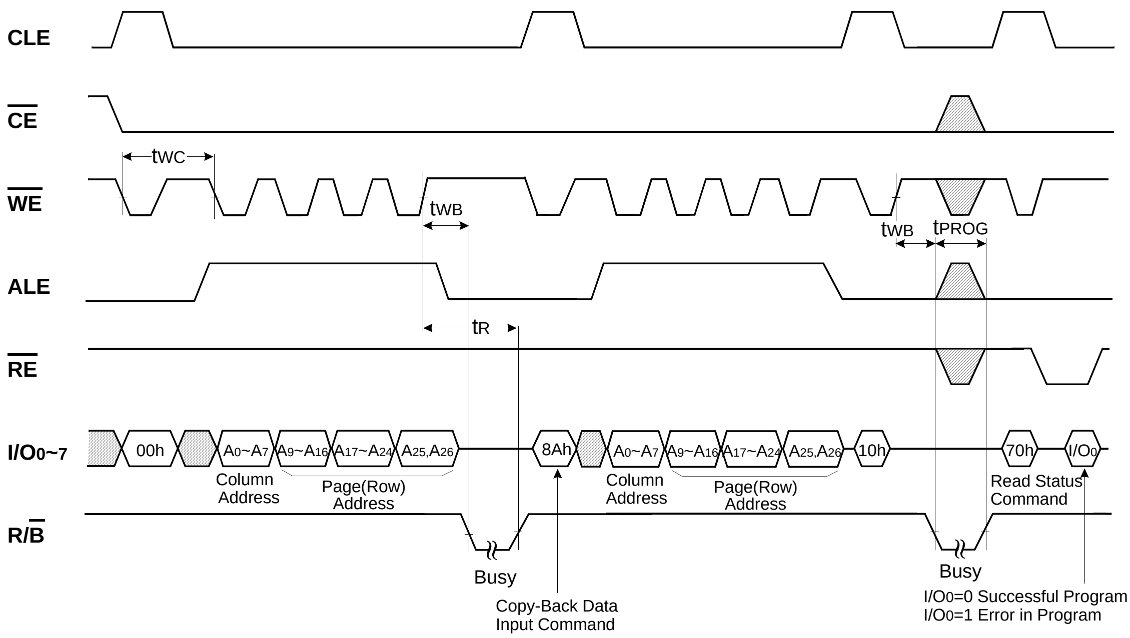


ID Defintition Table

90 ID : Access command = 90H

	Value	Description
1st Byte	ECh	Maker Code
2nd Byte	79h	Device Code
3rd Byte	A5h	Must be don't -cared
4th Byte	**C0h**	**Supports Multi Plane Operation (Must be don't-cared for 1.8V device)**

Copy-Back Program Operation



Device Operation

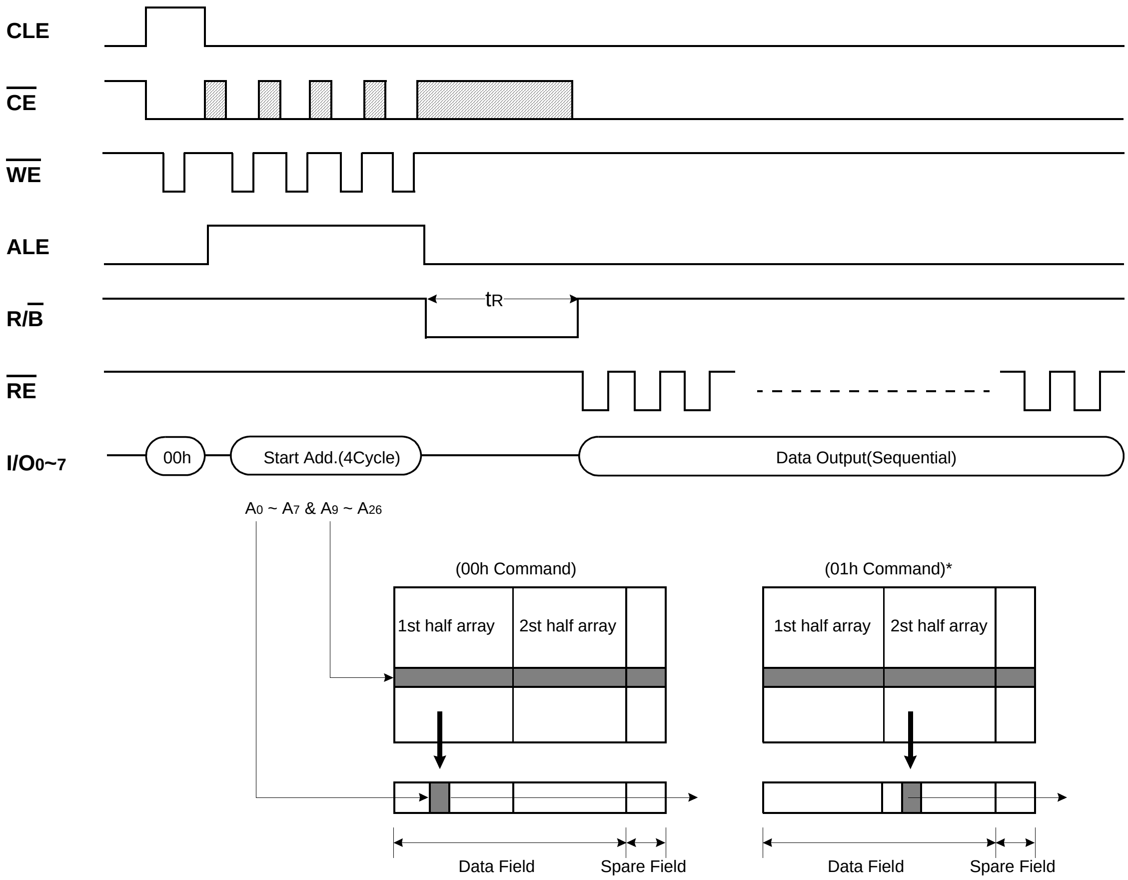
PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 15µs(t_R). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.

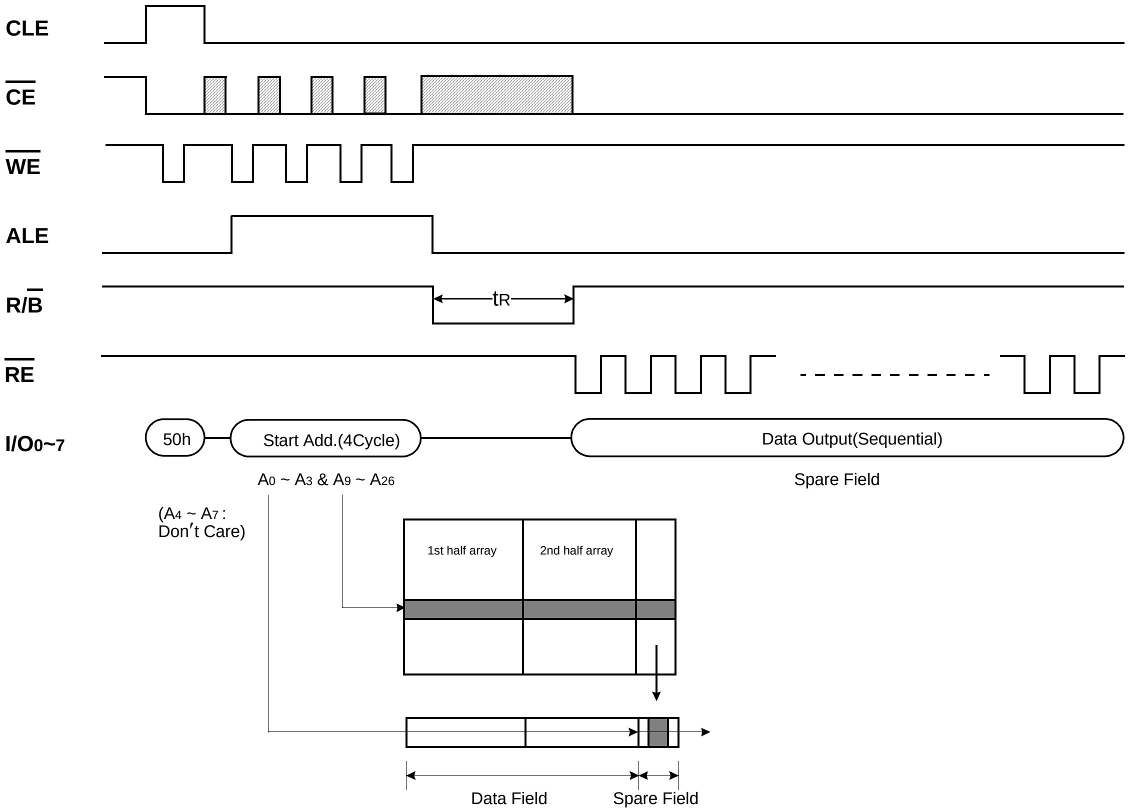
The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 9 to 12 show typical sequence and timings for each read operation.

Figure 8. Read1 Operation



* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 9. Read2 Operation

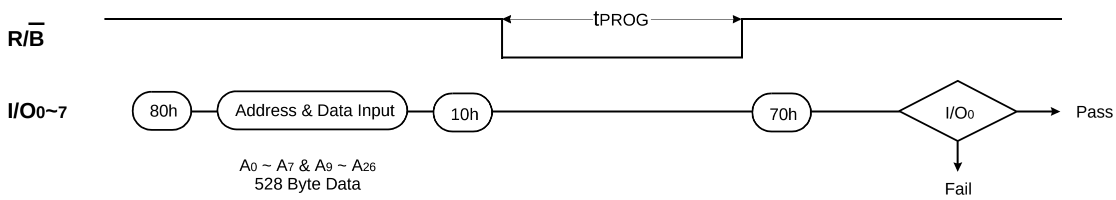


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 10). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 10. Program & Read Status Operation

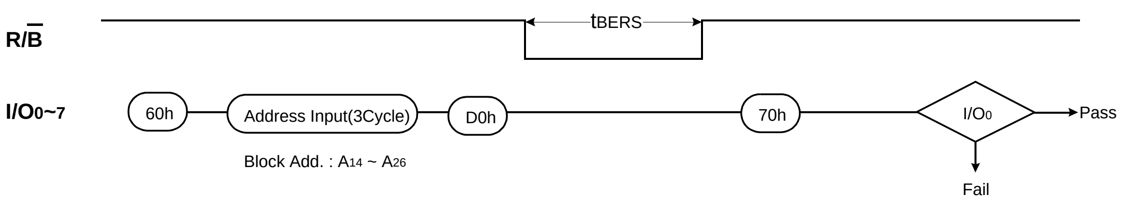


BLOCK ERASE

The Erase operation is done on a block(16K Byte) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{14} to A_{26} is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 11 details the sequence.

Figure 11. Block Erase Operation

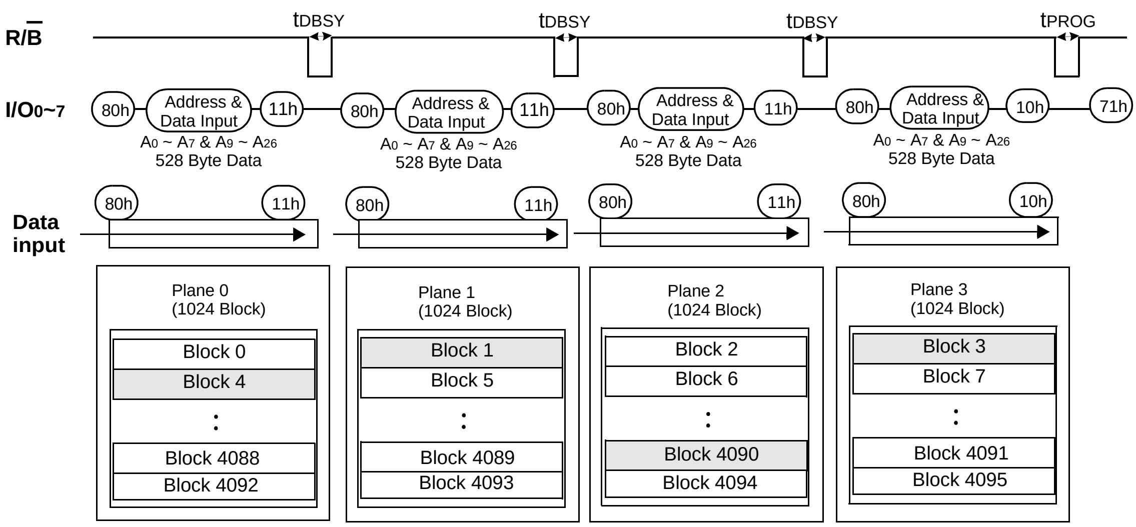


Multi-Plane Page Program into Plane 0~3 or Plane 4~7

Multi-Plane Page Program is an extension of Page Program, which is executed for a single plane with 528 byte page registers. Since the device is equipped with eight memory planes, activating the four sets of 528 byte page registers into plane 0~3 or plane 4~7 enables a simultaneous programming of four pages. Partial activation of four planes is also permitted.

After writing the first set of data up to 528 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program (10h) is inputted to finish data-loading of the current plane and move to the next plane. Since no programming process is involved, R/B remains in Busy state for a short period of time(tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for one of the other planes is inputted with the same command and address sequences. After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Since maximum four pages into plane 0~3 or plane 4~7 are programmed simultaneously, pass/fail status is available for each page when the program operation completes. The extended status bits (I/O1 through I/O 4) are checked by inputting the Read Multi-Plane Status Register. Status bit of I/O 0 is set to "1" when any of the pages fails.
Multi-Plane page Program with "01h" pointer is not supported, thus prohibited.

Figure 12. Four-Plane Page Program



Restirction in addressing with Multi Plane Page Program

While any block in each plane may be addressable for Multi-Plane Page Program, the four least significant addresses(A9-A13) for the selected pages at one operation must be the same. Figure 13 shows an example where 2nd page of each addressed block is selected for four planes. However, any arbitrary sequence is allowed in addressing multiple planes as shown in Figure17.

Figure 13. Multi-Plane Program & Read Status Operation

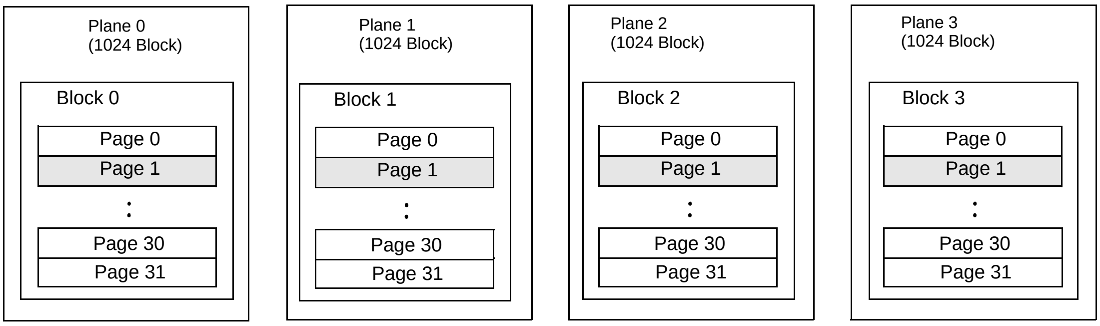


Figure 14. Addressing Multiple Planes

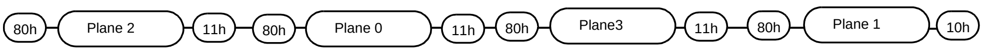
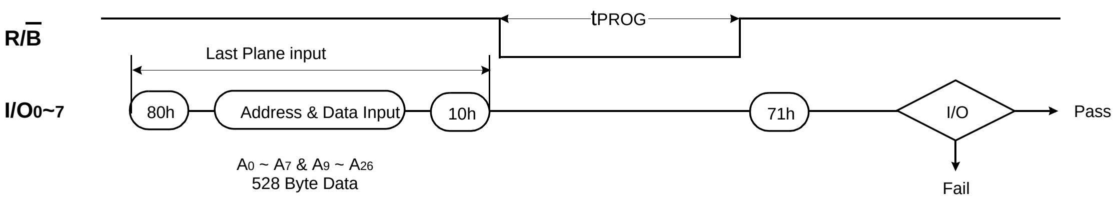


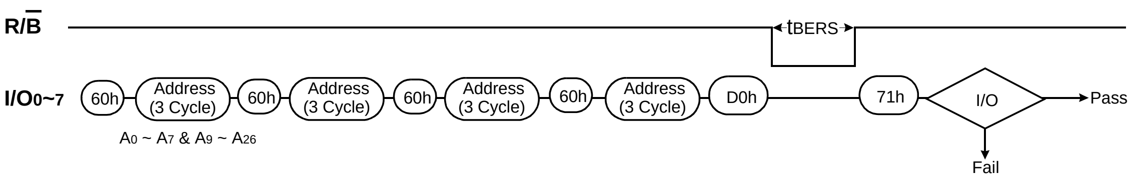
Figure 15. Multi-Plane Page Program & Read Status Operation



Multi-Plane Block Erase into Plane 0~3 or Plane 4~7

Basic concept of Multi-Plane Block Erase operation is identical to that of Multi-Plane Page Program. Up to four blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command followed by three address cycles) may be repeated up to four times for erasing up to four blocks. Only one block should be selected from each plane. The Erase Confirm command initiates the actual erasing process. The completion is detected by analyzing R/$\overline{B}$ pin or Ready/Busy status (I/O 6). Upon the erase completion, pass/fail status of each block is examined by reading extended pass/fail status(I/O 1 through I/O 4).

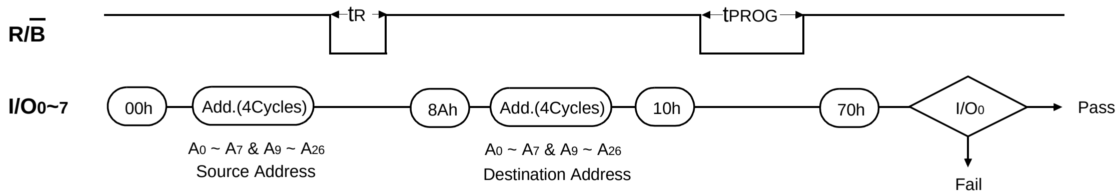
Figure 16. Four Block Erase Operation



Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. A14, A15 and A26 must be the same between source and target page. Figure20 shows the command sequence for single plane operation. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But if the soure page has a bit error for charge loss, accumulated copy-back operations could also accumulate bit errors. For this reason, two bit ECC is recommended for copy-back operation. "**

Figure 17. One Page Copy-Back program Operation



Multi-Plane Copy-Back Program

Multi-Plane Copy-Back Program is an extension of one page Copy-Back Program into four plane operation. Since the device is equipped with four memory planes, activating the four sets of 528 bytes page registers enables a simultaneous Multi-Plane Copy-Back programming of four pages. Partial activation of four planes is also permitted.

First, normal read operation with the "00h"command and address of the source page moves the whole 528 byte data into internal page buffers. Any further read operation for transferring the addressed pages to the corresponding page register must be executed with "03h" command instead of "00h" command. Any plane may be selected without regard to "00h" or "03h". Up to four planes may be addressed. Data moved into the internal page registers are loaded into the destination plane addresses. After the input of command sequences for reading the source pages, the same procedure as Multi-Plane Page programming except for a replacement address command with "8Ah" is executed. Since no programming process is involved during data loading at the destination plane address , R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program. Since maximum four pages are programmed simultaneously, pass/fail status is available for each page when the program operation completes. No pointer operation is supported with Multi-Plane Copy-Back Program. **Once the Multi-Plane Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase once the Multi-Plane Copy-Back Program is finished.**

Figure 18. Four-Plane Copy-Back Program

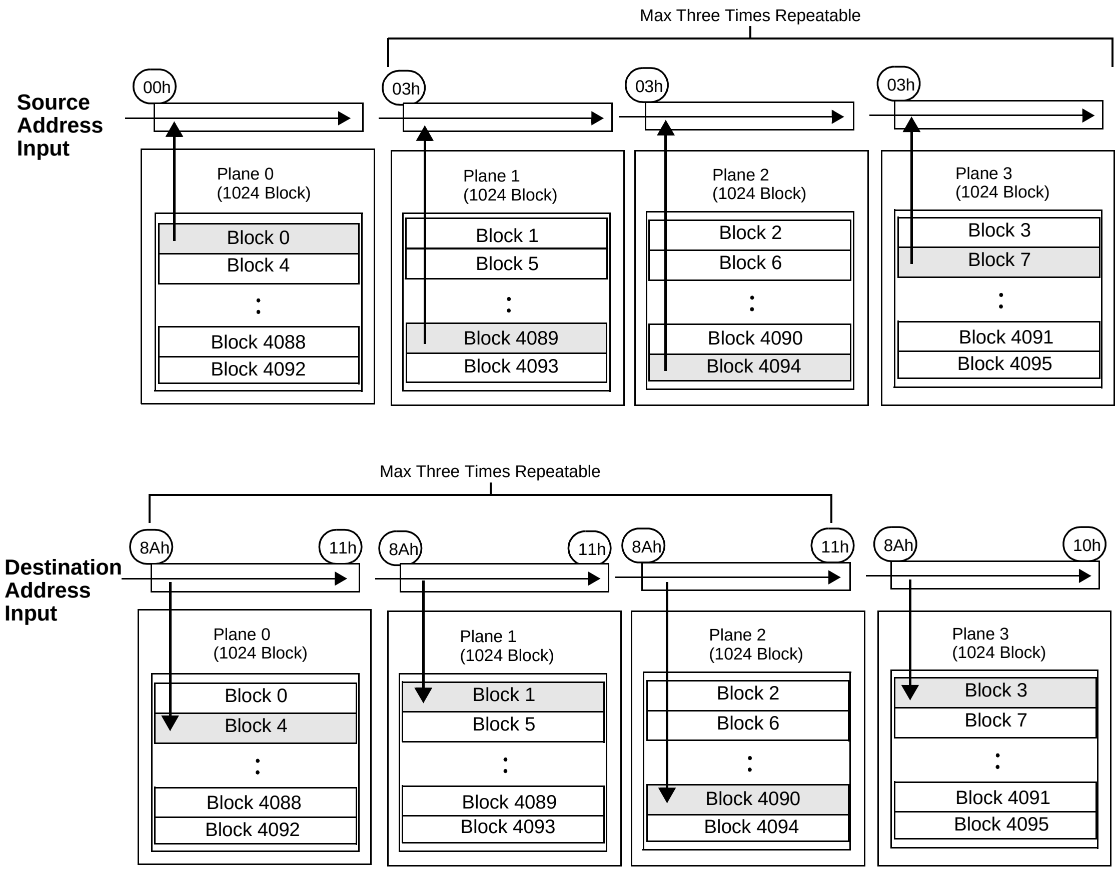
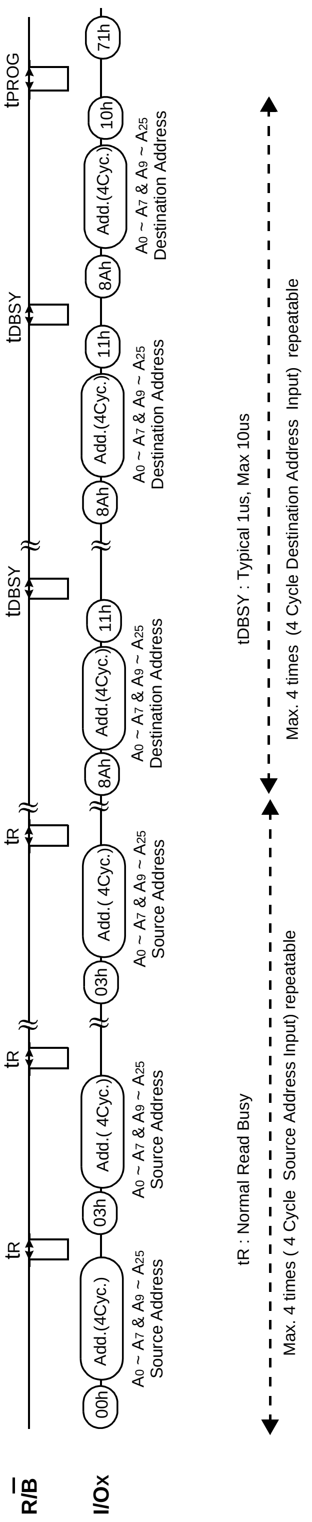


Figure 19. Four-Plane Copy-Back Page Program (Continued)



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

For Read Status of Multi Plane Program/Erase, the Read Multi-Plane Status command(71h) should be used to find out whether multi-plane program or erase operation is completed, and whether the program or erase operation is completed successfully. The pass/fail status data must be checked only in the Ready condition after the completion of Multi-Plane program or erase operation.

Table4. Read Staus Register Definition

I/O No.	Status	Definition by 70h Command	Definition by 71h Command
I/O 0	Total Pass/Fail	Pass : "0" Fail : "1"	Pass : "0"[1] Fail : "1"
I/O 1	Plane 0 Pass/Fail	Must be don't -cared	Pass : "0"[2] Fail : "1"
I/O 2	Plane 1 Pass/Fail	Must be don't -cared	Pass : "0"[2] Fail : "1"
I/O 3	Plane 2 Pass/Fail	Must be don't -cared	Pass : "0"[2] Fail : "1"
I/O 4	Plane 3 Pass/Fail	Must be don't -cared	Pass : "0"[2] Fail : "1"
I/O 5	Reserved	Must be don't -cared	Must be don't-cared
I/O 6	Device Operation	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"
I/O 7	Write Protect	Protected : "0" Not Protected : "1"	Protected : "0" Not Protected : "1"

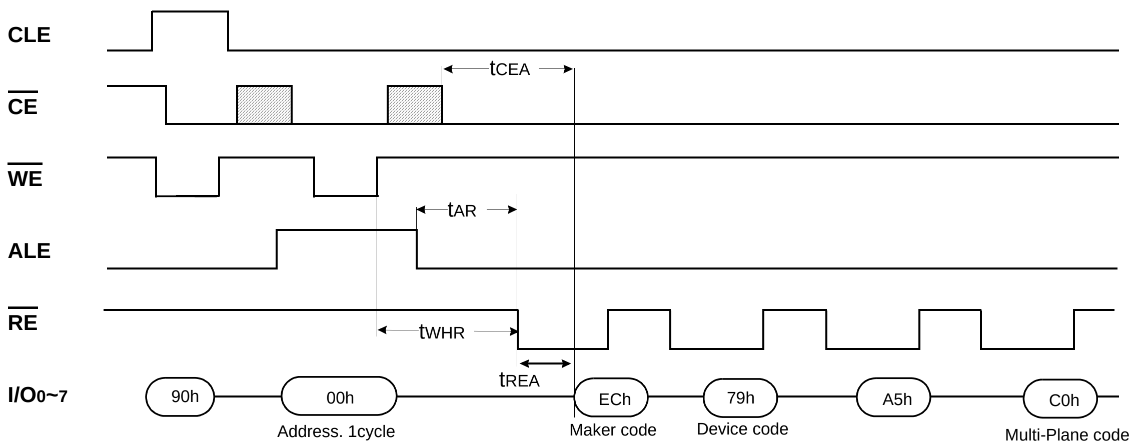
NOTE : 1. I/O 0 describes combined Pass/Fail condition for all planes. If any of the selected multiple pages/blocks fails in Program/ Erase operation, it sets "Fail" flag.

2. The pass/fail status applies only to the corresponding plane.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacture code(ECh), and the device code*, Reserved(A5h), Multi plane operation code(C0h) respectively. A5h must be don't-cared. C0h means that device supports Multi Plane operation but must be don't-cared for 1.8V device. The command register remains in Read ID mode until further commands are issued to it. Figure 20 shows the operation sequence.

Figure 20. Read ID Operation 1



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 5 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 21 below.

Figure 21. RESET Operation

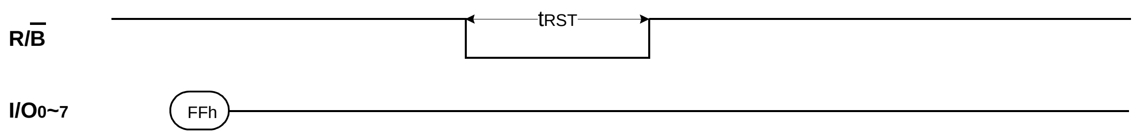


Table5. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 25). Its value can be determined by the following guidance.

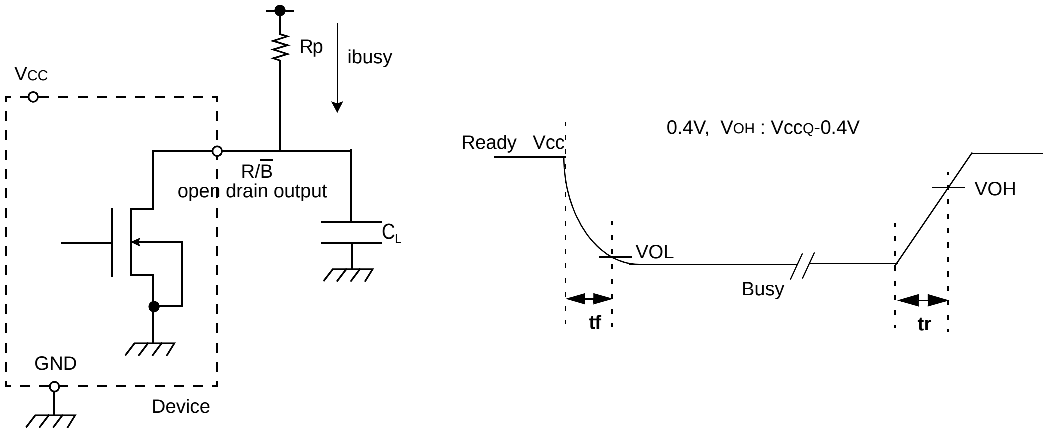
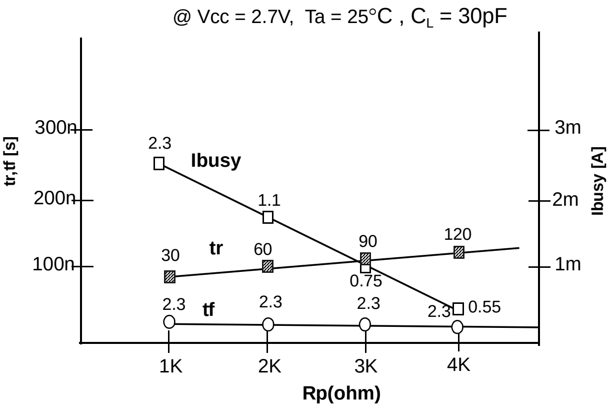


Figure 22. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

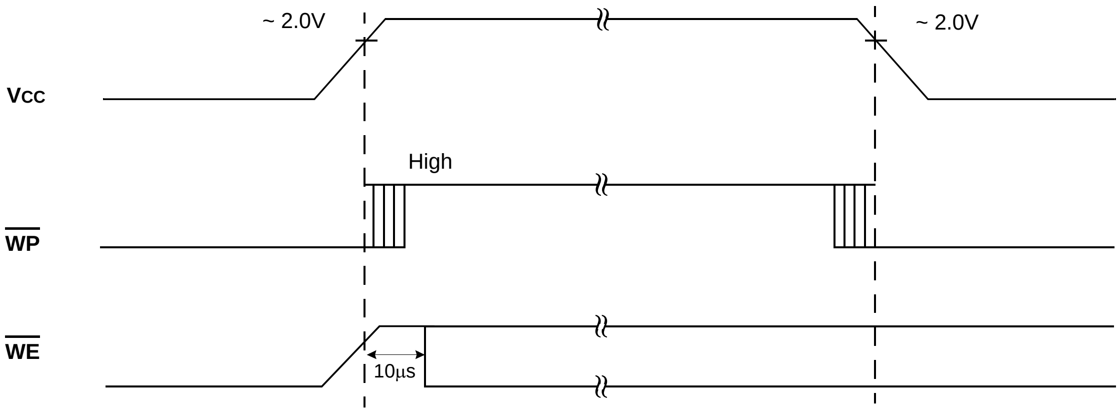
$$Rp(\text{min, 2.7V part}) = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \Sigma I_L} = \frac{2.5V}{3mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.8V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 10µs is required before internal circuit gets ready for any command sequences as shown in Figure 23. The two step command sequence for program/erase provides additional software protection.

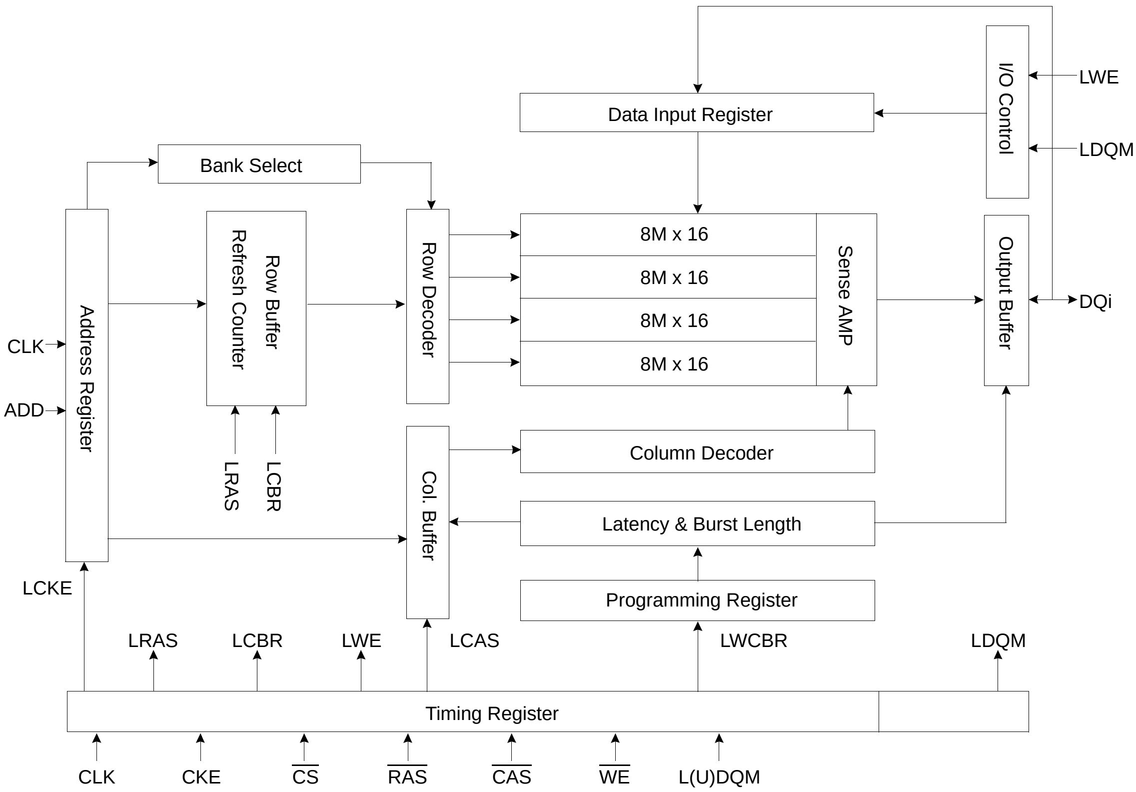
Figure 23. AC Waveforms for Power Transition



512Mb(32Mb x 16)

Mobile SDRAM DDP F-Die

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 2.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 2.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTES:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.8	1.95	V	
	V_{DDQ}	1.7	1.8	1.95	V	
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V_{OH}	V_{DDQ} -0.2	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.2	V	I_{OL} = 0.1mA
Input leakage current	I_{LI}	-2	-	2	uA	3

NOTES :
1. VIH (max) = 2.2V AC.The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -1.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
4. Dout is disabled, 0V ≤ VOUT ≤ VDDQ.

CAPACITANCE (V_{DD} = 1.8V, T_A = 23°C, f = 1MHz, V_{REF} =0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.5	6	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE	C_{IN}	2.5	6	pF	
DQM	C_{IN}	1.5	3	pF	
Address	C_{ADD}	2.5	6	pF	
DQ_0 ~ DQ_{15}	C_{OUT}	3	5	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85°C)

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="2">Test Condition</th><th colspan="2">KBE00G003M-D411</th><th>Unit</th><th>Note</th></tr>
<tr><td>Operating Current
(One Bank Active)</td><td>I_{CC1}</td><td colspan="2">Burst length = 1
$t_{RC} \geq t_{RC}$(min)
I_O = 0 mA</td><td colspan="2">80</td><td>mA</td><td>1</td></tr>
<tr><td rowspan="2">Precharge Standby Current in power-down mode</td><td>I_{CC2}P</td><td colspan="2">CKE ≤ V_{IL}(max), t_{CC} = 10ns</td><td colspan="2">0.6</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC2}PS</td><td colspan="2">CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞</td><td colspan="2">0.6</td></tr>
<tr><td rowspan="2">Precharge Standby Current in non power-down mode</td><td>I_{CC2}N</td><td colspan="2">CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns
Input signals are changed one time during 20ns</td><td colspan="2">20</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC2}NS</td><td colspan="2">CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞
Input signals are stable</td><td colspan="2">2</td></tr>
<tr><td rowspan="2">Active Standby Current
in power-down mode</td><td>I_{CC3}P</td><td colspan="2">CKE ≤ V_{IL}(max), t_{CC} = 10ns</td><td colspan="2">10</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC3}PS</td><td colspan="2">CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞</td><td colspan="2">2</td></tr>
<tr><td rowspan="2">Active Standby Current
in non power-down mode
(One Bank Active)</td><td>I_{CC3}N</td><td colspan="2">CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns
Input signals are changed one time during 20ns</td><td colspan="2">40</td><td>mA</td><td></td></tr>
<tr><td>I_{CC3}NS</td><td colspan="2">CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞
Input signals are stable</td><td colspan="2">10</td><td>mA</td><td></td></tr>
<tr><td>Operating Current
(Burst Mode)</td><td>I_{CC4}</td><td colspan="2">I_O = 0 mA
Page burst
4Banks Activated
t_{CCD} = 2CLKs</td><td colspan="2">120</td><td>mA</td><td>1</td></tr>
<tr><td>Refresh Current</td><td>I_{CC5}</td><td colspan="2">$t_{ARFC} \geq t_{ARFC}$(min)</td><td colspan="2">130</td><td>mA</td><td></td></tr>
<tr><td rowspan="4">Self Refresh Current</td><td rowspan="4">I_{CC6}</td><td rowspan="4">CKE ≤ 0.2V</td><td>TCSR Range</td><td>Max 40</td><td>Max 85</td><td>°C</td><td></td></tr>
<tr><td>Full Array</td><td>300</td><td>800</td><td rowspan="3">uA</td><td rowspan="3"></td></tr>
<tr><td>1/2 of Full Array</td><td>240</td><td>600</td></tr>
<tr><td>1/4 of Full Array</td><td>200</td><td>500</td></tr>
</table>

NOTES:
1. Measured with outputs open.
2. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ).

AC OPERATING TEST CONDITIONS(V_{DD} = 1.7V ~ 1.95V, T_A = -25 to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.9 x V_{DDQ} / 0.2	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	0.5 x V_{DDQ}	V
Output load condition	See Figure 2	

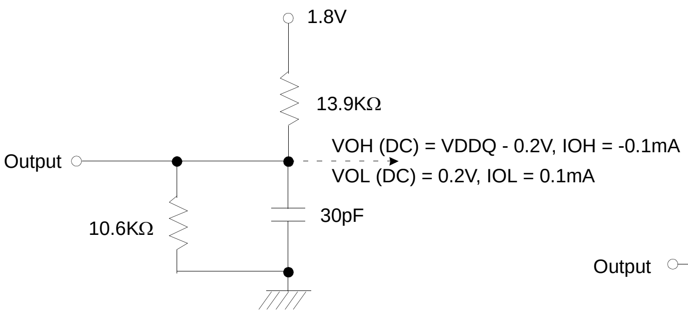


Figure 1. DC Output Load Circuit

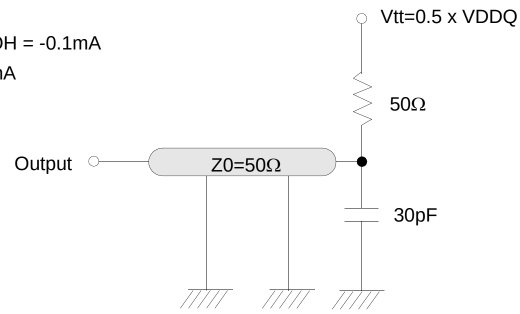


Figure 2. AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	KBE00G003M-D411	Unit	Note
Row active to row active delay	t_{RRD}(min)	18	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}(min)	27	ns	1
Row precharge time	t_{RP}(min)	27	ns	1
Row active time	t_{RAS}(min)	50	ns	1
	t_{RAS}(max)	100	us	
Row cycle time	t_{RC}(min)	77	ns	1
Last data in to row precharge	t_{RDL}(min)	15	ns	2
Last data in to Active delay	t_{DAL}(min)	tRDL + tRP	-	
Last data in to new col. address delay	t_{CDL}(min)	1	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	CLK	2
Auto refresh cycle time	t_{ARFC}(min)	80	ns	
Exit self refresh to active command	t_{SRFX}(min)	120	ns	
Col. address to col. address delay	t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4

NOTES:
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	KBE00F003M-D411		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	9	1000	ns	1
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
Output data hold time	CAS latency=3	t_{OH}	2.0		ns	2
CLK high pulse width		t_{CH}	3.0		ns	3
CLK low pulse width		t_{CL}	3.0		ns	3
Input setup time		t_{SS}	2.0		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	

NOTES :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12,A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don′t Care, H=Logic High, L=Logic Low)

NOTES :

1. OP Code : Operand Code
   A0 ~ A12 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
   Partial self refresh can be issued only after setting partial self refresh mode of EMRS.
4. BA0 ~ BA1 : Bank select addresses.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1	A12 ~ A10/AP	A9[*2]	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU[*1]	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

Full Page Length x16 : 512Mb(1024)

Register Programmed with Extended MRS

Address	BA1	BA0	A12 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU[*1]				DS		RFU[*1]		PASR		

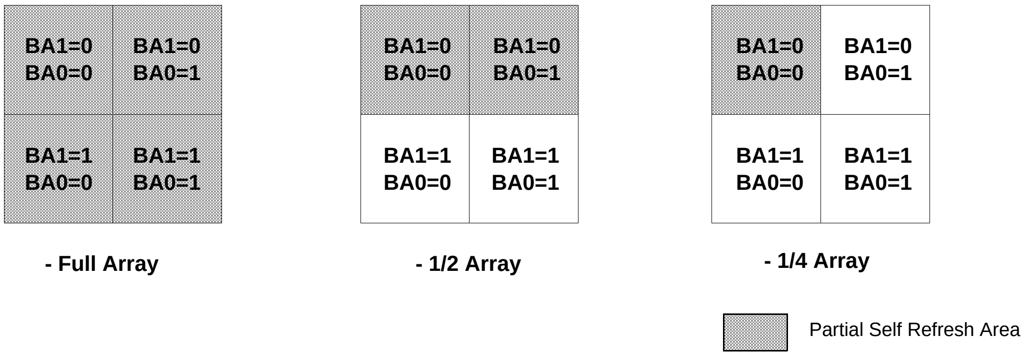
EMRS for PASR(Partial Array Self Ref.) & DS(Driver Strength)

Mode Select			Driver Strength			PASR			
BA1	BA0	Mode	A6	A5	Driver Strength	A2	A1	A0	Size of Refreshed Area
0	0	Normal MRS	0	0	Full	0	0	0	Full Array
0	1	Reserved	0	1	1/2	0	0	1	1/2 of Full Array
1	0	EMRS for Mobile SDRAM	1	0	1/4	0	1	0	1/4 of Full Array
1	1	Reserved	1	1	1/8	0	1	1	Reserved
Reserved Address						1	0	0	Reserved
A12~A10/AP	A9	A8	A7	A4	A3	1	0	1	Reserved
0	0	0	0	0	0	1	1	0	Reserved
						1	1	1	Reserved

NOTES:
1.RFU(Reserved for future use) should stay "0" during MRS cycle.
2.If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.

Partial Array Self Refresh

1. In order to save power consumption, Mobile SDRAM has PASR option.
2. Mobile SDRAM supports 3 kinds of PASR in self refresh mode : Full Array, 1/2 of Full Array, 1/4 of Full Array



Internal Temperature Compensated Self Refresh (TCSR)

Note :
1. In order to save power consumption, Mobile-SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range ; Max. 40 °C, Max. 85 °C.
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (Icc 6)			Unit
	Full Array	1/2 of Full Array	1/4 of Full Array	
Max. 40 °C	300	240	200	uA
Max. 85 °C	800	600	500	

B. POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used.
The default state without EMRS command issued is the half driver strength and full array refreshed.
The device is now ready for the operation selected by EMRS.
For operating with DS or PASR , set DS or PASR mode in EMRS setting stage.
In order to adjust another mode in the state of DS or PASR mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

C. BURST SEQUENCE

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

D. DEVICE OPERATIONS

ADDRESSES of 256Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 16

This SDRAM is organized as four independent banks of 4,194,304 words x 16 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 32

This SDRAM is organized as four independent banks of 2,097,152 words x 32 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 16

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

: In case x 32

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A0 ~ A11). The 12 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

ADDRESSES of 512Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 16

This SDRAM is organized as four independent banks of 8,388,608 words x 16 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 32

This SDRAM is organized as four independent banks of 4,194,304 words x 32 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 16

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 10 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

: In case x 32

The 22 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

D. DEVICE OPERATIONS (continued)

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock in order to function well Q perform and ICC specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time are the same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + tSS" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interruptions of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0 ~ An and BA0 ~ BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on the fields of functions. The burst length field uses A0 ~ A2, burst type uses A3, CAS latency (read latency from column address) use A4 ~ A6, vendor specific options or test mode use A7 ~ A8, A10/AP ~ An and BA0 ~ BA1. The write burst length is programmed using A9. A7 ~ A8, A10/AP ~ An and BA0 ~ BA1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

D. DEVICE OPERATIONS (continued)

EXTENDED MODE REGISTER SET (EMRS)

The extended mode register stores the data for selecting driver strength and partial self refresh. EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used. The default state without EMRS command issued is the half driver strength, and full array refreshed. The extended mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and high on BA1 ,low on BA0(The SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A12 in the same cycle as $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 - A2 are used for partial self refresh , A5 - A6 are used for Driver strength, "Low" on BA0 and "High" on BA1 are used for EMRS. All the other address pins except A0-A2, A5-A6, and BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.

BANK ACTIVATE.

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer.

The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high, requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{\text{CS}}$ and $\overline{\text{CAS}}$ with $\overline{\text{WE}}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

D. DEVICE OPERATIONS (continued)

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

ALL BANKS PRECHARGE

All banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge to all the banks, all banks are in idle state.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid BA0 ~ BA1 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A10/AP. If burst read or burst write by asserting high on A10/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

AUTO REFRESH

The storage cells of 64Mb, 128Mb, 256Mb and 512Mb SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with all banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{ARFC}(min). The minimum number of clock cycles required can be calculated by driving t_{ARFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The 64Mb and 128Mb SDRAM's auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms. The 256Mb and 512Mb SDRAM's auto refresh cycle can be performed once in 7.8us or a burst of 8192 auto refresh cycles once in 64ms.

D. DEVICE OPERATIONS(continued)

SELF REFRESH

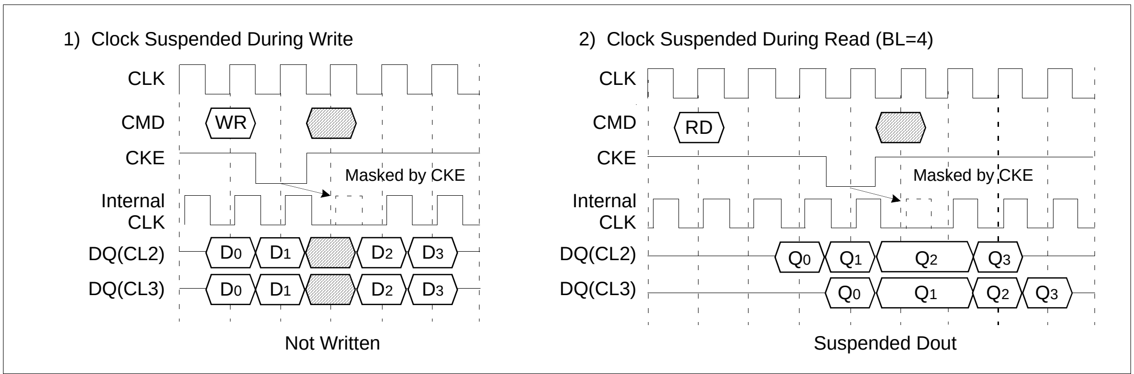
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

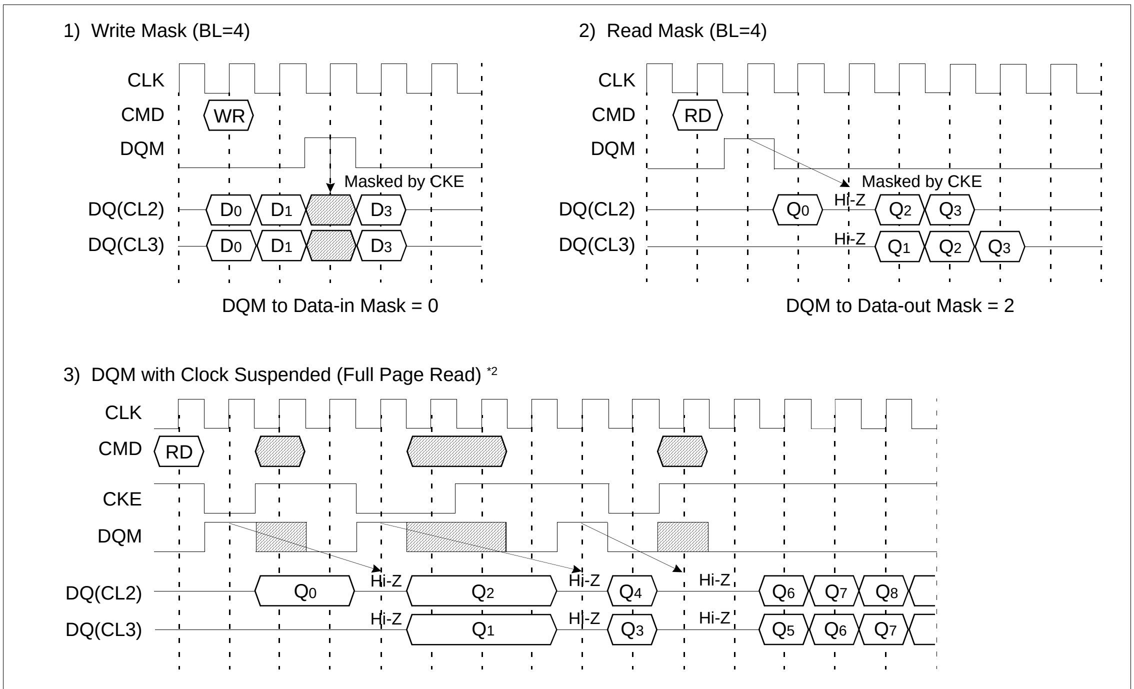
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{SRFX} before the SDRAM reaches idle state to begin normal operation. In case that the system uses burst auto refresh during normal operation, it is recommended to use burst 8192 auto refresh cycles for 256Mb and 512Mb, and burst 4096 auto refresh cycles for 128Mb and 64Mb immediately before entering self refresh mode and after exiting in self refresh mode. On the other hand, if the system uses the distributed auto refresh, the system only has to keep the refresh duty cycle.

E. BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

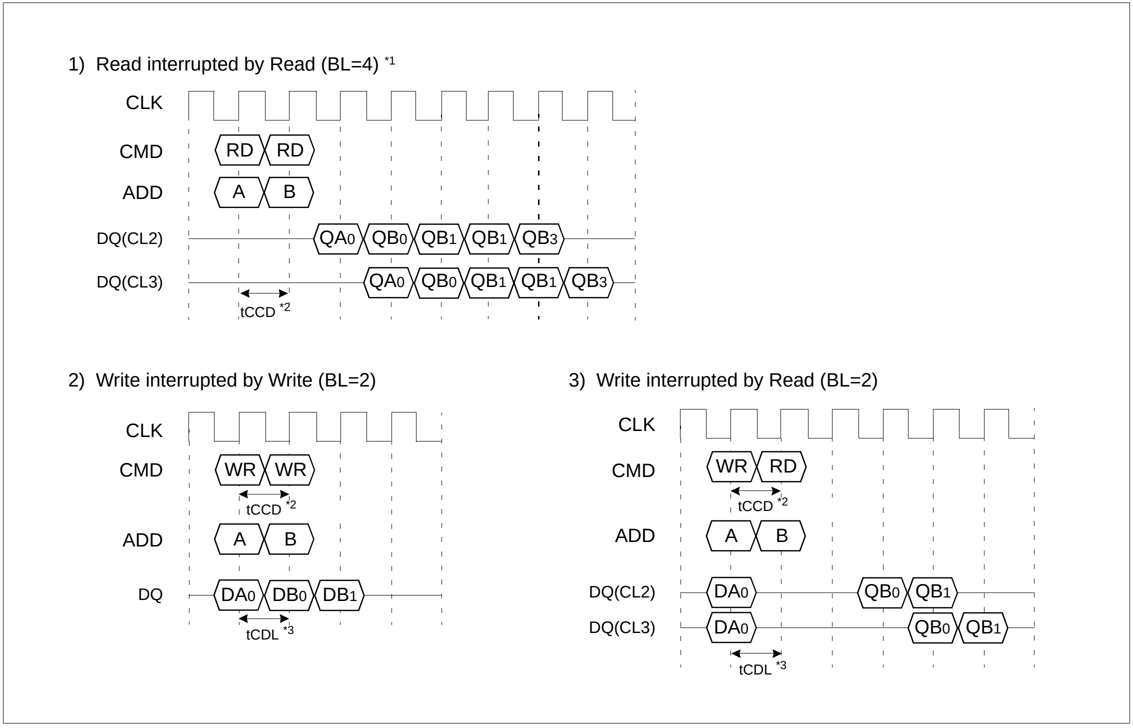


2. DQM Operation



***NOTE :**
1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

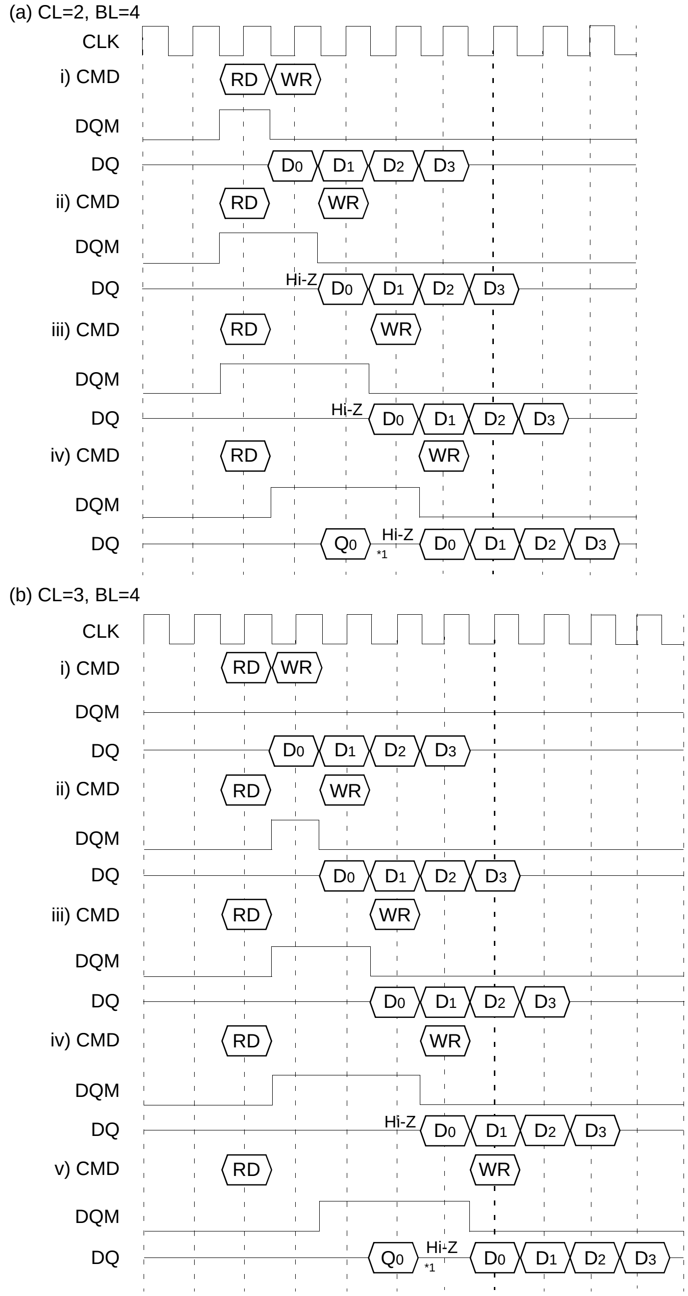
3. CAS Interrupt (I)



***NOTE:**

1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
   By "CAS Interrupt", to stop burst read/write by CAS access ; read and write.
2. tCCD : CAS to CAS delay. (=1CLK)
3. tCDL : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM

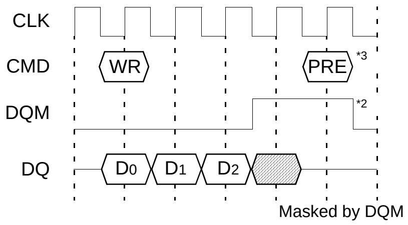


***NOTE:**

1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

1) tRDL = 2CLK



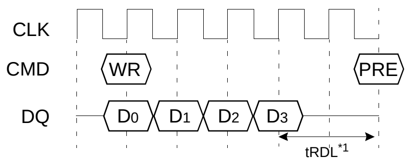
***NOTE:**

1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

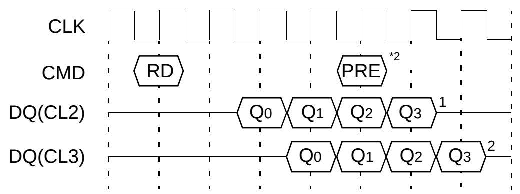
6. Precharge

1) Normal Write

BL=4 & tRDL=2CLK

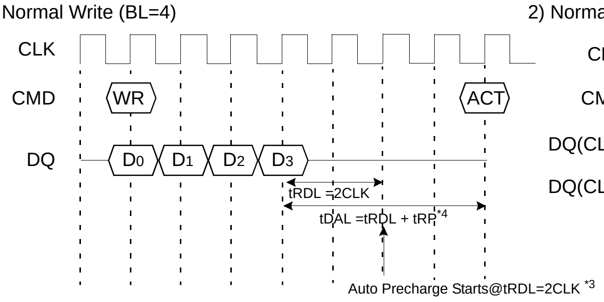


2) Normal Read (BL=4)

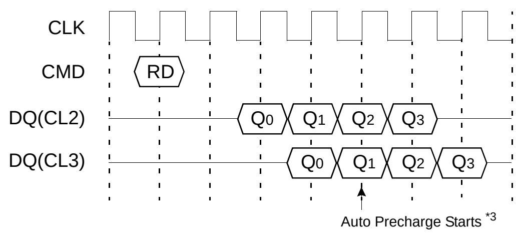


7. Auto Precharge

1) Normal Write (BL=4)



2) Normal Read (BL=4)



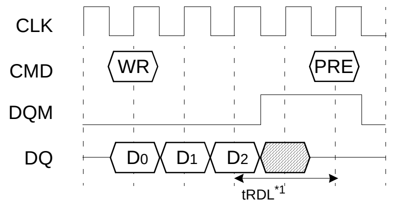
***NOTE:**

1. SAMSUNG can support tRDL=2CLK .
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
   The new read/write command of other activated bank can be issued from this point.
   At burst read/write with auto precharge, CAS interrupt of the same bank is illegal
4. tDAL defined Last data in to Active delay. SAMSUNG can support tDAL=tRDL+ tRP .

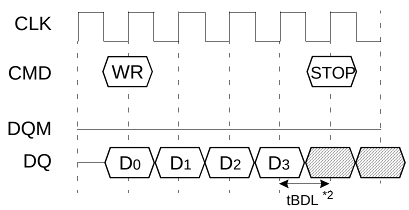
8. Burst Stop & Interrupted by Precharge

1) Normal Write

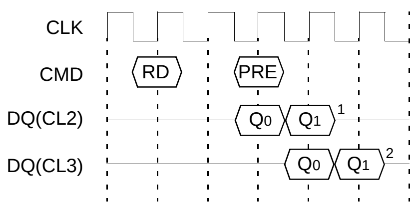
BL=4 & tRDL=2CLK



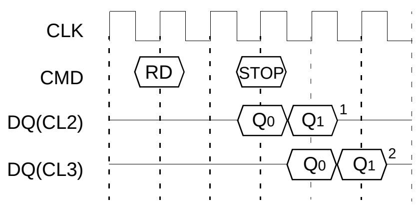
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

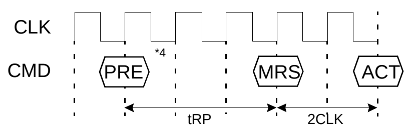


4) Read Burst Stop (BL=4)



9. MRS

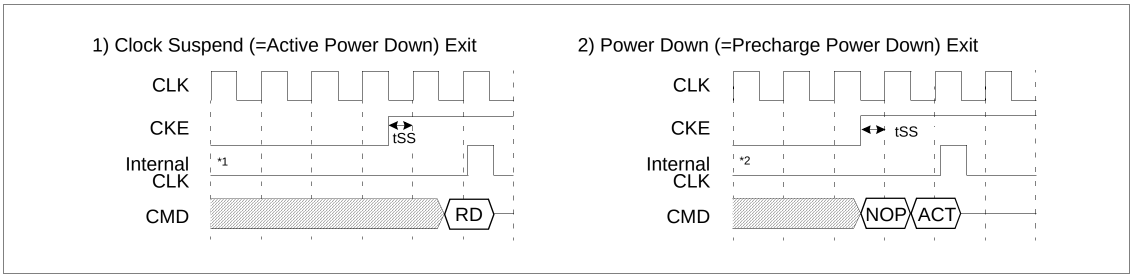
1) Mode Register Set



***NOTE:**

1. SAMSUNG can support tRDL=2CLK.
2. tBDL : 1 CLK ; Last data in to burst stop delay.
   Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectively.
4. PRE : All banks precharge is necessary.
   MRS can be issued only at all banks precharge state.

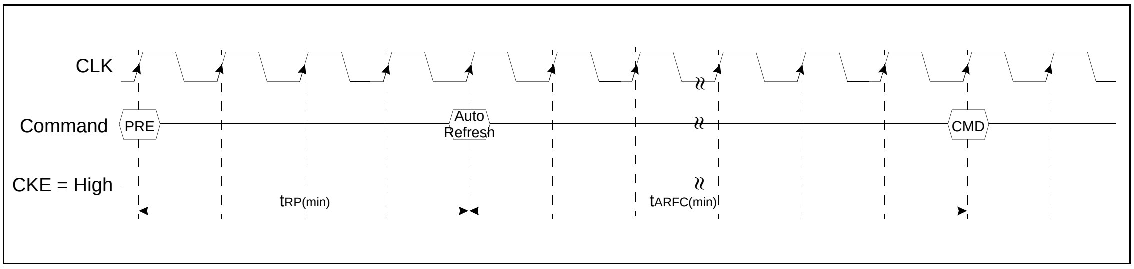
10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh

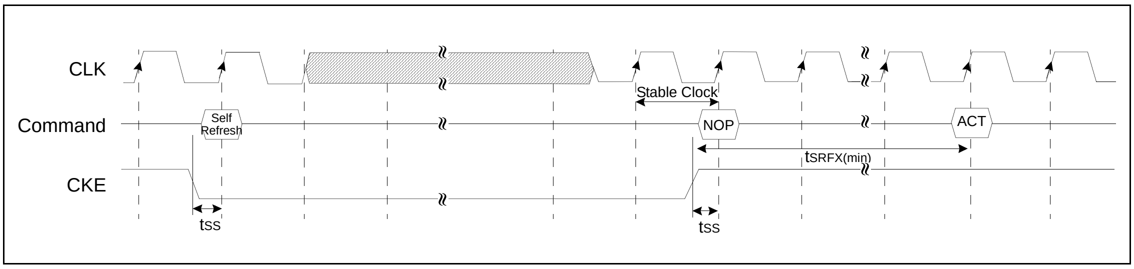
Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CLK). All banks must be precharged and idle for t_{RP}(min) before the auto refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{ARFC}(min).



Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CLK) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. To exit the Self Refresh mode, supply stable clock input before returning CKE high, assert deselect or NOP command and then assert CKE high. In case that the system uses burst auto refresh during normal opreation, it is recommended to use burst auto refresh cycle immediately before entering self refresh mode and after exiting in self refresh mode. On the other hand, if the system uses the distributed auto refresh, the system only has to keep the refresh duty cycle.



12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting.
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". Wrap around mode(infinite burst length) should be stopped by burst stop. $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt.
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1. At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 2 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A_{10}/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	

FUNCTION TRUTH TABLE (TABLE 1)

Current	CS	RAS	CAS	WE	BA	Address	Action	Note
Precharging	H	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	NOP --> Idle after t_{RP}	4
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***NOTE:**
1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state ; Function may be Iegal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

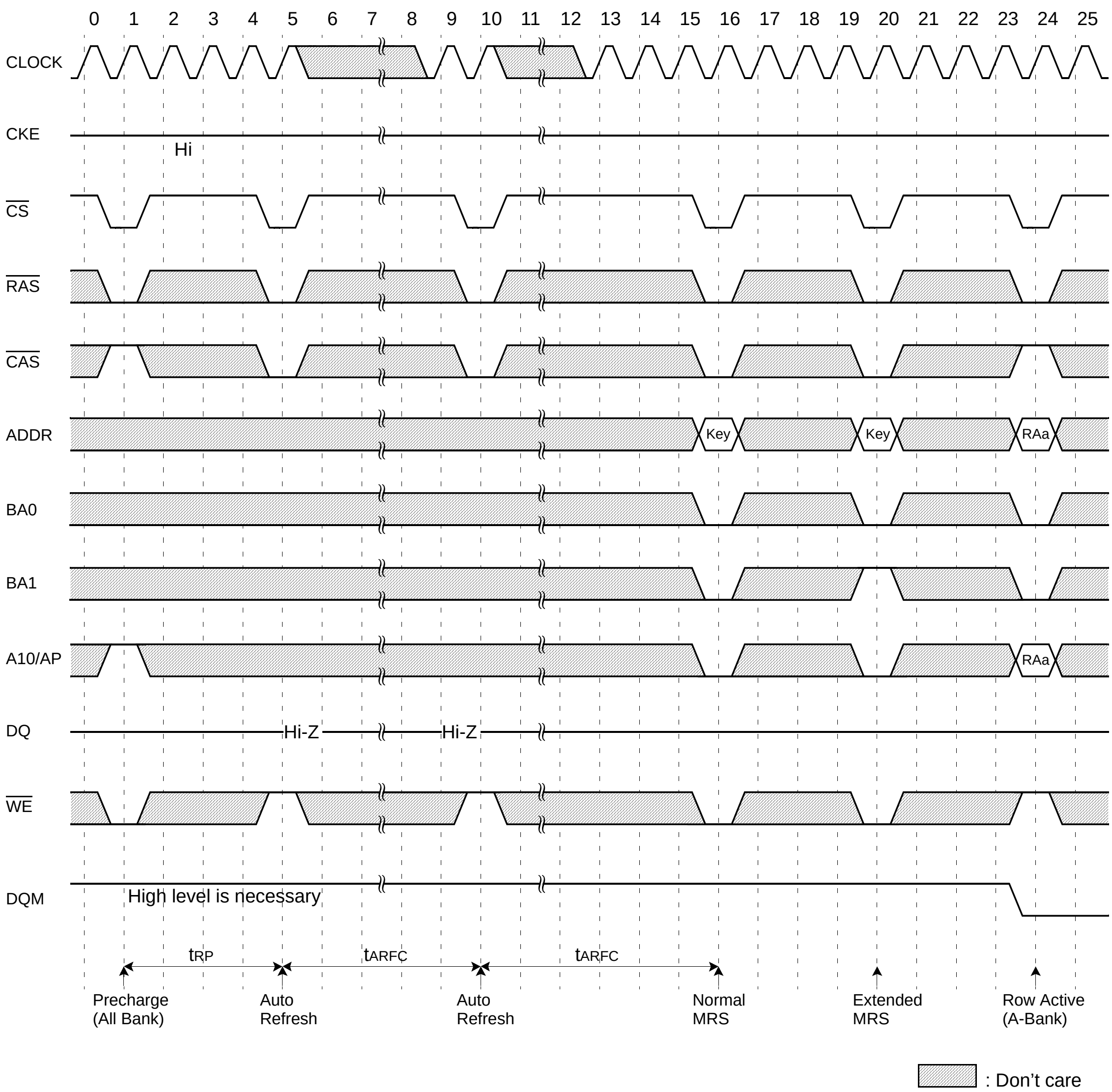
Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Note
Self Refresh	H	X	X	X	X	X	X	Exit Self Refresh --> Idle after t_{SRFX}(ABI)	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{SRFX} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{SRFX} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations : ABI = All Banks Idle, RA = Row Address

***NOTE:**
6. CKE low to high transition is asynchronous.
7. CKE low to high transition is asynchronous if restarts internal clock.
   A minimum setup time 1CLK + t_{SS} must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the all banks idle state.
9. Must be a legal command.

Power Up Sequence
Single Bit Read - Write - Read Cycle(Same Page) @CAS Latency=3, Burst Length=1
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read Cycle at Different Bank @Burst Length=4
Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK
Read & Write Cycle at Different Bank @Burst Length=4
Read & Write Cycle With Auto Precharge I @Burst Length=4
Read & Write Cycle With Auto Precharge II @Burst Length=4
Clock Suspension & DQM Operation Cycle @CAS Letency=2, Burst Length=4
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK
Burst Read Single bit Write Cycle @Burst Length =2
Active/precharge Power Dower Down Mode @CAS Latency=2 Burst Length=4
Self Refresh Entry & Exit Cycle & Exit Cycle
Mode Register Set Cycle and Auto Refresh Cycle
Extended Mode Register Set Cycle

Power Up Sequence for Mobile SDRAM

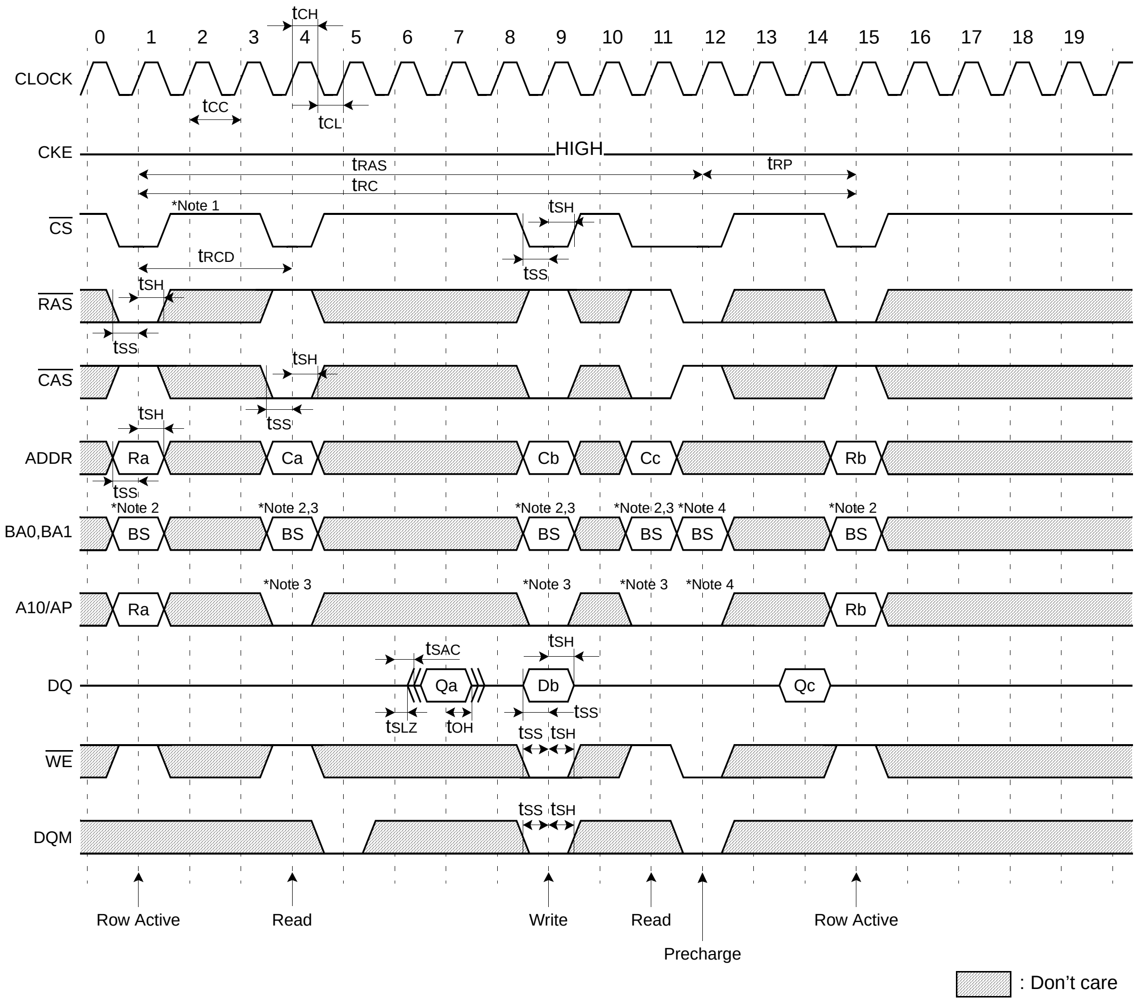


***NOTE:**

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

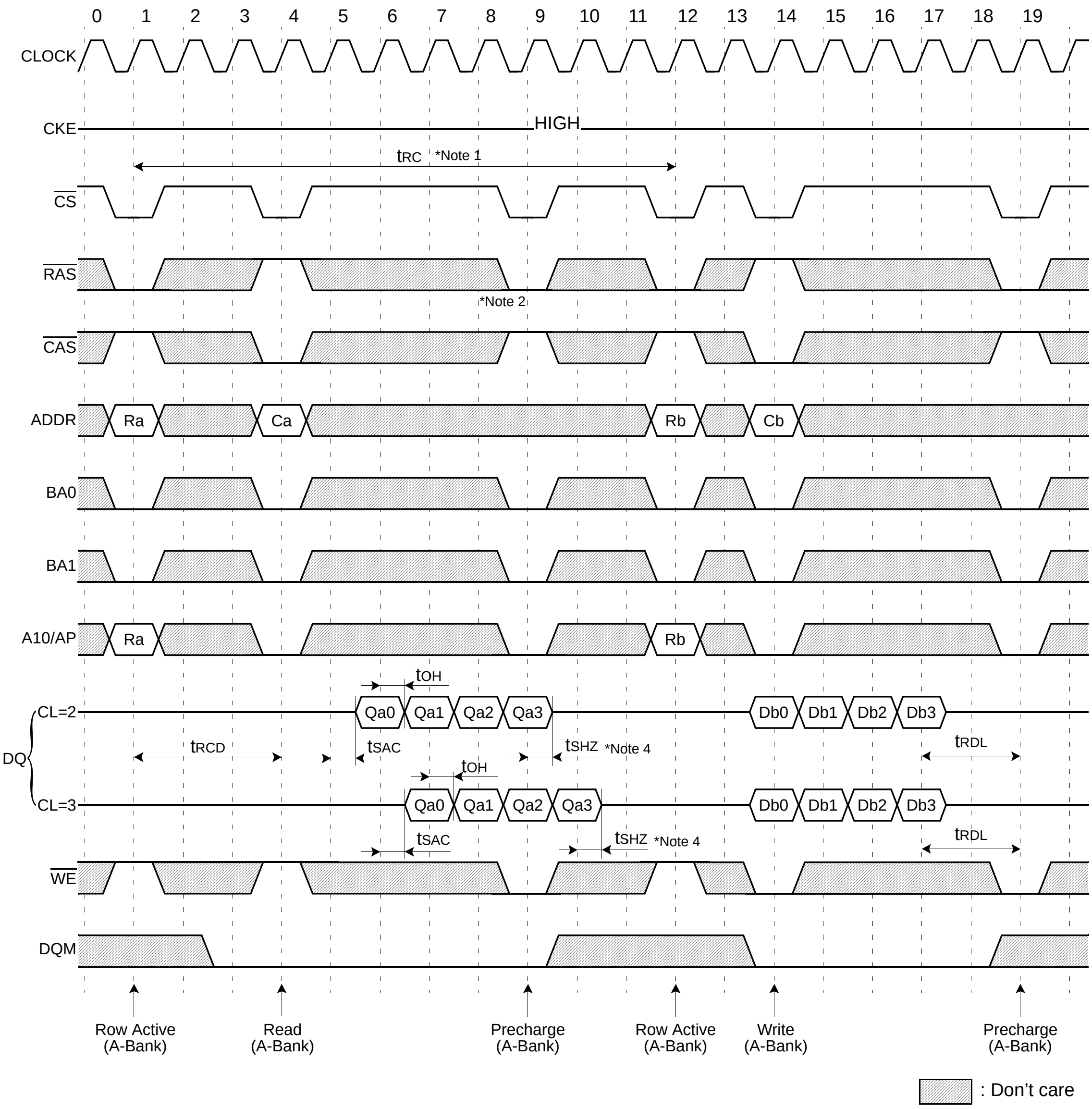
EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used.
The default state without EMRS command issued is the half driver strength and full array refreshed.
The device is now ready for the operation selected by EMRS.
For operating with DS or PASR , set DS or PASR mode in EMRS setting stage.
In order to adjust another mode in the state of DS or PASR mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



***NOTE:**
1. All input except CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0,BA1.

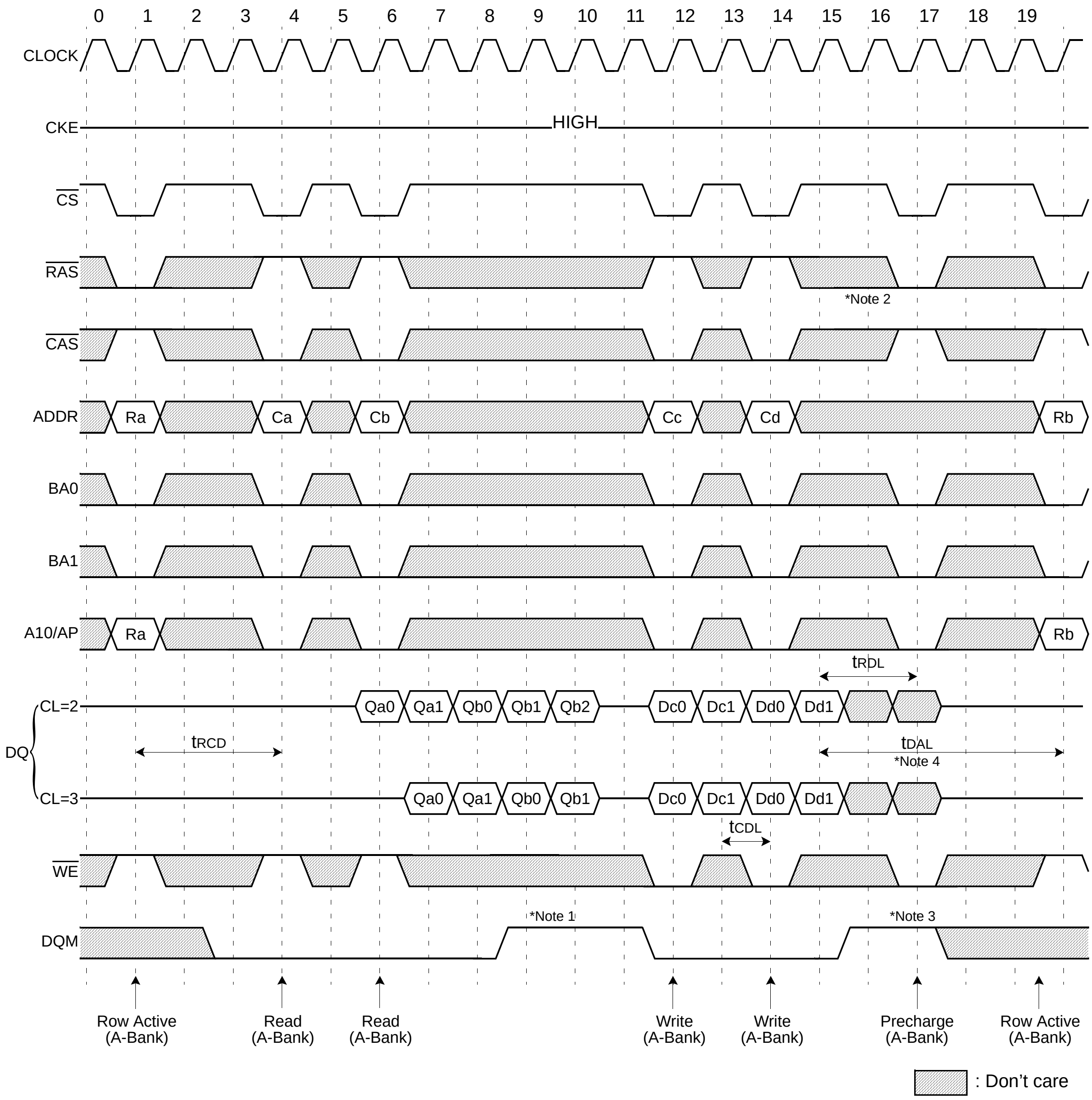
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



***NOTE:**

1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(tSHZ) after the clcok.
3. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

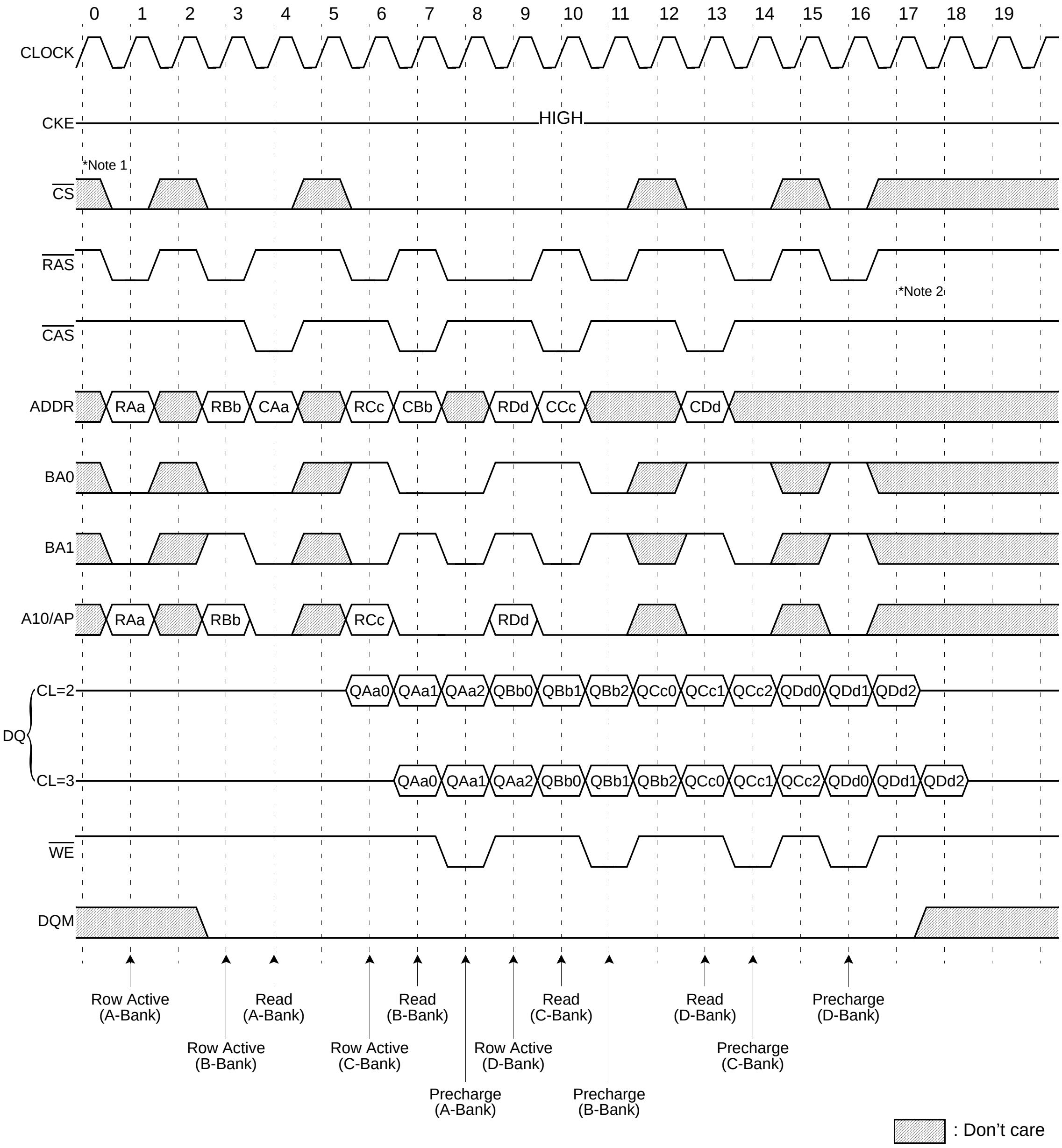
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



***NOTE:**

1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL ,last data in to active delay, is 2CLK + tRP.

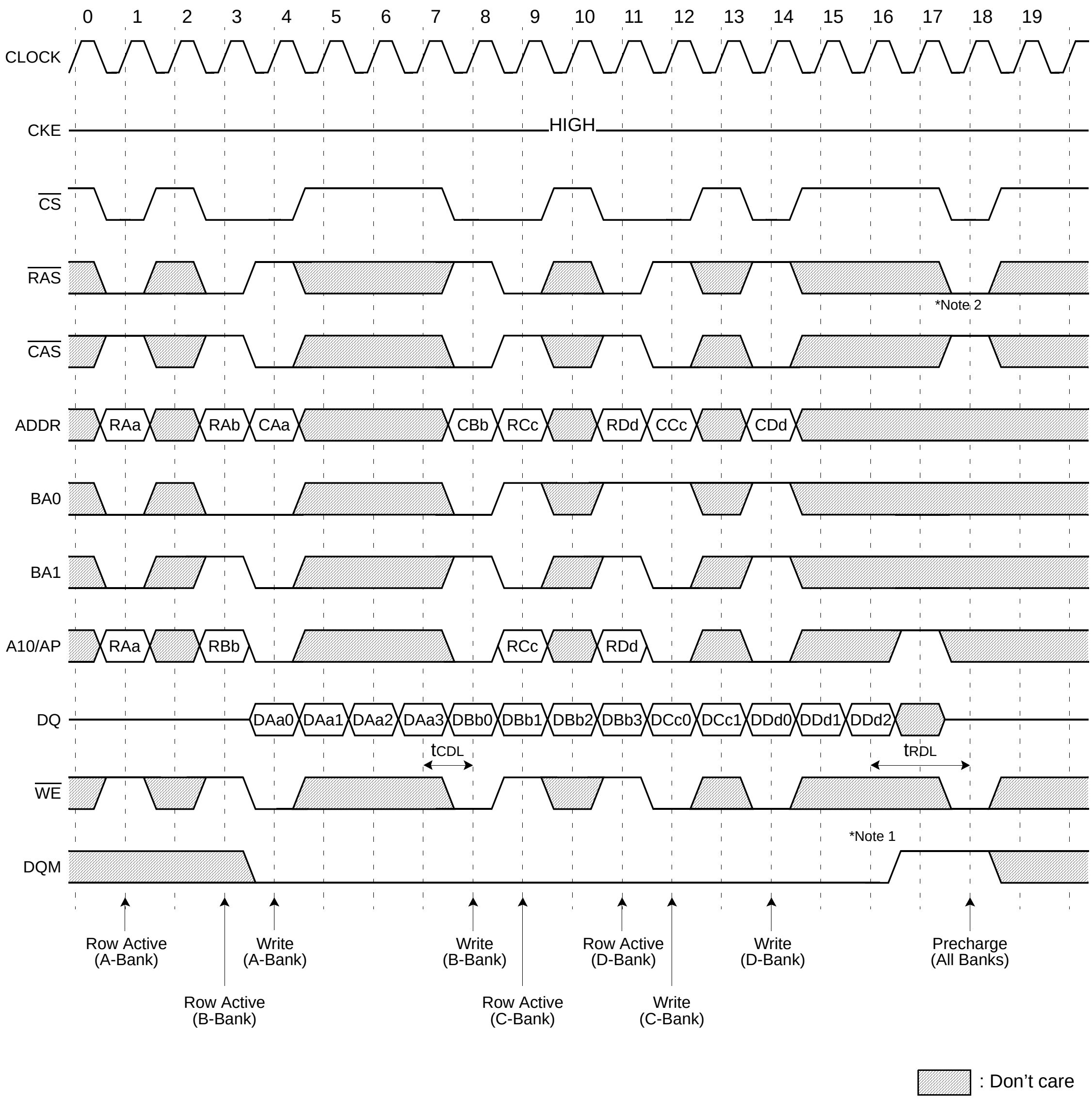
Page Read Cycle at Different Bank @Burst Length=4



***NOTE:**

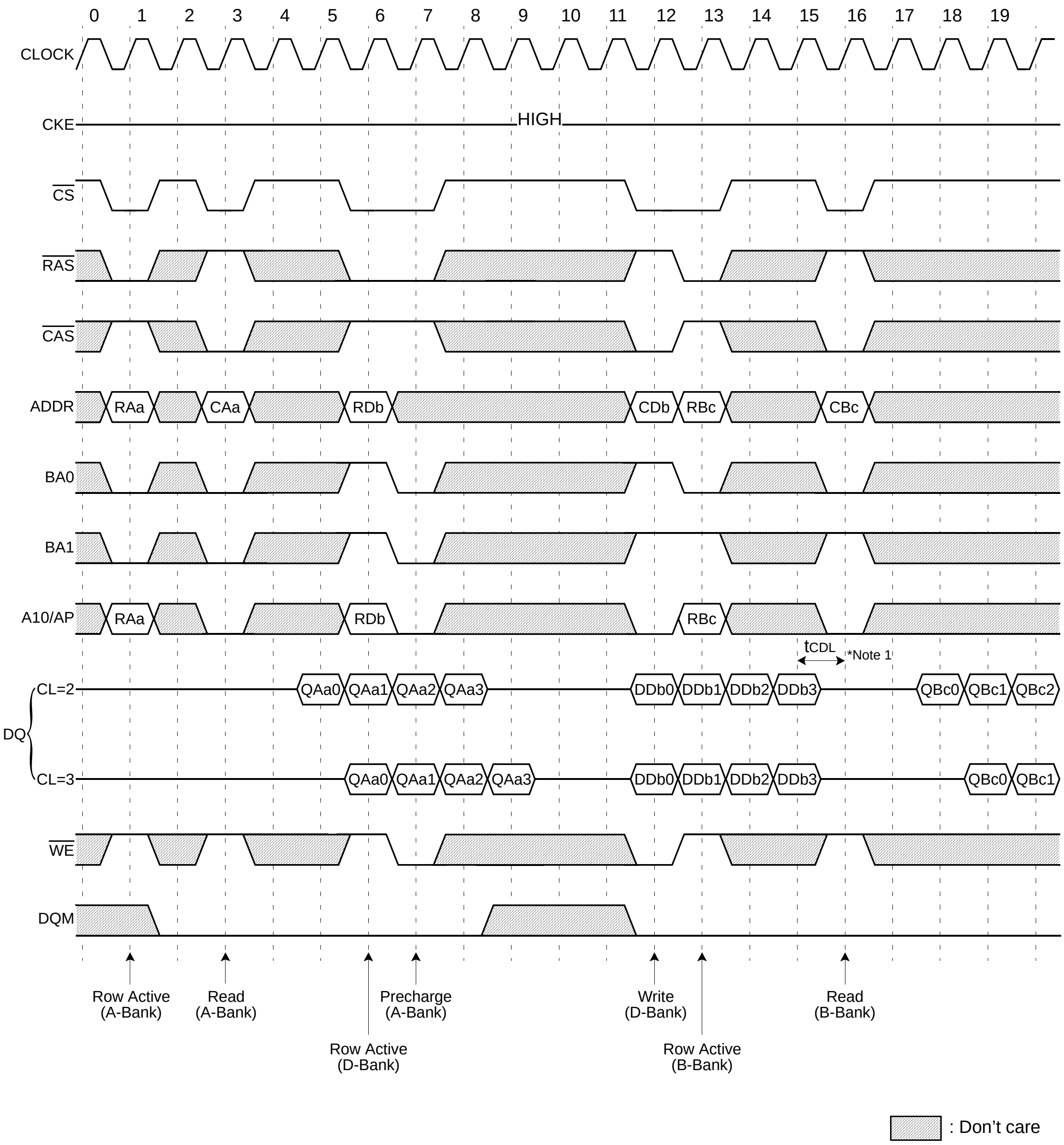
1. CS can be don't cared when RAS, CAS and WE are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK



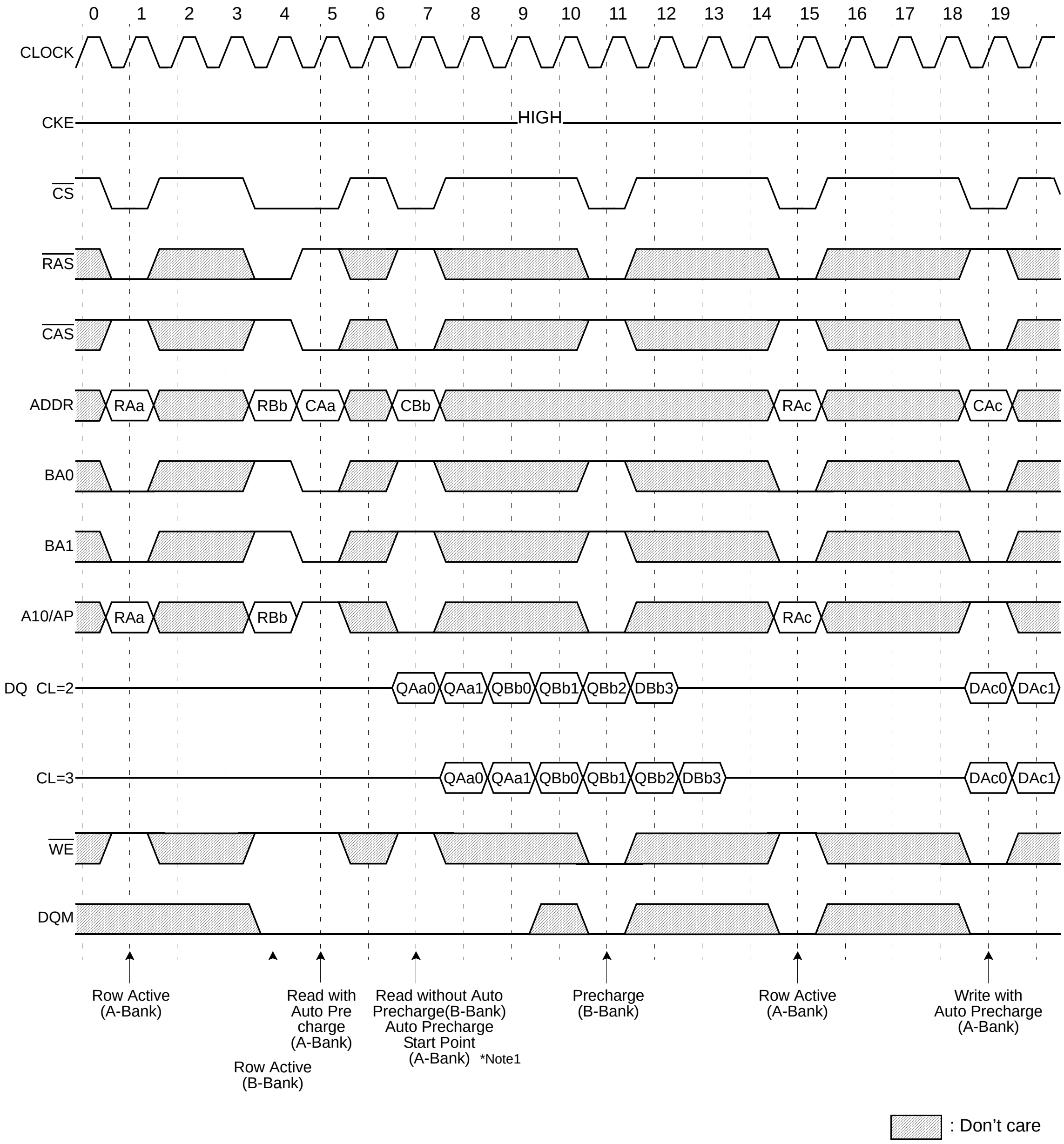
***NOTE:**
1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



***NOTE:**
1. tCDL should be met to complete write.

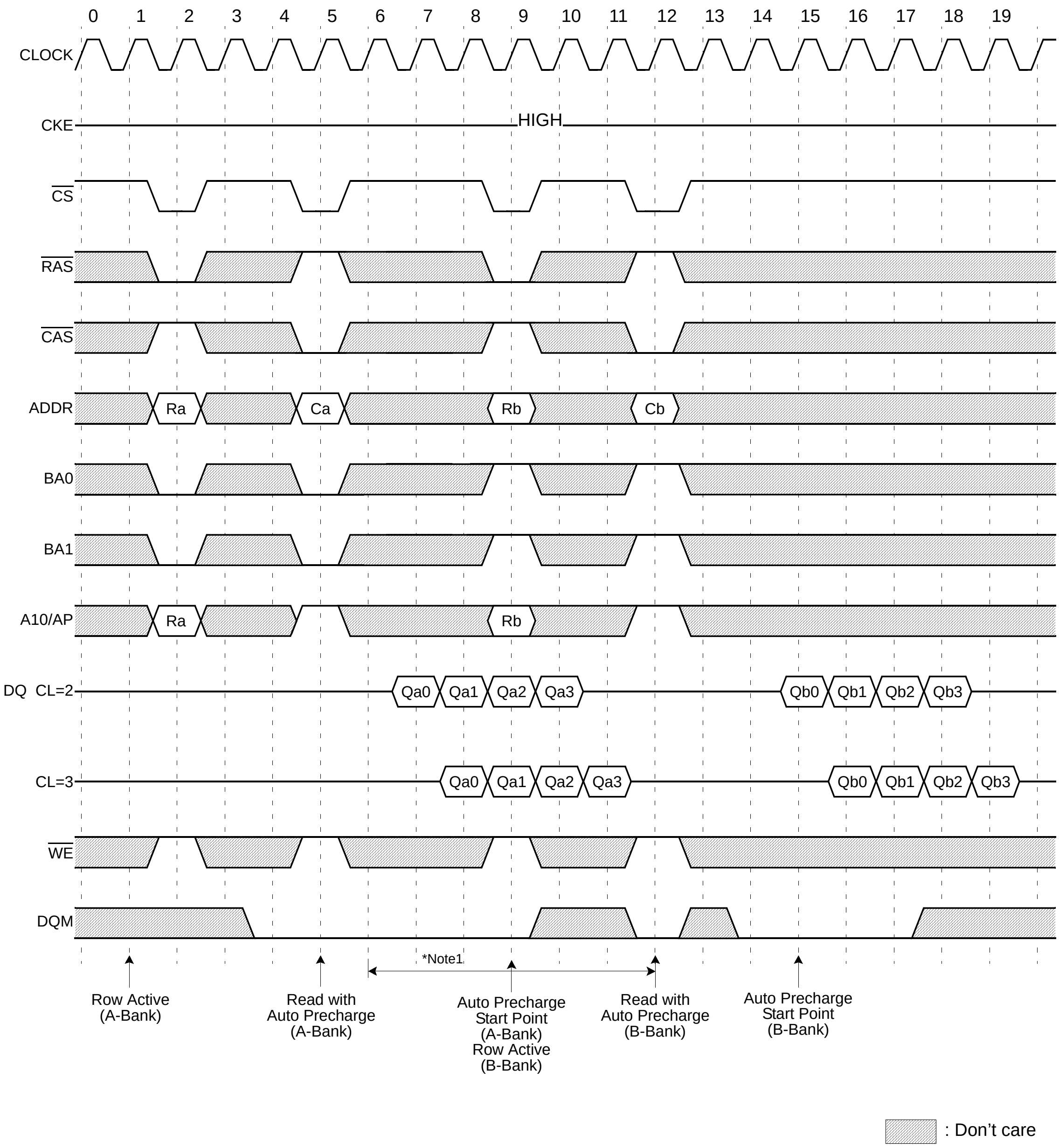
Read & Write Cycle with Auto Precharge I @Burst Length=4



***NOTE:**

1. When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
   - if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point .
   - any command can not be issued at A-Bank during tRP after A-Bank auto precharge starts.

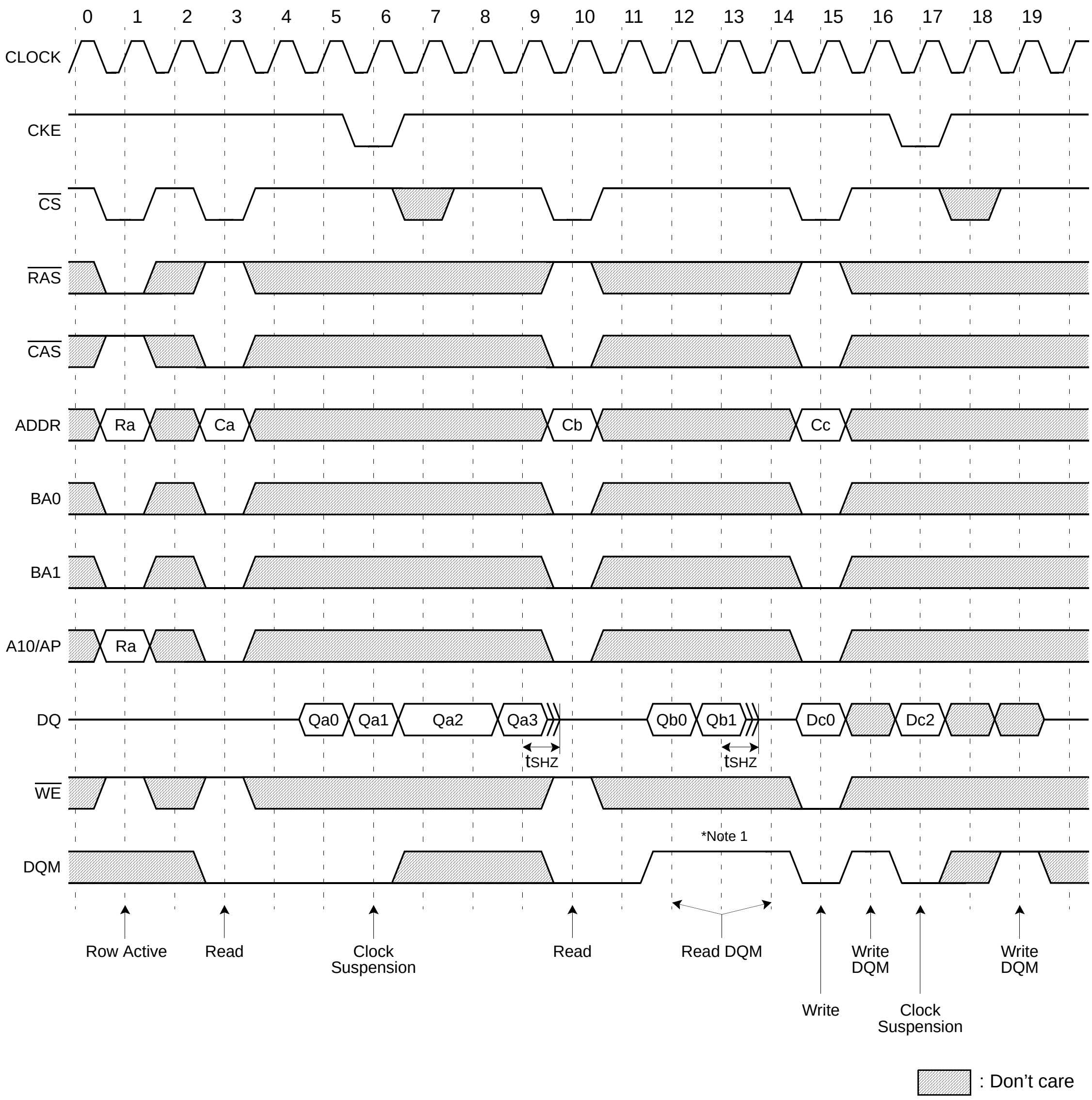
Read & Write Cycle with Auto Precharge II @Burst Length=4



***NOTE:**

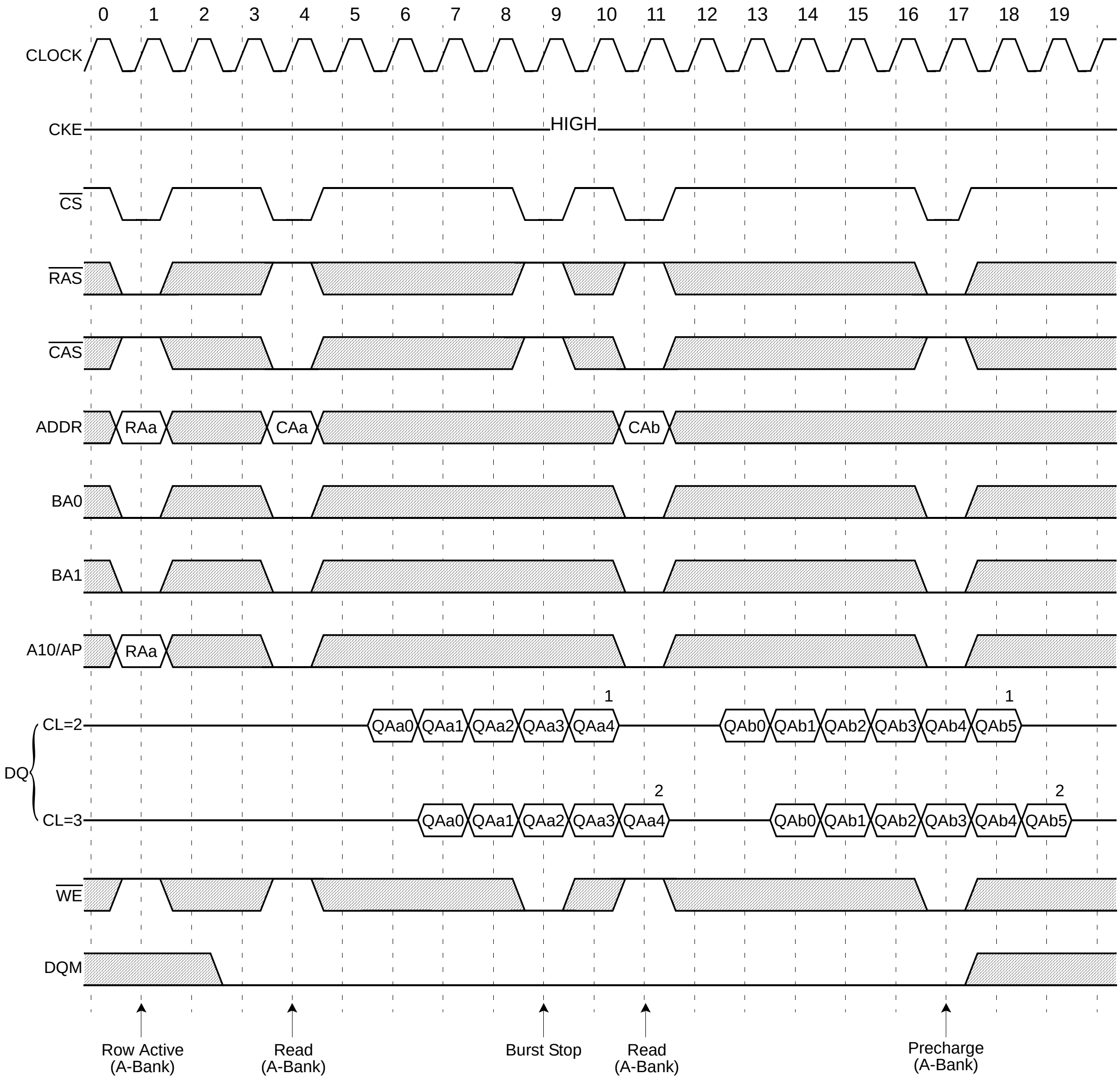
1. Any command to A-bank is not allowed in this period.
   tRP is determined from at auto precharge start point

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



***NOTE:**
1. DQM is needed to prevent bus contention.

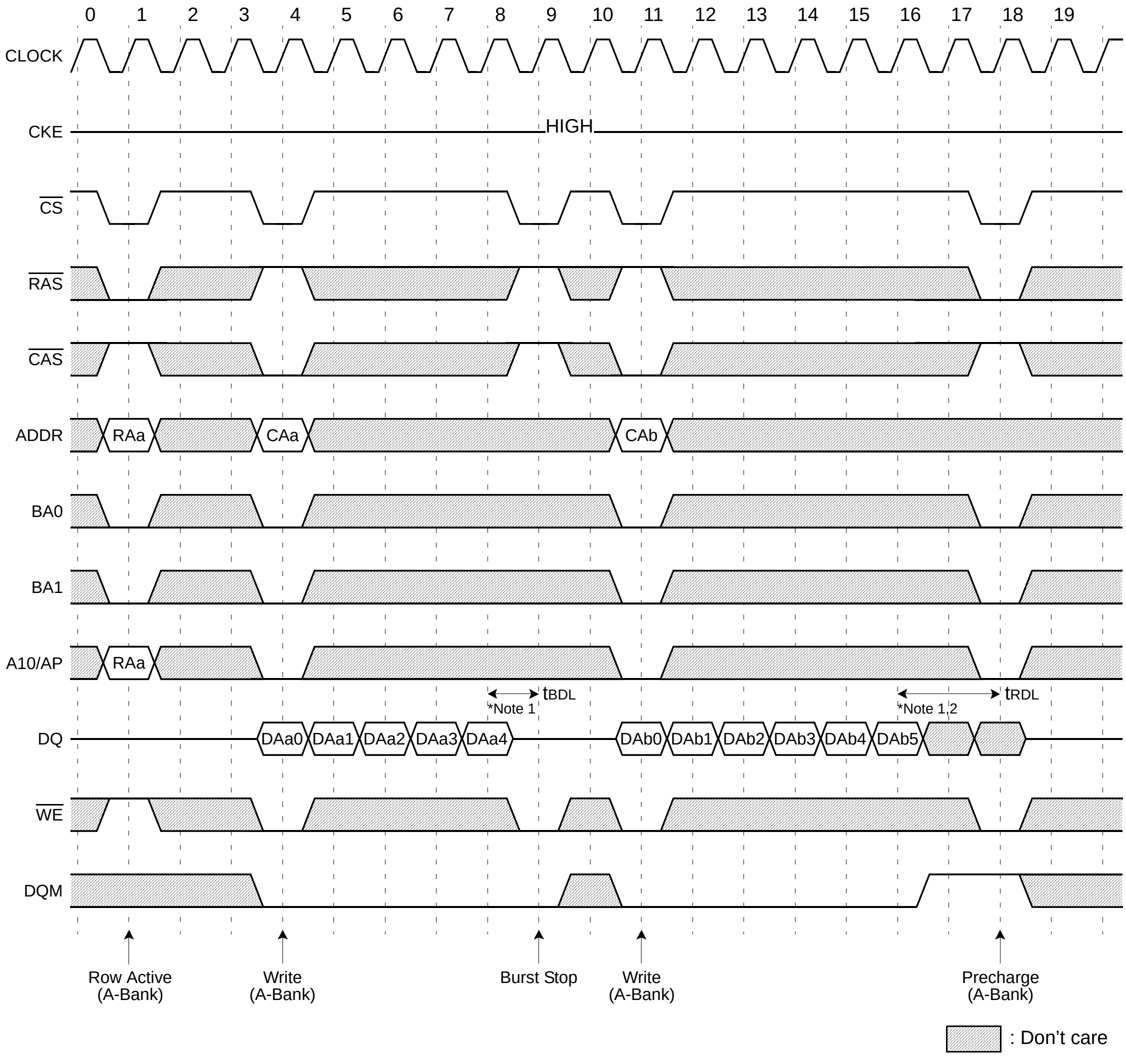
Read Interrupted by Precharge Command & Read Burst Stop Cycle @Full Page Burst



: Don't care

***NOTE:**
1. At full page mode, burst is finished by burst stop or precharge.
2. About the valid DQs after burst stop, it is same as the case of RAS interrupt.
   Both cases are illustrated above timing diagram. See the label 1, 2 on them.
   But at burst write, Burst stop and RAS interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

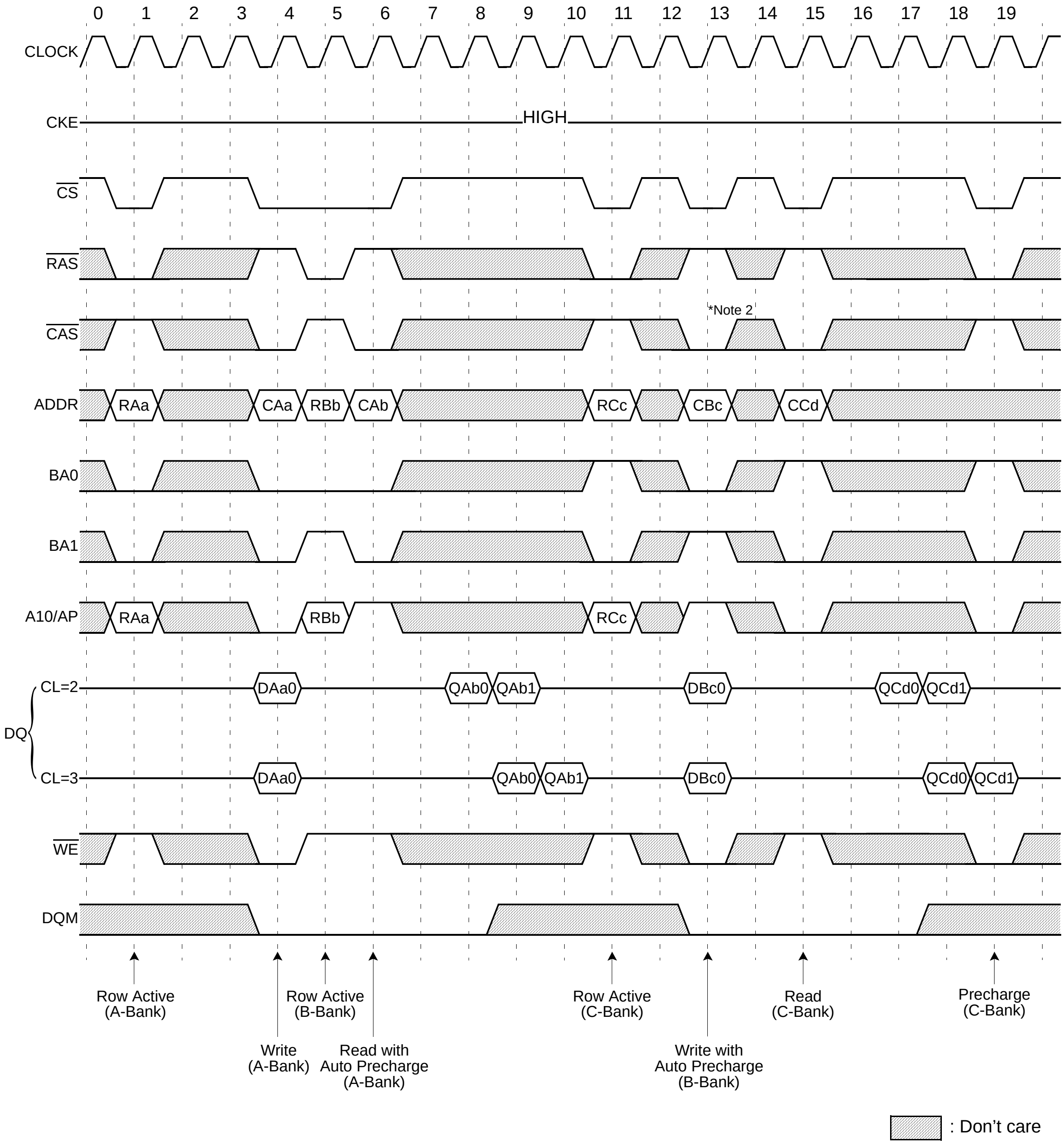
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK



***NOTE:**

1. At full page mode, burst is finished by burst stop or precharge.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of tRDL.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

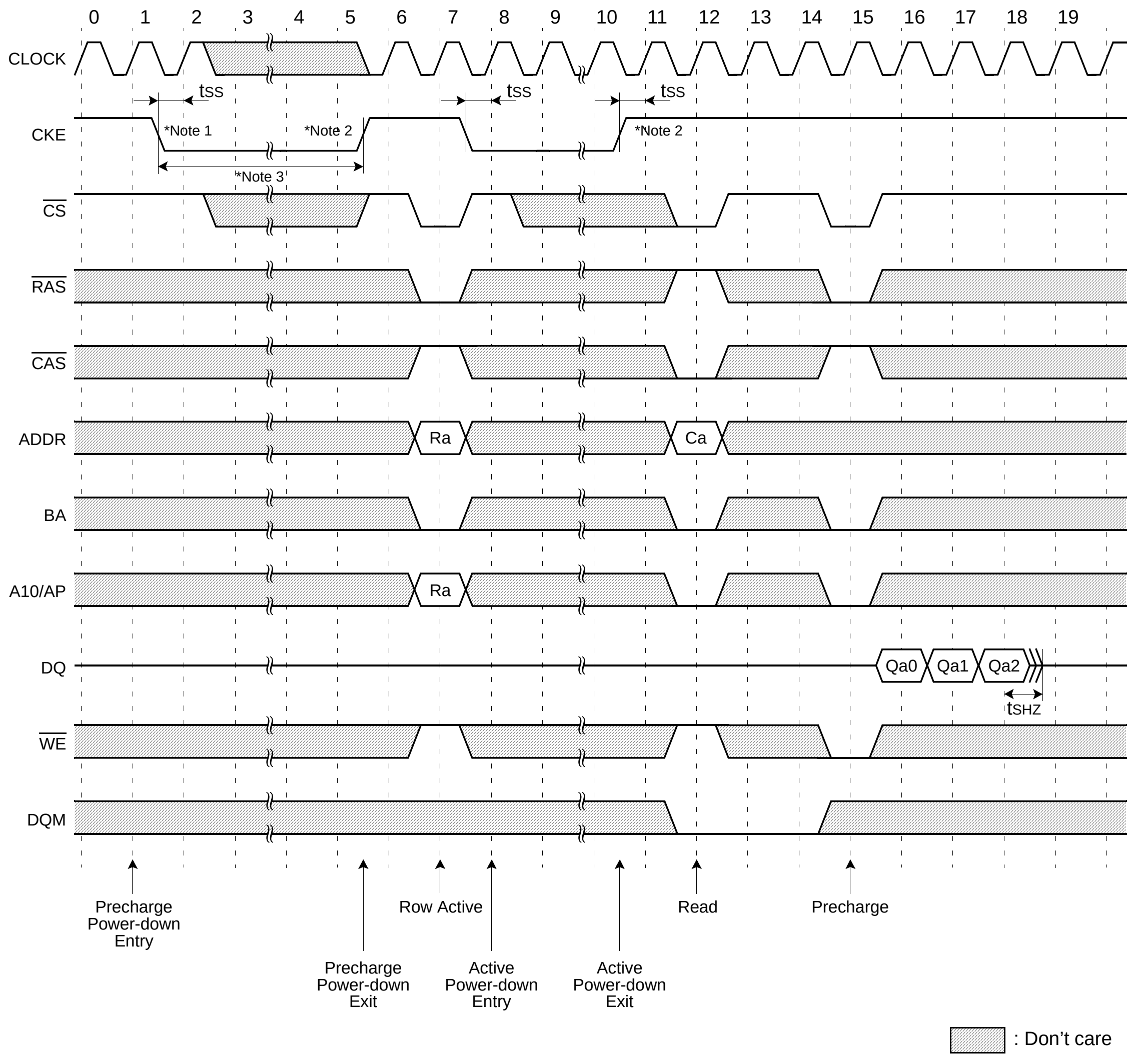
Burst Read Single bit Write Cycle @Burst Length=2



***NOTE:**

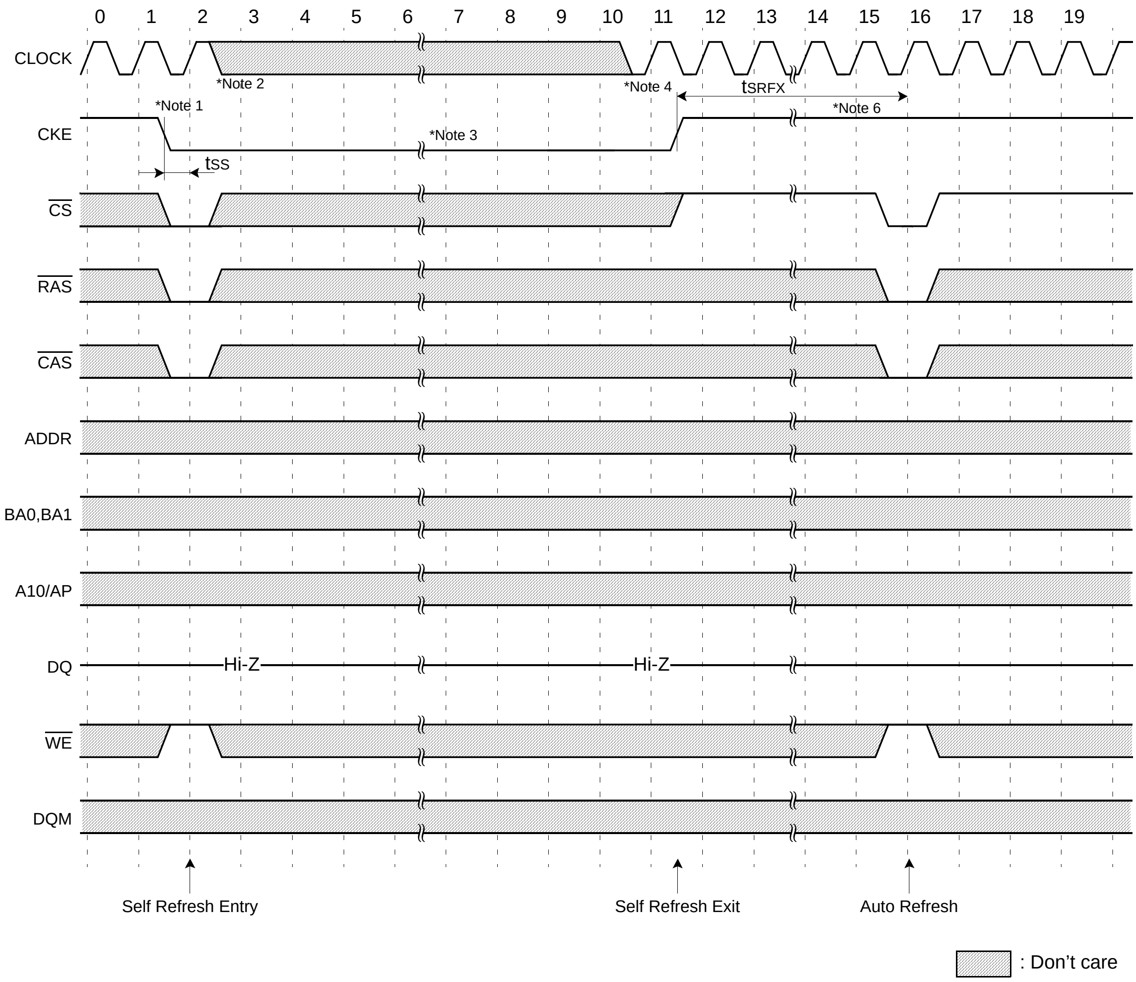
1. BRSW modes is enabled by setting A9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that tRAS should not be violated.
   Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
   the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



***NOTE:**
1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tSS prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



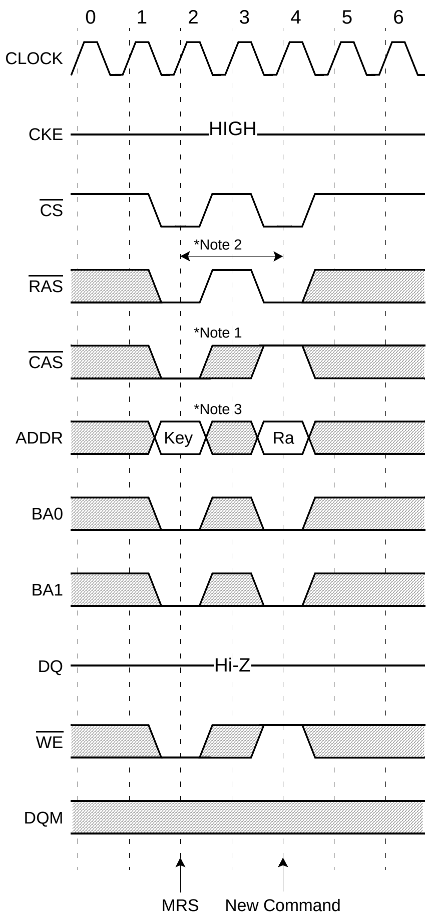
***NOTE:**
TO ENTER SELF REFRESH MODE

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum tRAS is required before exit from self refresh.

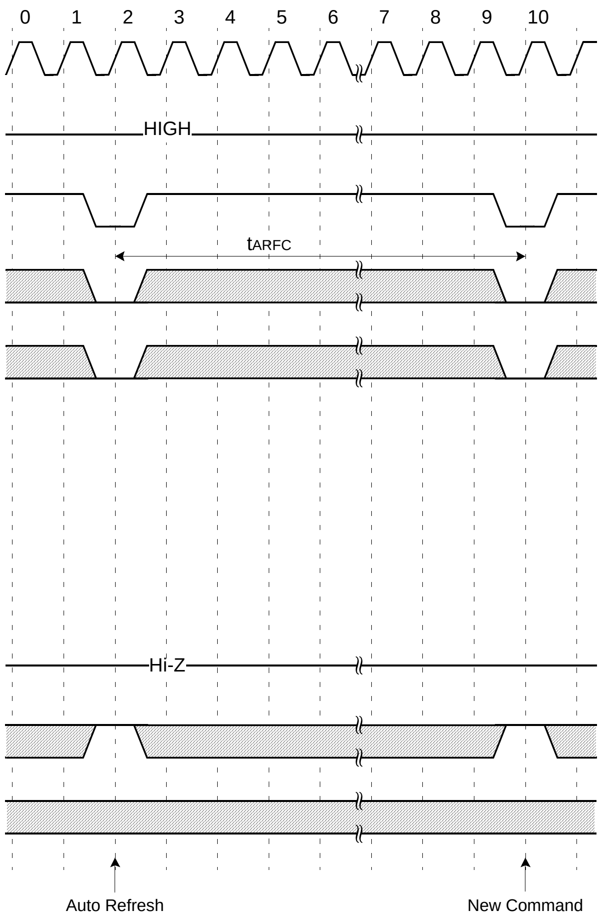
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum tSRFX is required after CKE going high to complete self refresh exit.
7. 4K cycle(64Mb ,128Mb) or 8K cycle(256Mb, 512Mb) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle

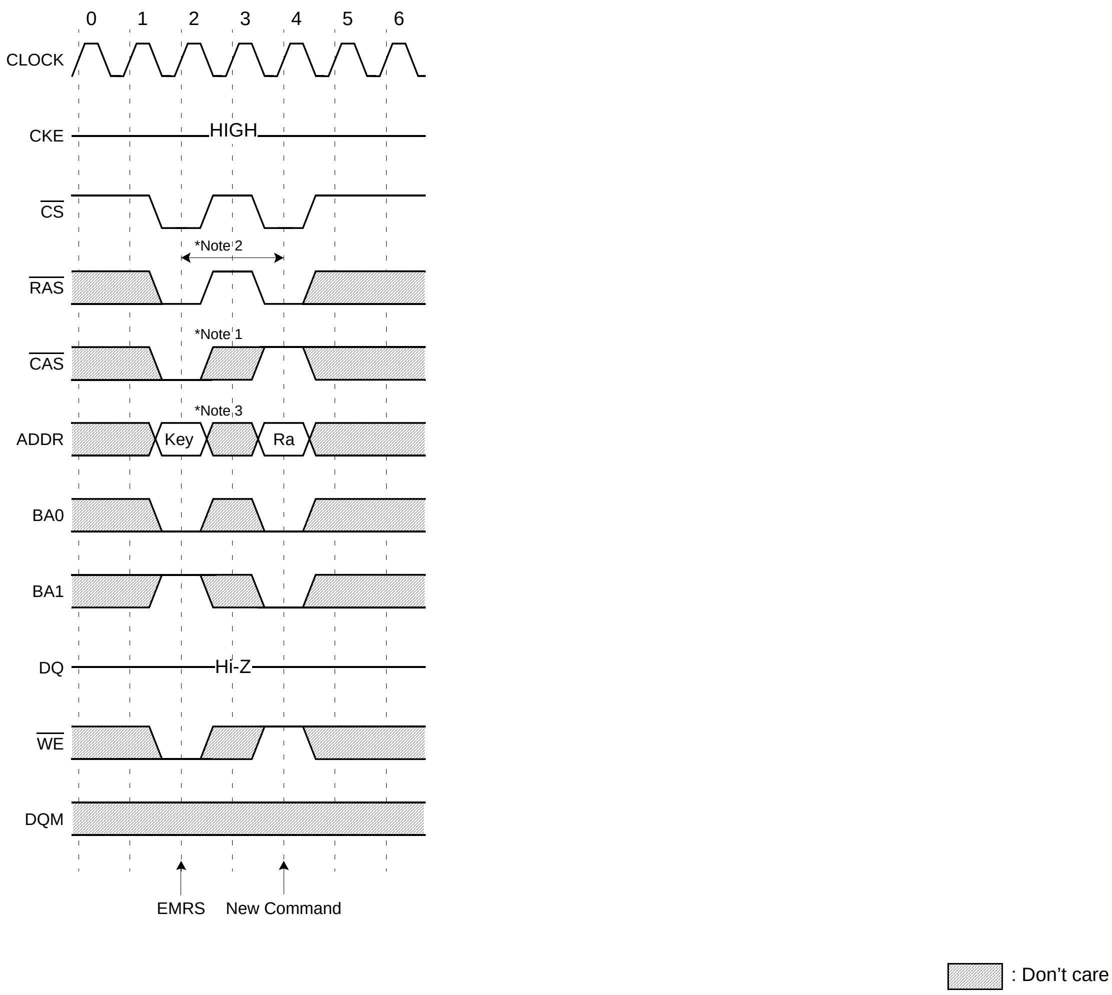


* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

: Don't care

***NOTE:**
MODE REGISTER SET CYCLE
1. CS, RAS, CAS, BA0, BA1 & WE activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new RAS activation.
3. Please refer to Mode Register Set table.

Extended Mode Register Set Cycle



***NOTE:**

EXTENDED MODE REGISTER SET CYCLE

1. CS, RAS, CAS, BA0, BA1 & WE activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new RAS activation.
3. Please refer to Mode Register Set table.

PACKAGE DIMENSION

107-Ball Fine pitch Ball Grid Array Package (measured in millimeters)