KS57C2504
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The S3C7254 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM4 (Samsung Arrangeable Microcontrollers).With a two-channel comparator, up-to-320-dot LCD direct drive capability, 8-bit timer/counter, and serial I/O, the S3C7254 offers an excellent design solution for a wide variety of applications which require LCD functions.

Up to 27 pins of the 80-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the S3C7254's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

FEATURES

Memory

- 512 × 4-bit RAM
- 4096 × 8-bit ROM

27 I/O Pins

- I/O: 15 pins
- Input only: 4 pins
- Output only: 8 pins

Comparator

- Two-channel mode: internal reference (4-bit resolution)
- One-channel mode: external reference

LCD Controller/Driver

- 40 segments and 8 common terminals
- 3, 4 and 8 common selectable
- Internal resistor circuit for LCD bias
- All dot can be switched on/off

8-Bit Basic Timer

- 4 interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Serial I/O interface clock generator

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Interrupts

- Three internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 80-pin QFP

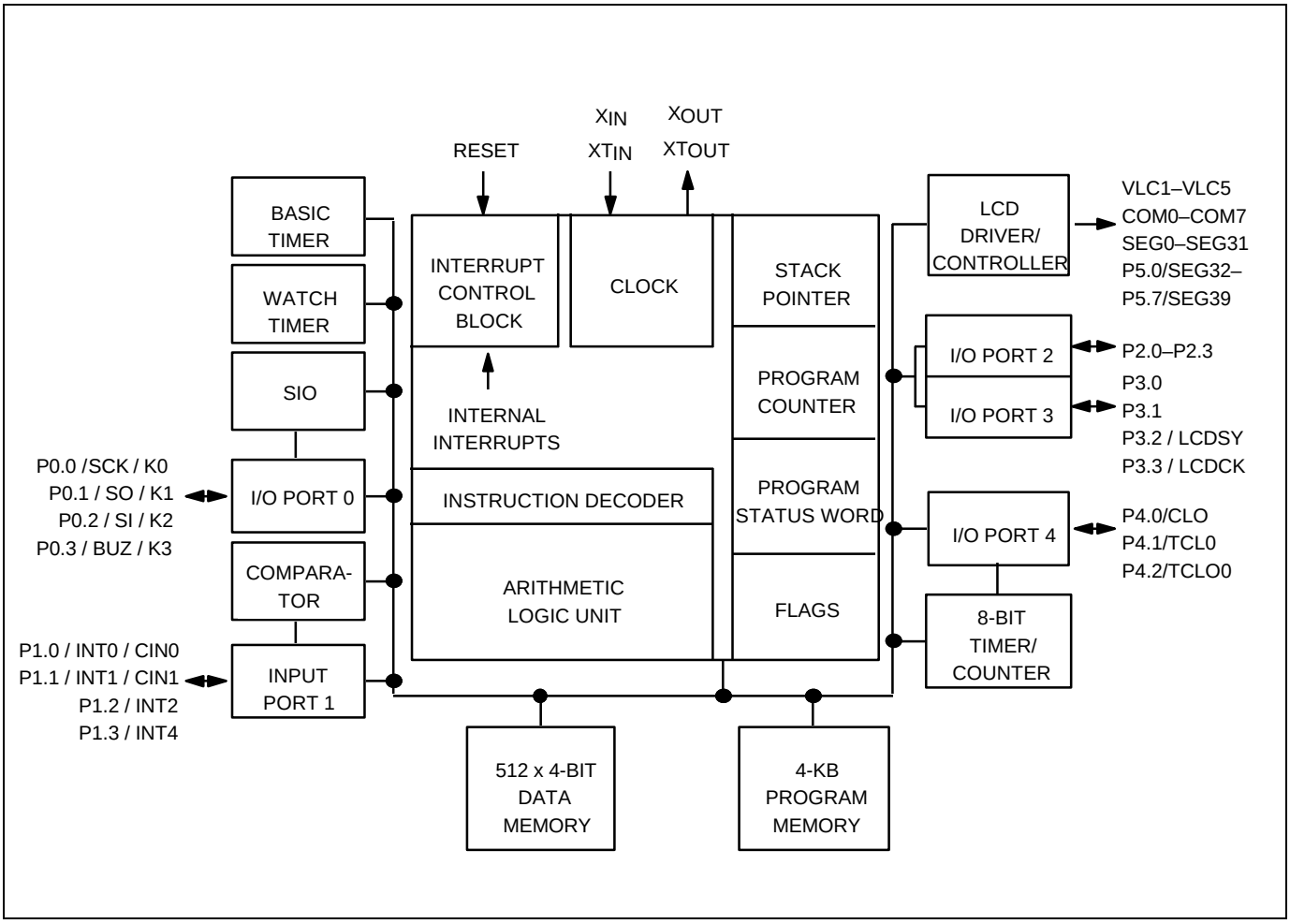


Figure 1. S3C7254 Simplified Block Diagram

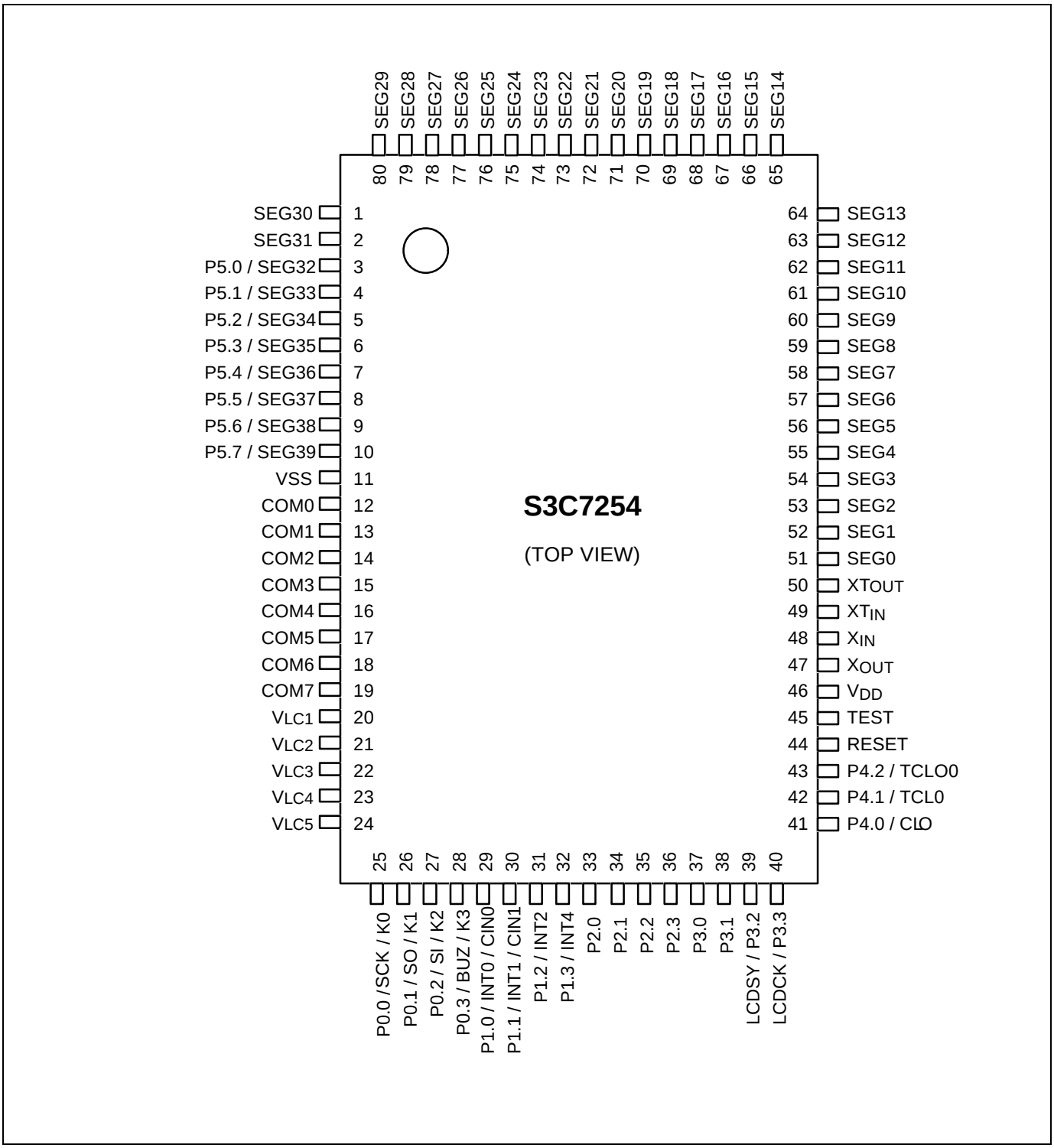


Figure 2. S3C7254 80–Pin QFP Assignment Diagram

Table 1. S3C7254 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	25 26 27 28	K0/SCK K1/SO K2/SI K3/BUZ
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test are possible. The 1-bit unit pull-up resistors are assigned to input pins by software. An interrupt is generated by digital input at P1.0, P1.1.	29 30 31 32	INT0/CIN0 INT1/CIN1 INT2 INT4
P2.0–P2.3	I/O	Same as port 0 except that 8-bit read/write and test is possible.	33–36	–
P3.0 P3.1 P3.2 P3.3			37 38 39 40	– – LCDSY LCDCK
P4.0 P4.1 P4.2	I/O	Same as port 0 except that port 4 is 3-bit I/O port.	41 42 43	CLO TCL0 TCLO0
P5.0–P5.7	O	Output port for 1-bit data	3–10	SEG32– SEG39
SCK	I/O	Serial I/O interface clock signal	25	P0.0/K0
SO	I/O	Serial data output	26	P0.1/K1
SI	I/O	Serial data input	27	P0.2/K2
BUZ	I/O	2 KHz, 4 KHz, 8 KHz or 16 KHz frequency output for buzzer sound	28	P0.3/K3
K0–K3	I/O	External interrupt. The triggering edge is selectable.	25–28	P0.0–P0.3
INT0 INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	29 30	P1.0/CIN0 P1.1/CIN1
INT2	I	Quasi-interrupt with detection of rising or falling edges	31	P1.2
INT4	I	External interrupts with detection of rising and falling edges	32	P1.3

Table 1. S3C7254 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
CIN0 CIN1	I	2-channel comparator input. CIN0: comparator input or external reference input CIN1: comparator input only.	29 30	P1.0/INT0 P1.1/INT1
LCDSY	I/O	LCD synchronization clock output for display expansion	39	P3.2
LCDCK	I/O	LCD clock output for display expansion	40	P3.3
CLO	I/O	Clock output	41	P4.0
TCL0	I/O	External clock input for timer/counter 0	42	P4.1
TCLO0	I/O	Timer/counter 0 clock output	43	P4.2
SEG32–SEG39	O	LCD segment signal output	3–10	P5.0–P5.7
SEG0–SEG29 SEG30–SEG31	O	LCD segment signal output	51–80 1–2	–
COM0–COM7	O	LCD common signal output	12–19	–
V_{LC1}–V_{LC5}	–	LCD power supply. Voltage dividing resistors are assignable by mask option.	20–24	–
X_{IN}, X_{OUT}	–	Crystal, ceramic or RC oscillator pins for system clock.	48, 47	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock.	49, 50	–
V_{DD}	–	Main power supply	46	–
V_{SS}	–	Ground	11	–
RESET	I	Chip reset signal input	44	–
TEST	I	Chip test signal input (must be connected to V_{SS})	45	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

Table 2. S3C7254 Pin Descriptions

Pin Name	Pin Type	Share Pin	Circuit Type	Reset Value
P0.0–P0.3	I/O	SCK/K0, SO/K1, SI/K2, BUZ/K3	6	Input
P1.0–P1.1	I	INT0/CIN0, INT1/CIN1	10	Comparator
P1.2–P1.3	I	INT2, INT4	3	Input
P2.0–P2.3	I/O	–	5	Input
P3.0–P3.1	I/O	–	5	Input
P3.2–P3.3	I/O	LCDSY, LCDCK	5	Input
P4.0, P4.2	I/O	CLO, TCLO0	5	Input
P4.1	I/O	TCL0	6	Input
P5.0–P5.7	O	SEG32–SEG39	7	High
COM0–COM7	O	–	8	High
SEG0–SEG31	O	–	8	High
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
RESET	I	–	2	–
VLC1–VLC5	–	–	–	–
X_{IN}, X_{OUT}	–	–	–	–
XT_{IN}, XT_{OUT}	–	–	–	–
TEST	I	–	–	–

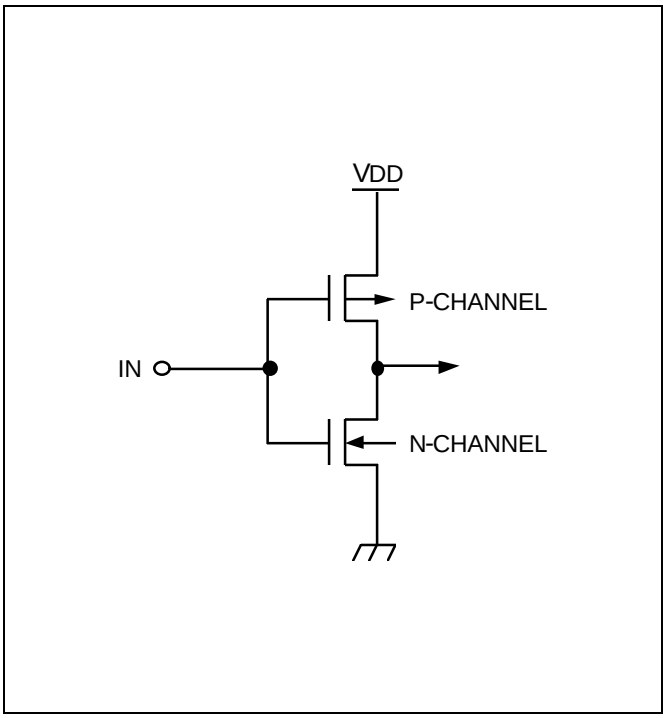


Figure 3. Pin Circuit Type 1

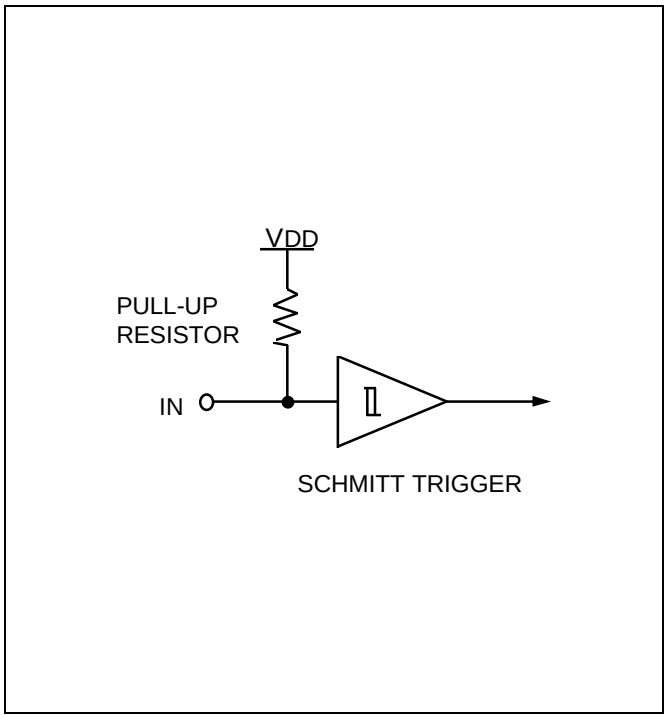


Figure 4. Pin Circuit Type 2

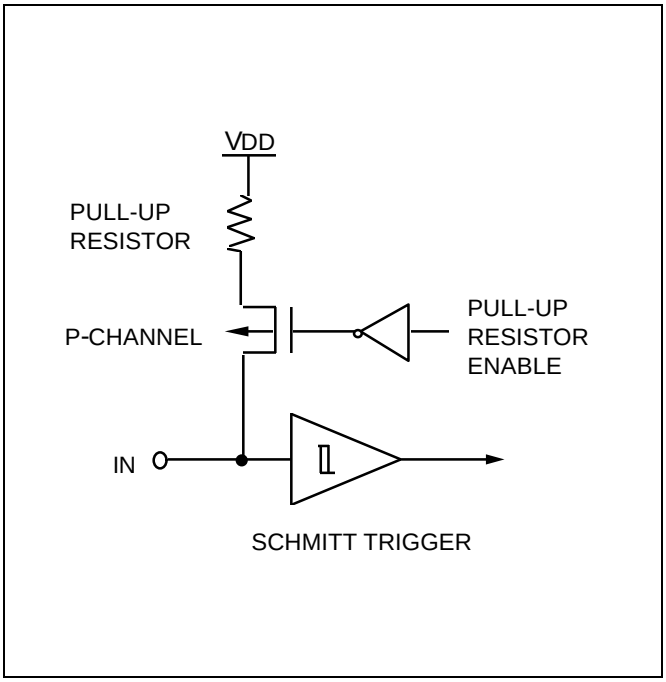


Figure 5. Pin Circuit Type 3

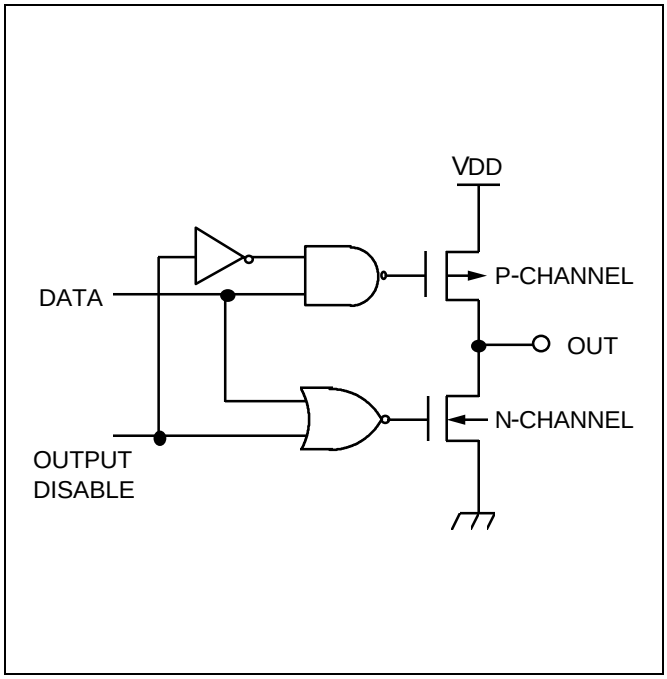


Figure 6. Pin Circuit Type 4

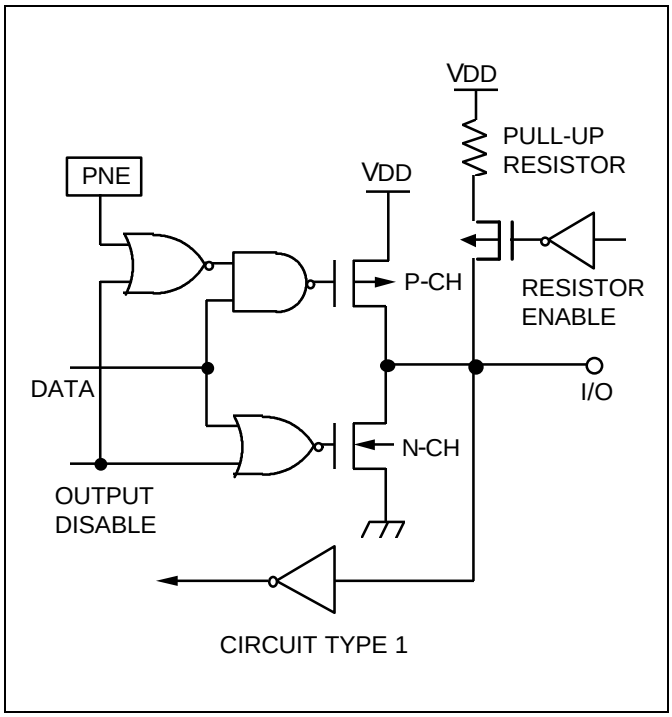


Figure 7. Pin Circuit Type 5

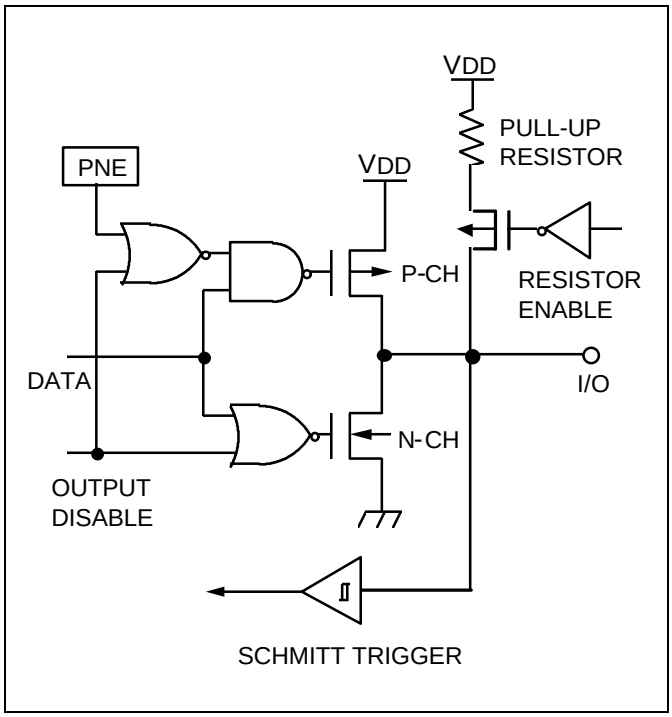


Figure 8. Pin Circuit Type 6

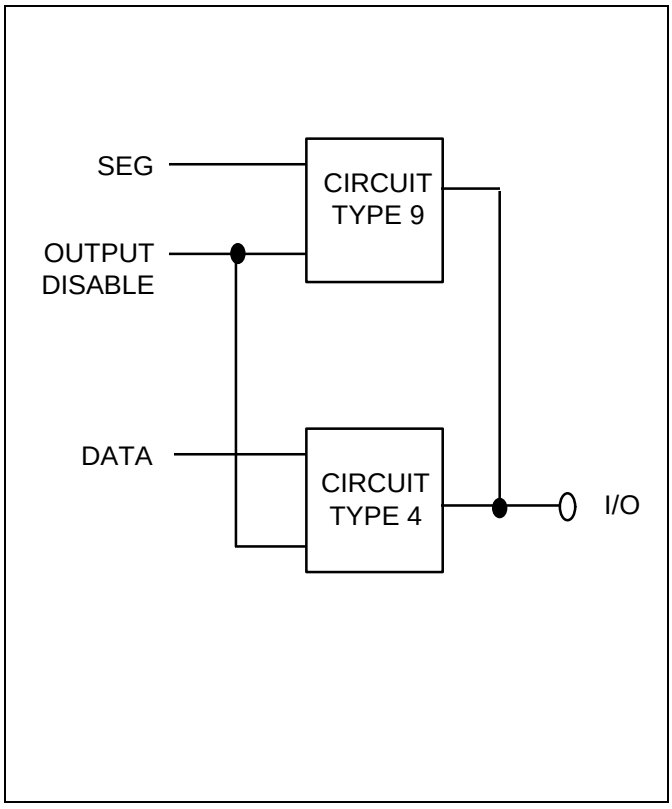


Figure 9. Pin Circuit Type 7

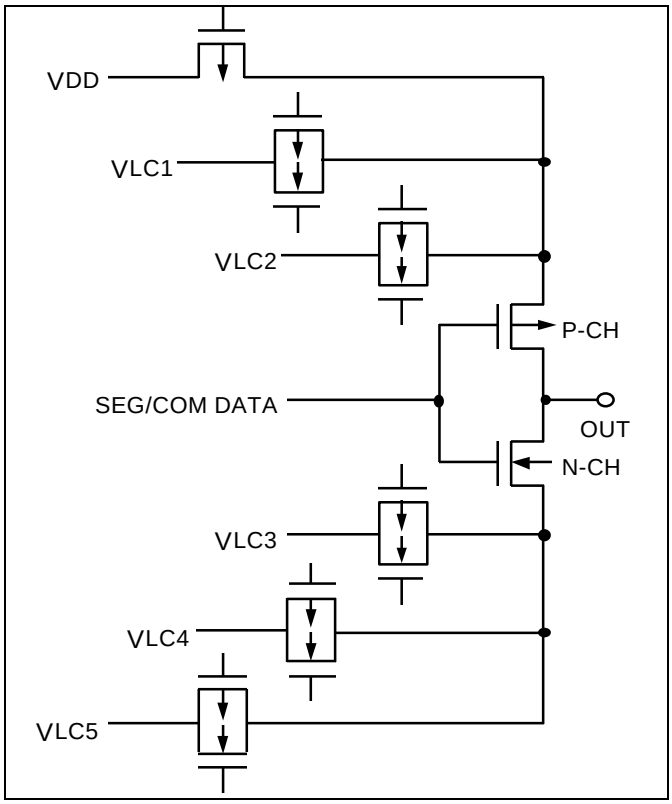


Figure 10. Pin Circuit Type 8

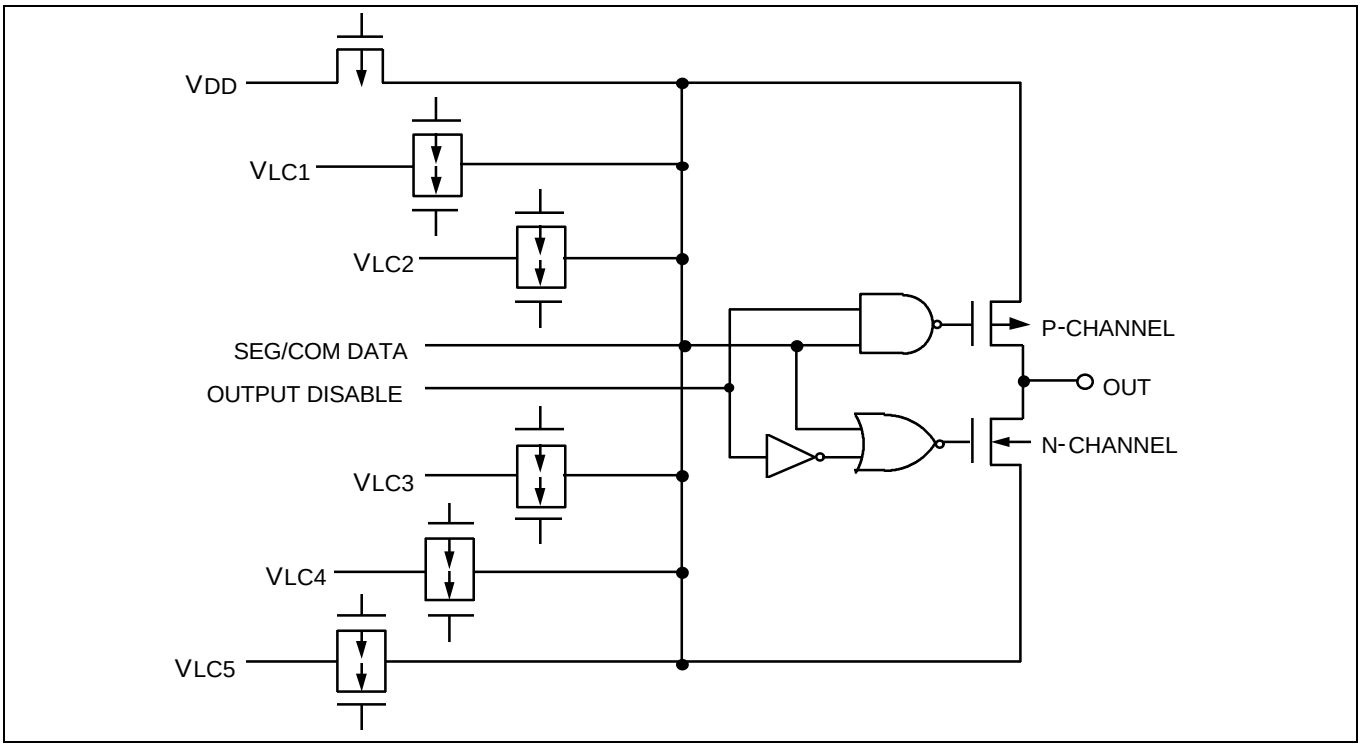


Figure 11. Pin Circuit Type 9

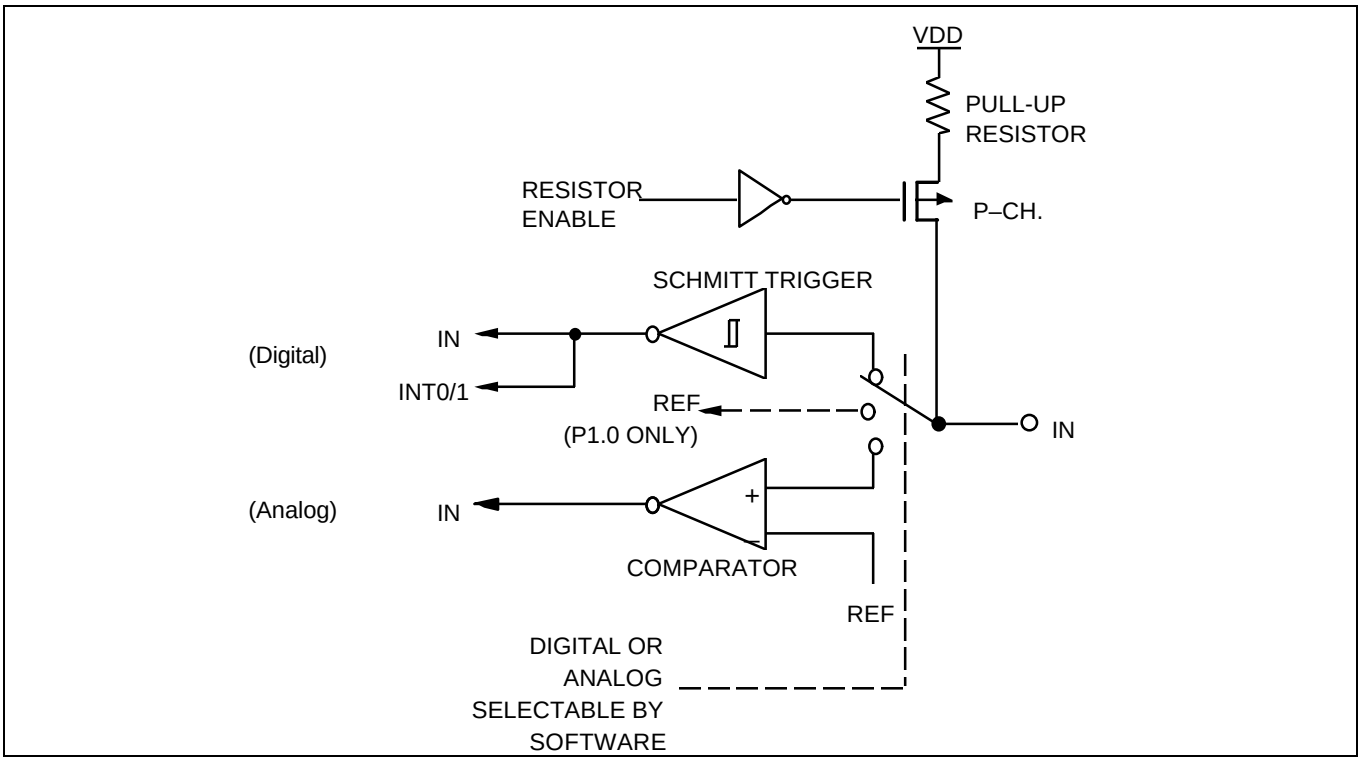


Figure 12. Pin Circuit Type 10

PROGRAM MEMORY (ROM)

ROM maps for S3C7254 devices are mask programmable at the factory. In its standard configuration, the device's 4,096 × 8-bit program memory has three areas that are directly addressable by the program counter (PC):

- 16-byte area for vector addresses
- 96-byte instruction reference area
- 16-byte general-purpose area
- 3,968-byte general-purpose area

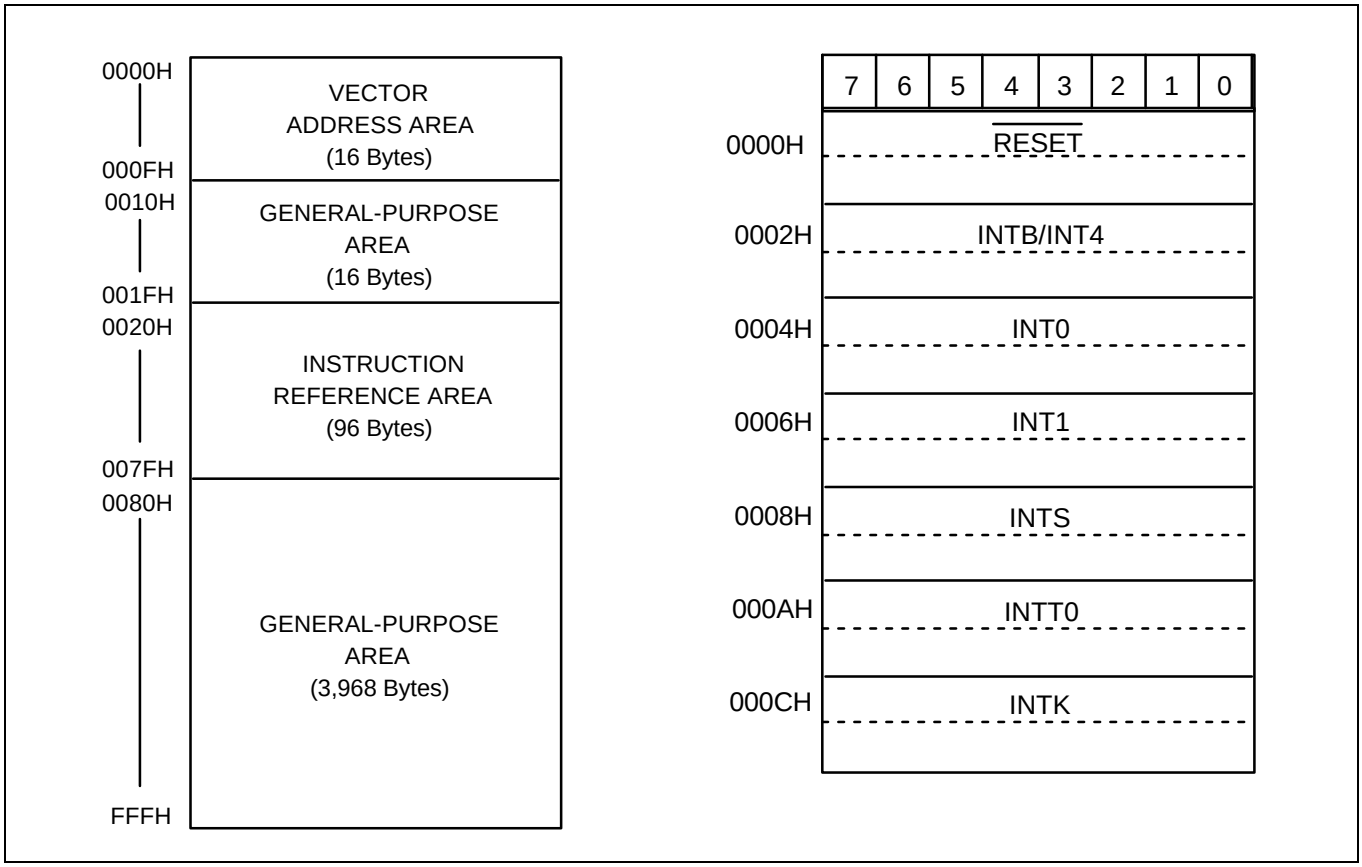


Figure 13. ROM Address Structure

DATA MEMORY (RAM)

In its standard configuration, the 512 x 4-bit data memory has five areas:

- 32 × 4-bit working register area in bank 0
- 224 × 4-bit general-purpose area in bank 0 which is also used as the stack area
- 176 × 4-bit general-purpose area in bank 1
- 80 × 4-bit area for LCD data in bank 1
- 128 × 4-bit area in bank 15 for memory-mapped I/O addresses

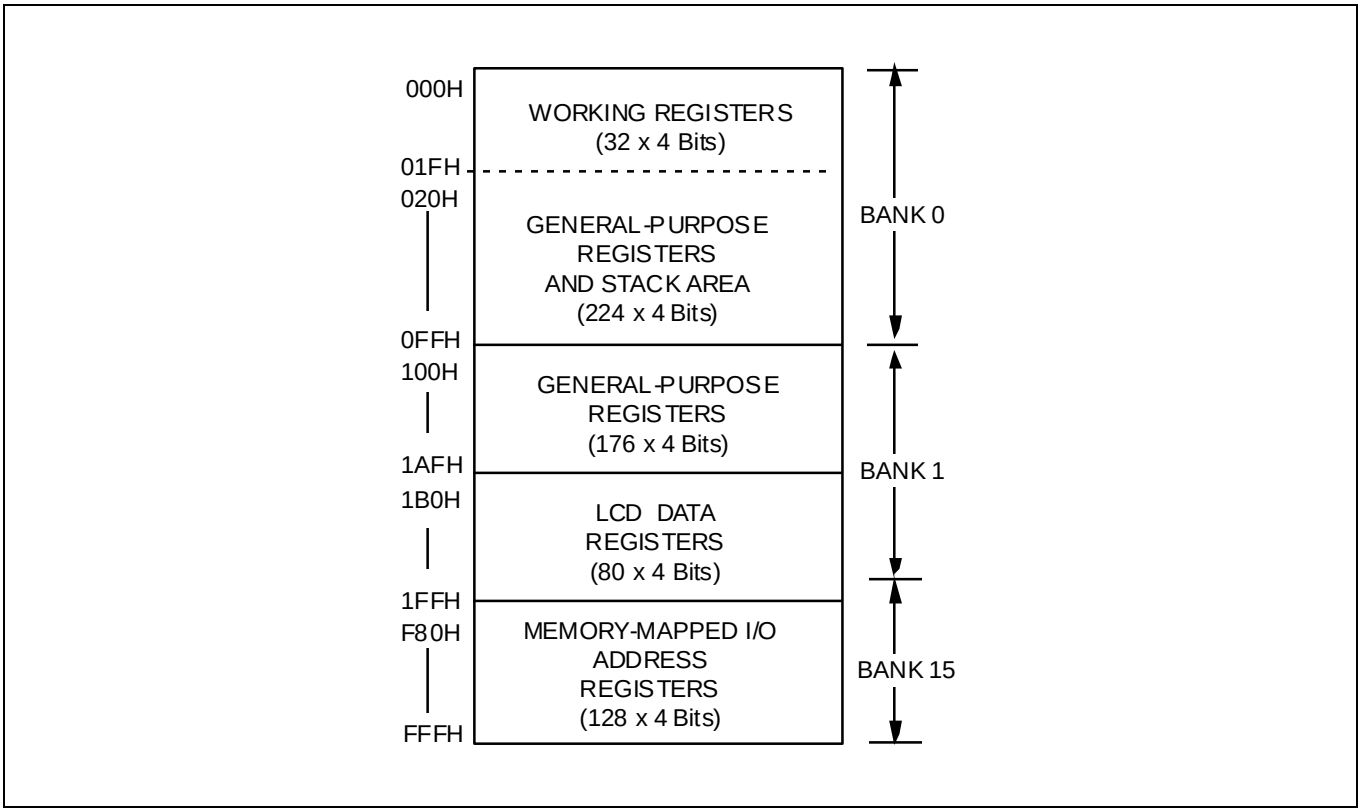
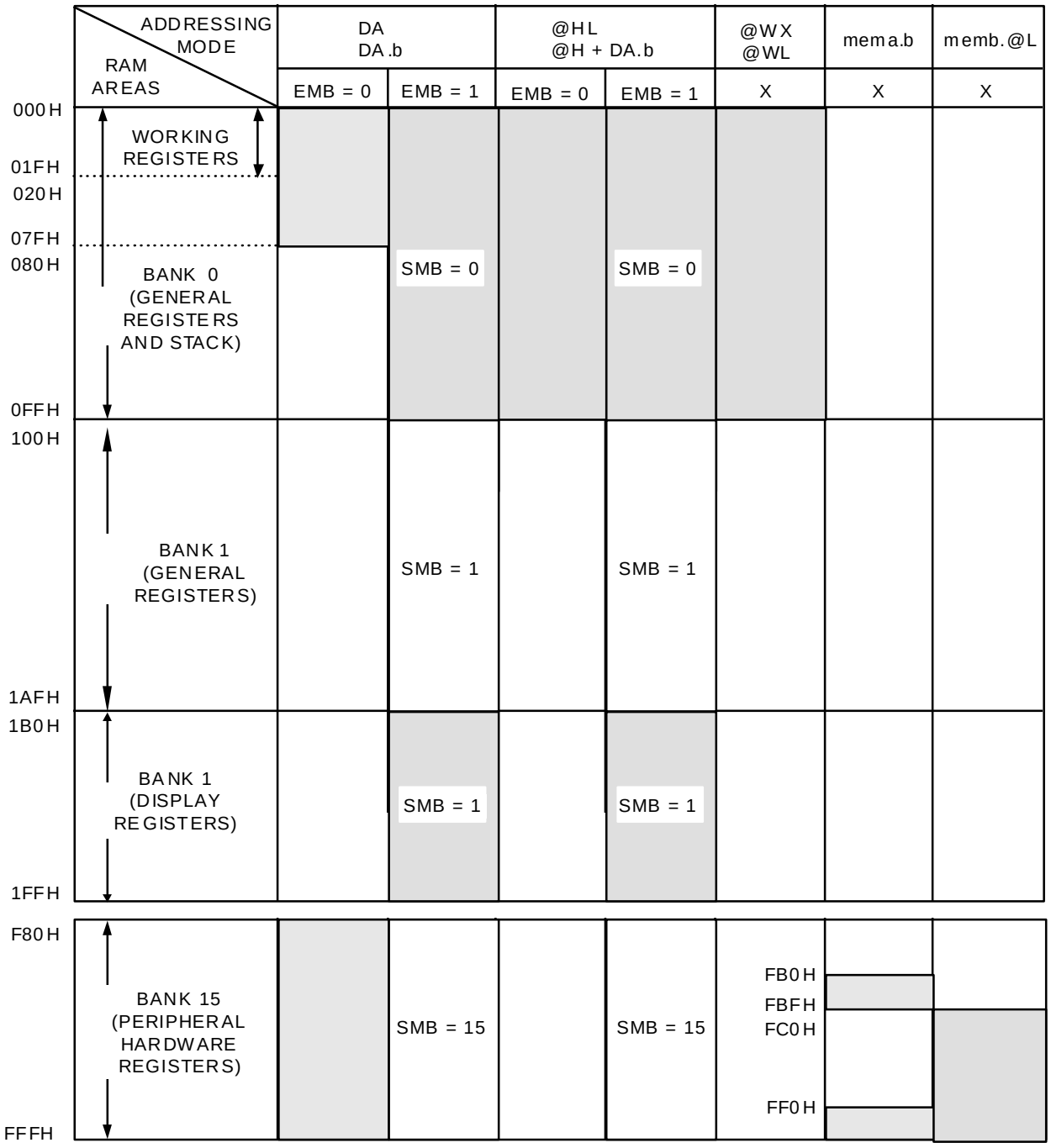


Figure 14. Data Memory (RAM) Map

ADDRESSING MODES



NOTES: 1. 'X' means don't care.
2. Blank columns indicate RAM areas that are not addressable, given the addressing method and enable memory bank (EMB) flag setting shown in the column headers.

Figure 15. RAM Address Structure

Table 3. I/O Map for Memory Bank 15

Memory Bank 15							Addressing Mode		
Address	**Register**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
F80H	SP	.3	.2	.1	"0"	R/W	No	No	Yes
F81H		.7	.6	.5	.4				
•									
•									
•									
F85H	BMOD	.3	.2	.1	.0	W	.3	Yes	No
F86H	BCNT					R	No	No	Yes
F87H									
F88H	WMOD	.3	.2	.1	.0	W	.3 (1)	No	Yes
F89H		.7	"0"	.5	.4				
F8AH									
F8BH									
F8CH	LMOD	.3	.2	.1	.0	W	No	No	Yes
F8DH		.7	.6	.5	.4				
F8EH	LCON	.3	.2	"1"	.0	W	No	Yes	No
F8FH									
F90H	TMOD0	.3	.2	"0"	"0"	W	.3	No	Yes
F91H		"0"	.6	.5	.4				
F92H		"0"	TOE0	"0"	"0"	R/W	Yes	Yes	No
F93H									
F94H	TCNT0					R	No	No	Yes
F95H									
F96H	TREF0					W	No	No	Yes
F97H									
•									
•									
•									
FA6H	PNE1	.3	.2	.1	.0	W	No	Yes	No
FA7H									

Table 3. I/O Map for Memory Bank 15 (Continued)

Memory Bank 15							Addressing Mode		
Address	**Register**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
FA8H	PNE2	.3	.2	.1	.0	W	No	No	Yes
FA9H		.7	.6	.5	.4				
FAAH	PNE3	"0"	.2	.1	.0			Yes	No
•									
•									
•									
FB0H	PSW	IS1	IS0	EMB	ERB	R/W	Yes	Yes	Yes
FB1H		C (2)	SC2	SC1	SC0	R	No	No	
FB2H	IPR	IME	.2	.1	.0	W	IME	Yes	No
FB3H	PCON	.3	.2	.1	.0	W	No	Yes	No
FB4H	IMOD0	.3	"0"	.1	.0	W	No	Yes	No
FB5H	IMOD1	"0"	"0"	"0"	.0	W	No	Yes	No
FB6H	IMODK	"0"	.2	.1	.0	W	No	Yes	No
FB7H	SCMOD	.3	"0"	"0"	.0	W	Yes	No	No
FB8H		IE4	IRQ4	IEB	IRQB	R/W	Yes	Yes	No
FB9H									
FBAH		"0"	"0"	IEW	IRQW	R/W	Yes	Yes	No
FBBH		"0"	"0"	IEK	IRQK				
FBCH		"0"	"0"	IET0	IRQT0				
FBDH		"0"	"0"	IES	IRQS				
FBEH		IE1	IRQ1	IE0	IRQ0				
FBFH		"0"	"0"	IE2	IRQ2				
FC0H	BSC0					R/W	Yes	Yes	Yes
FC1H	BSC1								
FC2H	BSC2								Yes
FC3H	BSC3								
•									
•									
•									

Table 3. I/O Map for Memory Bank 15 (Continued)

Memory Bank 15							Addressing Mode		
Address	**Register**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
FD0H	CLMOD	.3	"0"	.1	.0	W	No	Yes	No
FD1H									
FD2H									
FD3H									
FD4H	CMPREG	.3	.2	.1	.0	R	No	Yes	No
FD5H									
FD6H	CMOD	.3	.2	.1	.0	R/W	No	No	Yes
FD7H		.7	.6	.5	"0"				
FD8H									
FD9H									
FDAH	IMOD2	"0"	"0"	"0"	.0	W	No	Yes	No
FDBH									
FDCH	PUMOD1	.3	.2	"0"	.0	W	No	No	Yes
FDDH		"0"	"0"	"0"	.4				
FDEH	PUMOD2	.3	.2	.1	.0	W	No	Yes	No
FDFH									
FE0H	SMOD	.3	.2	.1	.0	W	.3	No	Yes
FE1H		.7	.6	.5	"0"				
FE2H	P1MOD	"0"	"0"	.1	.0	W	No	Yes	No
FE3H									
FE4H	SBUF					R/W	No	No	Yes
FE5H									
FE6H	PMG1	.3	.2	.1	.0	W	No	No	Yes
FE7H		"0"	.6	.5	.4				
FE8H	PMG2	.3	.2	.1	.0				
FE9H		.7	.6	.5	.4				
•									
•									
•									

Table 3. I/O Map for Memory Bank 15 (Concluded)

Memory Bank 15							Addressing Mode		
Address	**Register**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
FF0H	Port 0 (P0)	.3	.2	.1	.0	R/W	Yes	Yes	No
FF1H	Port 1 (P1)	.3	.2	.1	.0	R			
FF2H	Port 2 (P2)	.3	.2	.1	.0	R/W	Yes	Yes	Yes
FF3H	Port 3 (P3)	.3 / .7	.2 / .6	.1 / .5	.0 / .4	R/W			
FF4H	Port 4 (P4)	"0"	.2	.1	.0	R/W	Yes	Yes	No
•									
•									
•									
FFFH									

NOTES:

1. Bit 3 in the WMOD register is read only.
2. The carry flag can be read or written by specific bit manipulation instructions only.

OSCILLATOR CIRCUITS

The S3C7254 microcontroller have two oscillator circuits: a main system clock circuit, and a subsystem clock circuit. The main system clock frequencies can be divided by 4, 8, or 64 by manipulating PCON bits 1 and 0.

The system clock mode control register, SCMOD, lets you select a *main system clock (fx)* or a *subsystem clock (fxt)* as the CPU clock and to start (or stop) main system clock oscillation.

The watch timer, buzzer and LCD display operate normally with a subsystem clock source, since they operate at very slow speeds and with very low power consumption (as low as 122 µs at 32.768 kHz).

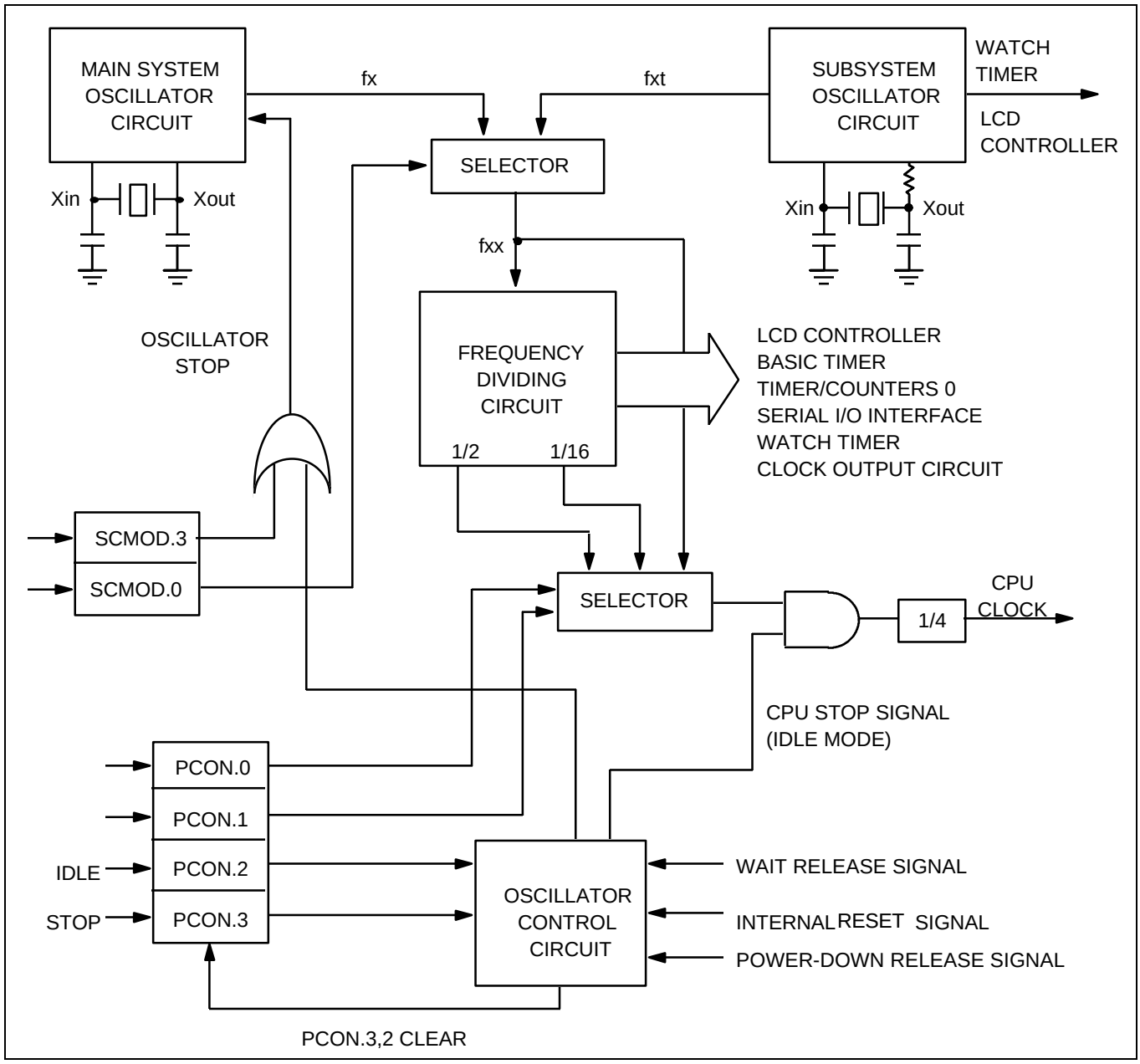


Figure 16. Clock Circuit Diagram

MAIN SYSTEM OSCILLATOR CIRCUITS

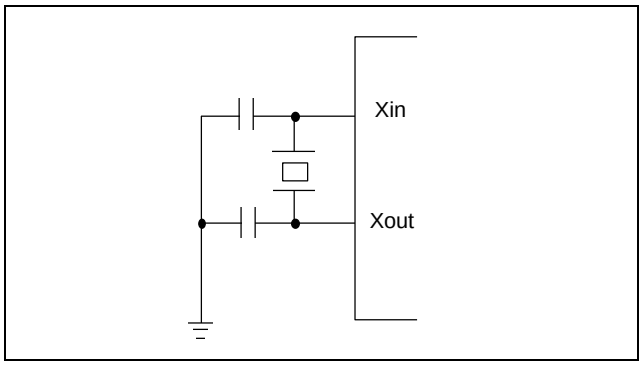


Figure 17. Crystal/Ceramic Oscillator (fx)

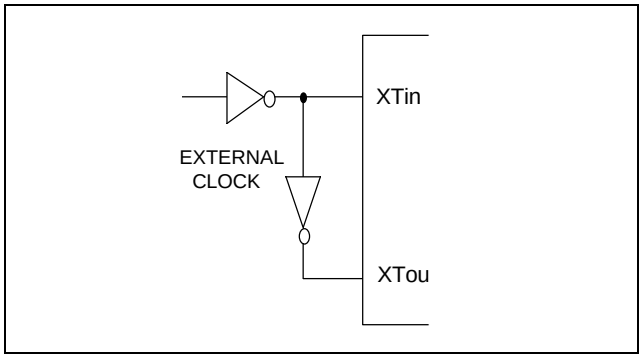


Figure 18. External Oscillator (fx)

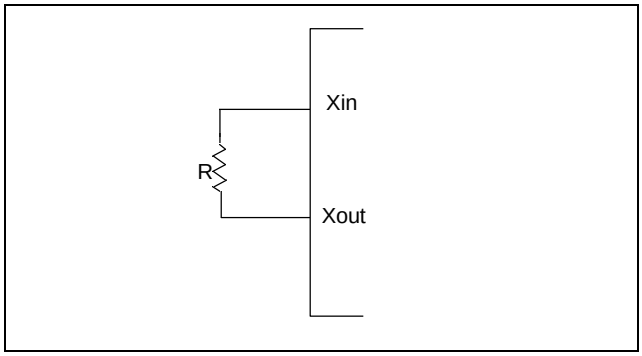


Figure 19. RC Oscillator (fx)

SUBSYSTEM OSCILLATOR CIRCUITS

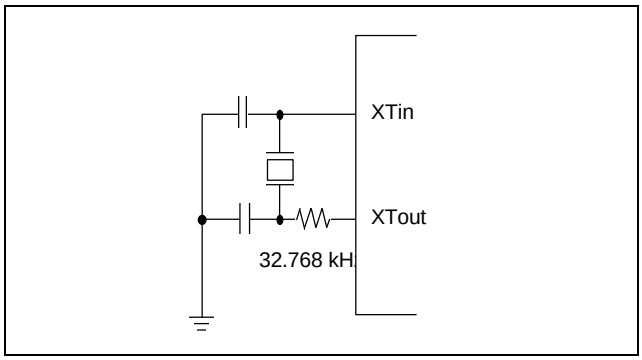


Figure 20. Crystal/Ceramic Oscillator (fxt)

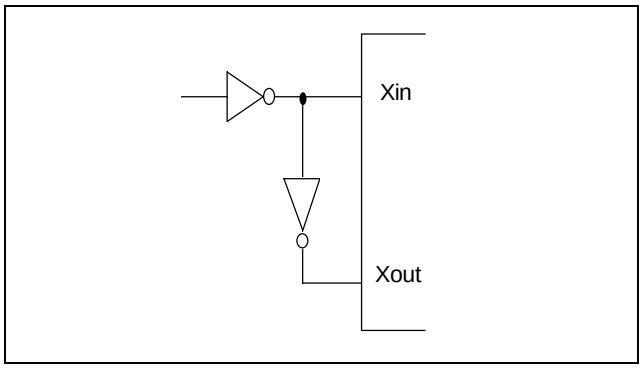


Figure 21. External Oscillator (fxt)

POWER CONTROL REGISTER (PCON)

The power control register, PCON, is a 4-bit register that is used to select the CPU clock frequency and to control CPU operating and power-down modes.

PCON bits 3 and 2 are addressed by the STOP and IDLE instructions, respectively, to engage the idle and stop power-down modes. Idle and stop modes can be initiated by these instruction despite the current value of the enable memory bank flag (EMB). PCON bits 1 and 0 are used to select a specific system clock frequency. There are two basic choices:

— Main system clock (fx) or subsystem clock (fxt);

— Divided fx frequency of 4, 8, or 64.

PCON.1 and PCON.0 settings are also connected with the system clock mode control register, SCMOD. If SCMOD.0 = "0" the main system clock is always selected by the PCON.1 and PCON.0 setting; if SCMOD.0 = "1" the subsystem clock is selected.

Table 4. Power Control Register (PCON) Organization

PCON Bit Settings		Resulting CPU Operating Mode
PCON.3	PCON.2	
0	0	Normal CPU operating mode
0	1	Idle power-down mode
1	0	Stop power-down mode

PCON Bit Settings		Resulting CPU Clock Frequency	
PCON.1	PCON.0	If SCMOD.0 = "0"	If SCMOD.0 = "1"
0	0	fx/64	—
1	0	fx/8	—
1	1	fx/4	fxt/4

☞ PROGRAMMING TIP — Setting the CPU Clock

To set the CPU clock to 0.95 µs at 4.19 MHz:

```
BITS    EMB
SMB     15
LD      A,#3H
LD      PCON,A
```

INSTRUCTION CYCLE TIMES

The unit of time that equals one machine cycle varies depending on whether the main system clock (fx) or a subsystem clock (fxt) is used, and on how the oscillator clock signal is divided (by 4, 8, or 64). Table 5 shows corresponding cycle times in microseconds.

Table 5. Instruction Cycle Times for CPU Clock Rates

Selected CPU Clock	Resulting Frequency	Oscillation Source	Cycle Time (µsec)
fx/64	65.5 kHz	fx = 4.19 MHz	15.3
fx/8	524.0 kHz		1.91
fx/4	1.05 MHz		0.95
fxt/4	8.19 kHz	fxt = 32.768 kHz	122.0

SYSTEM CLOCK MODE REGISTER (SCMOD)

The system clock mode register, SCMOD, is a 4-bit register that is used to select the CPU clock and to control main system clock oscillation. Only its least significant and most significant bits can be manipulated by 1-bit write instructions.

Subsystem clock oscillation cannot, of course, be stopped internally. Also, if you have selected fx as the CPU clock, setting SCMOD.3 to "1" will not stop main system clock oscillation. This can only be done by a STOP instruction.

Table 6. System Clock Mode Register (SCMOD) Organization

SCMOD Register Bit Settings		Resulting Clock Selection	
SCMOD.3	SCMOD.0	CPU Clock	fx Oscillation
0	0	fx	On
0	1	fxt	On
1	1	fxt	Off

SWITCHING THE CPU CLOCK

Together, bit settings in the power control register, PCON, and the system clock mode register, SCMOD, determine whether a main system or a subsystem clock is selected as the CPU clock, and also how this frequency is to be divided. This makes it possible to switch dynamically between main and subsystem clocks and to modify operating frequencies.

SCMOD.3 and SCMOD.0 select the main system clock (fx) or a subsystem clock (fxt) and start or stop main system clock oscillation. PCON.1 and PCON.0 control the frequency divider circuit, and divide the selected fx or fxt clock by 4, 8, or 64.

NOTE

A clock switch operation does not go into effect immediately when you make the SCMOD and PCON register modifications — the previously selected clock continues to run for a certain number of machine cycles.

For example, you are using the default CPU clock (normal operating mode and a main system clock of fx/64) and you want to switch from the fx clock to a subsystem clock and to stop the main system clock. To do this, you first need to set SCMOD.0 to "1". This switches the clock from fx to fxt but allows main system clock oscillation to continue. Before the switch actually goes into effect, a certain number of machine cycles must elapse. After this time interval, you can then disable main system clock oscillation by setting SCMOD.3 to "1".

This same 'stepped' approach must be taken to switch from a subsystem clock to the main system clock: first, clear SCMOD.3 to "0" to enable main system clock oscillation. Then, after a certain number of machine cycles has elapsed, select the main system clock by clearing all SCMOD values to logic zero.

Following a RESET, CPU operation starts with the lowest main system clock frequency of 15.3 µsec at 4.19 MHz after the standard oscillation stabilization interval of 31.3 ms has elapsed. Table 6–4 details the number of machine cycles that must elapse before a CPU clock switch modification goes into effect.

Table 7. Elapsed Machine Cycles During CPU Clock Switch

<table>
<tr><th colspan="2" rowspan="2">AFTER
BEFORE</th><th colspan="6">SCMOD.0 = 0</th><th rowspan="2">SCMOD.0 = 1</th></tr>
<tr><th colspan="2">PCON.1 = 0</th><th colspan="2">PCON.1 = 1</th><th colspan="2">PCON.1 = 1</th></tr>
<tr><td rowspan="6">SCMOD.0 = 0</td><td>PCON.1 = 0</td><td colspan="2" rowspan="2">N/A</td><td colspan="2" rowspan="2">1 MACHINE CYCLE</td><td colspan="2" rowspan="2">1 MACHINE CYCLE</td><td rowspan="2">N/A</td></tr>
<tr><td>PCON.0 = 0</td></tr>
<tr><td>PCON.1 = 1</td><td colspan="2" rowspan="2">8 MACHINE CYCLES</td><td colspan="2" rowspan="2">N/A</td><td colspan="2" rowspan="2">8 MACHINE CYCLES</td><td rowspan="2">N/A</td></tr>
<tr><td>PCON.0 = 0</td></tr>
<tr><td>PCON.1 = 1</td><td colspan="2" rowspan="2">16 MACHINE CYCLES</td><td colspan="2" rowspan="2">16 MACHINE CYCLES</td><td colspan="2" rowspan="2">N/A</td><td rowspan="2">fx / 4fxt</td></tr>
<tr><td>PCON.0 = 1</td></tr>
<tr><td>SCMOD.0 = 1</td><td></td><td colspan="2">N/A</td><td colspan="2">N/A</td><td colspan="2">fx / 4fxt (M/C)</td><td>N/A</td></tr>
</table>

NOTES:
1. Even if oscillation is stopped by setting SCMOD.3 during main system clock operation, the stop mode is not entered.
2. Since the Xin input is connected internally to V_{SS} to avoid current leakage due to the crystal oscillator in stop mode, do not set SCMOD.3 to "1" when an external clock is used as the main system clock.
3. When the system clock is switched to the subsystem clock, it is necessary to disable any interrupts which may occur during the time intervals shown in Table 6–4.
4. 'N/A' means 'not available'.

☞ PROGRAMMING TIP — Switching Between Main System and Subsystem Clock

1. Switch from the main system clock to the subsystem clock:

```
MA2SUB  BITS    SCMOD.0     ;  Switches to subsystem clock
        CALL    DLY80       ;  Delay 80 machine cycles
        BITS    SCMOD.3     ;  Stop the main system clock
        RET
DLY80   LD      A,#0FH
DEL1    NOP
        NOP
        DECS    A
        JR      DEL1
        RET
```

2. Switch from the subsystem clock to the main system clock:

```
SUB2MA  BITR    SCMOD.3     ;  Start main system clock oscillation
        CALL    DLY80       ;  Delay 80 machine cycles
        BITR    SCMOD.0     ;  Switch to main system clock
        RET
```

CLOCK OUTPUT MODE REGISTER (CLMOD)

The clock output mode register, CLMOD, is a 4-bit register that is used to enable or disable clock output to the CLO pin and to select the CPU clock source and frequency. CLMOD is addressable by 4-bit write instructions only.

RESET clears CLMOD to logic zero, which automatically selects the CPU clock as the clock source (without initiating clock oscillation), and disables clock output.

CLMOD.3 is the enable/disable clock output control bit; CLMOD.1 and CLMOD.0 are used to select one of four possible clock sources and frequencies: normal CPU clock, fxx/8, fxx/16, or fxx/64. Table 6–5. Clock Output Mode Register (CLMOD) Organization

Table 8. Clock Output Mode Register (CLMOD) Organization

CLMOD Bit Settings		Resulting Clock Output	
CLMOD.1	**CLMOD.0**	**Clock Source**	**Frequency**
0	0	CPU clock (fx/4, fx/8, fx/64, fxt/4)	1.05 MHz, 524 kHz, 65.5 kHz, 8.19 kHz
0	1	fxx/8	524 kHz, 4.096 kHz
1	0	fxx/16	262 kHz, 2.048 kHz
1	1	fxx/64	65.5 kHz, 0.512 kHz

CLMOD.3	Result of CLMOD.3 Setting
0	Clock output is disabled
1	Clock output is enabled

NOTE: Frequencies assume that fxx is 4.19 MHz and fxt is 32.768 kHz.

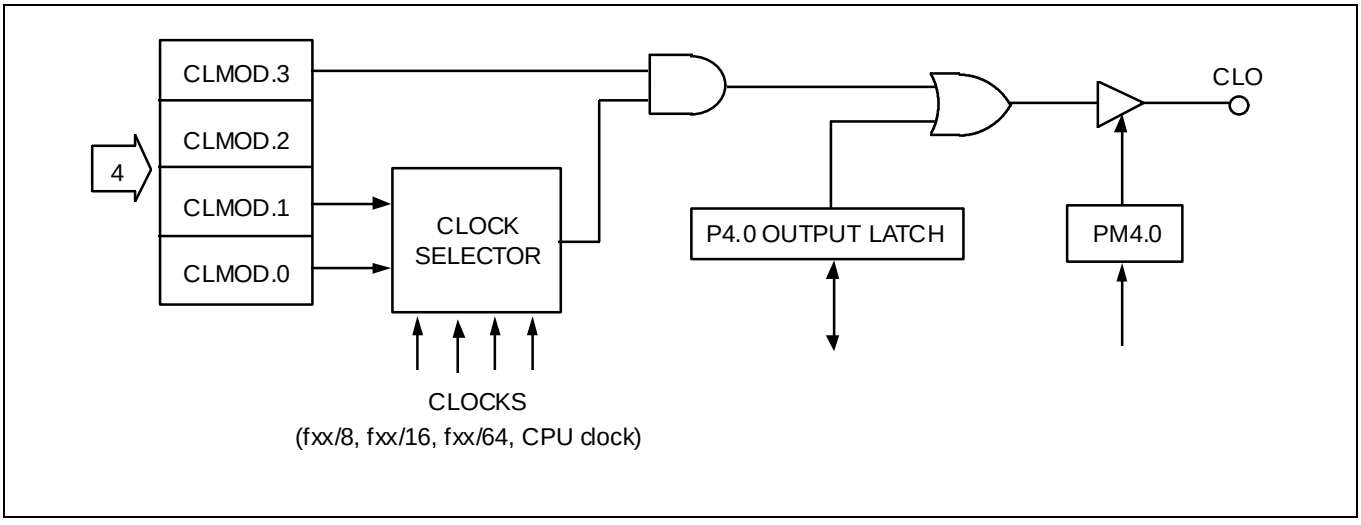


Figure 22. CLO Output Pin Circuit Diagram

☞ PROGRAMMING TIP — CPU Clock Output to the CLO Pin

To output the CPU clock to the CLO pin:

```
BITS    EMB
SMB     15
LD      EA,#10H
LD      PMG1,EA          ;  P4.0 ← Output mode
BITR    P4.0             ;  Clear P4.0 output latch
LD      A,#9H
LD      CLMOD,A
```

INTERRUPTS

The S3C7254 has four external, three internal and two quasi interrupts. Table 9 shows the conditions for each interrupt generation. The request flags that allow the interrupts to be generated are cleared to logic zero by hardware when the service routine is vectored. The quasi interrupt (INT2, IRQW) request flags must be cleared by software.

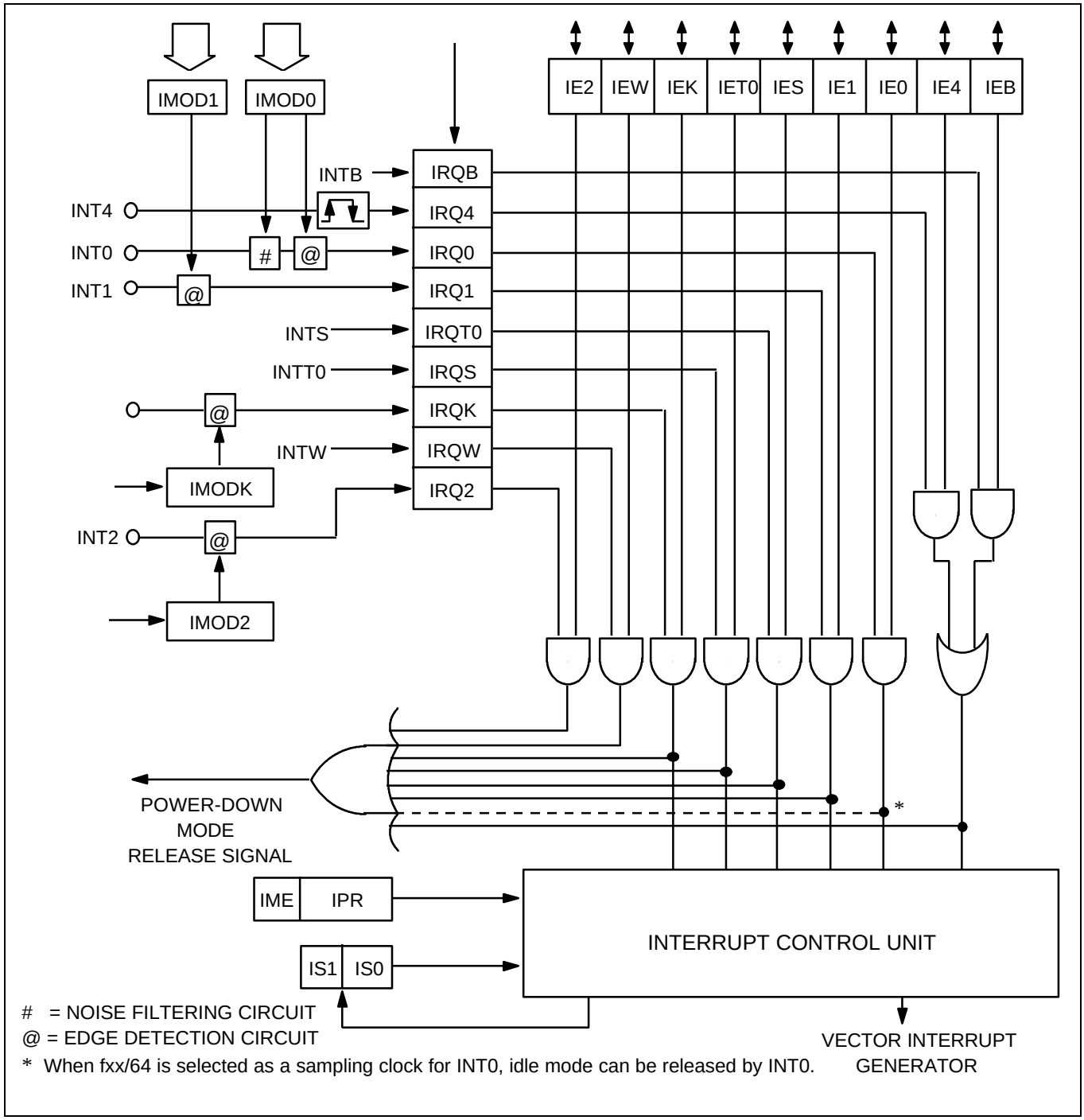


Figure 23. Interrupt Control Circuit Diagram

Table 9. Interrupt Request Flag Conditions and Priorities

Interrupt Source	Internal / External	Pre-condition for IRQx Flag Setting	Interrupt Priority	IRQ Flag Name
INTB	I	Reference time interval signal from basic timer	1	IRQB
INT4	E	Both rising and falling edges detected at INT4	1	IRQ4
INT0	E	Rising or falling edge detected at INT0 pin	2	IRQ0
INT1	E	Rising or falling edge detected at INT1 pin	3	IRQ1
INTS	I	Completion signal for serial transmit-and-receive or receive-only operation	4	IRQS
INTT0	I	Signals for TCNT0 and TREF0 registers match	5	IRQT0
INTK	E	When a rising or falling edge detected at any one of the K0–K3 pins	6	IRQK
INT2 *	E	Rising or falling edge detected at INT2	—	IRQ2
INTW	I	Time interval of 0.5 second or 3.19 ms	—	IRQW

NOTE: The quasi-interrupt INT2 is only used for testing incoming signals.

INTERRUPT ENABLE FLAGS (IEX)

IEx flags, when set to logical one, enable specific interrupt requests to be serviced. When the interrupt request flag is set to logical one, an interrupt will not be serviced until its corresponding IEx flag is also enabled.

Interrupt enable flags can be read, written, or tested directly by 1-bit instructions. IEx flags can be addressed directly at their specific RAM addresses, despite the current value of the enable memory bank (EMB) flag.

Table 10. Interrupt Enable and Request Flag

Address	Bit 3	Bit 2	Bit 1	Bit 0
FB8H	IE4	IRQ4	IEB	IRQB
FBAH	0	0	IEW	IRQW
FBBH	0	0	IEK	IRQK
FBCH	0	0	IET0	IRQT0
FBDH	0	0	IES	IRQS
FBEH	IE1	IRQ1	IE0	IRQ0
FBFH	0	0	IE2	IRQ2

NOTES:
1. IEx refers generically to all interrupt enable flags.
2. IRQx refers generically to all interrupt request flags.
3. IEx = 0 is interrupt disable mode.
4. IEx = 1 is interrupt enable mode.

INTERRUPT PRIORITY REGISTER (IPR)

The 4-bit interrupt priority register (IPR) is used to control multi-level interrupt handling. Its reset value is logic zero. Before the IPR can be modified by 4-bit write instructions, all interrupts must first be disabled by a DI instruction.

By manipulating the IPR settings, you can choose to process all interrupt requests with the same priority level, or you can select one type of interrupt for high-priority processing. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

Table 11. Standard Interrupt Priorities

Interrupt	Default Priority
INTB, INT4	1
INT0	2
INT1	3
INTS	4
INTT0	5
INTK	6

The MSB of the IPR, the interrupt master enable flag (IME), enables and disables all interrupt processing. Even if an interrupt request flag and its corresponding enable flag are set, a service routine cannot be executed until the IME flag is set to logic one. The IME flag can be directly manipulated by EI and DI instructions, regardless of the current enable memory bank (EMB) value.

Table 12. Interrupt Priority Register Settings

IPR.2	IPR.1	IPR.0	Result of IPR Bit Setting
0	0	0	Process all interrupt requests at low priority (NOTE)
0	0	1	Process INTB and INT4 interrupts only
0	1	0	Process INT0 interrupts only
0	1	1	Process INT1 interrupts only
1	0	0	Process INTS interrupts only
1	0	1	Process INTT0 interrupts only
1	1	0	Process INTK interrupts only

NOTE: When all interrupts are low priority (the lower three bits of the IPR register are logic zero), the interrupt requested first will have high priority. Therefore, the first- request interrupt cannot be superceded by any other interrupt.

EXTERNAL INTERRUPT 0, 1 AND 2 MODE REGISTERS (IMOD0, IMOD1 AND IMOD2)

The following components are used to process external interrupts at the INT0, INT1 and INT2 pins:

— Noise filtering circuit for INT0

— Edge detection circuit

— Three mode registers, IMOD0, IMOD1 and IMOD2

The mode registers are used to control the triggering edge of the input signal. IMOD0, IMOD1 and IMOD2 settings let you choose either the rising or falling edge of the incoming signal as the interrupt request trigger. The INT4 interrupt is an exception since its input signal generates an interrupt request on both rising and falling edges. Since INT2 is a qusi-interrupt, the interrupt request flag (IRQ2) must be cleared by software.

IMOD0, IMOD1 and IMOD2 are addressable by 4-bit write instructions. RESET clears all IMOD values to logic zero, selecting rising edges as the trigger for incoming interrupt requests.

Table 13. IMOD0, 1 and 2 Register Organization

IMOD0	IMOD0.3	0	IMOD0.1	IMOD0.0	Effect of IMOD0 Settings
	0				Select CPU clock for sampling
	1				Select fxx/64 sampling clock
			0	0	Rising edge detection
			0	1	Falling edge detection
			1	0	Both rising and falling edge detection
			1	1	IRQ0 flag cannot be set to "1"

IMOD1 IMOD2	0	0	0	IMOD1.0 IMOD2.0	Effect of IMOD1 and IMOD2 Settings
				0	Rising edge detection
				1	Falling edge detection

When a sampling clock rate of fxx/64 is used for INT0, an interrupt request flag must be cleared before 16 machine cycles have elapsed. Since the INT0 pin has a clock-driven noise filtering circuit built into it, please take the following precautions when you use it:

— To trigger an interrupt, the input signal width at INT0 must be at least two times wider than the pulse width of the clock selected by IMOD0. This is true even when the INT0 pin is used for general-purpose input.

— you can use INT0 to release idle mode, when fxx/64 is selected as a sampling clock.

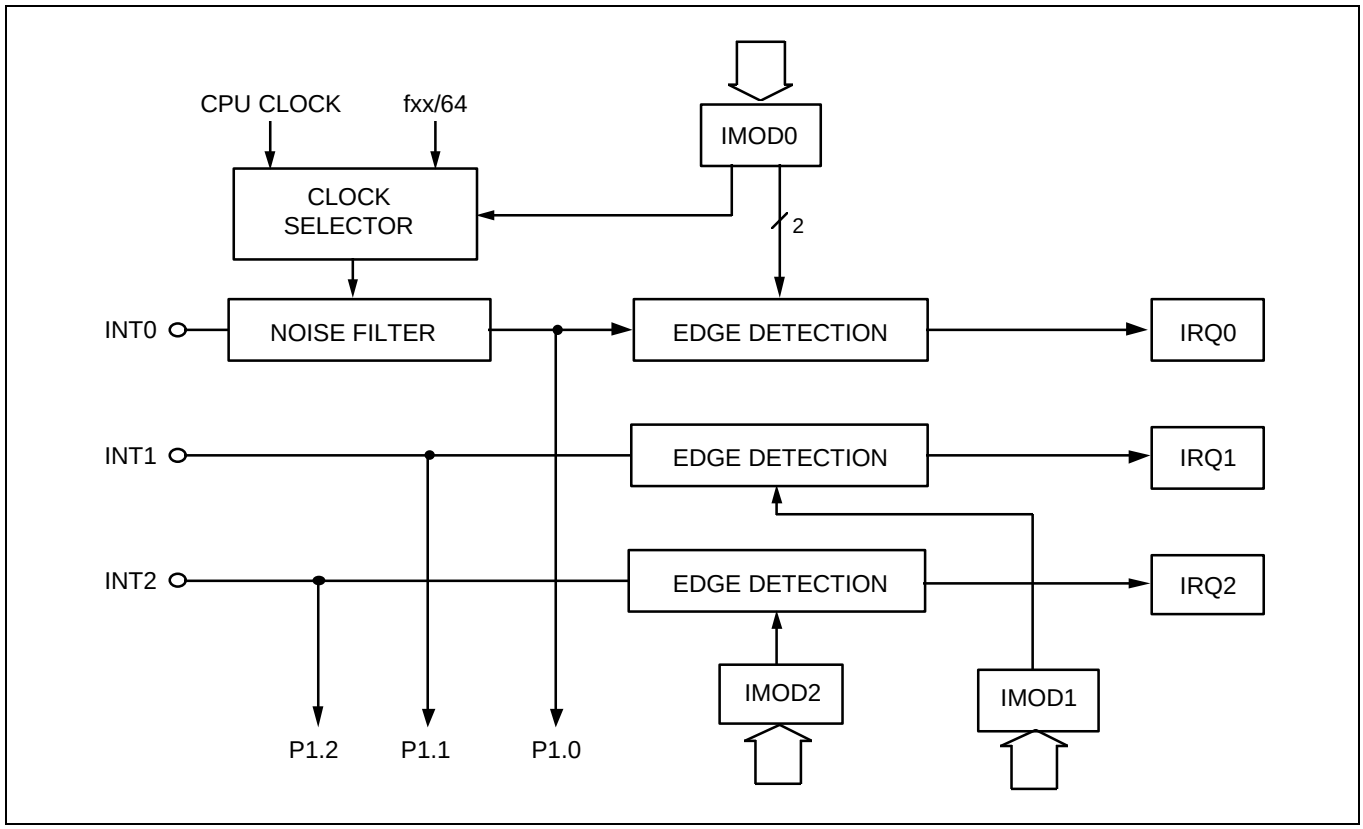


Figure 24. Circuit Diagram for INT0, INT1 and INT2 Pins

EXTERNAL KEY INTERRUPT MODE REGISTER (IMODK)

The mode register for external key interrupts at the K0–K3 pins, IMODK, is addressable only by 4-bit write instructions. RESET clears all IMODK bits to logic zero.

Rising or falling edge can be detected by bit IMODK.2 settings. If a rising or falling edge is detected at any one of the selected K pin by the IMODK register, the IRQK flag is set to logic one and a release signal for power-down mode is generated.

Table 14. IMODK Register Bit Settings

IMODK	0	IMODK.2	IMODK.1	IMODK.0	Effect of IMODK Settings
		0, 1	0	0	Disable key interrupt
			0	1	Enable edge detection at the K0–K1 pins
			1	0	Enable edge detection at the K0–K2 pins
			1	1	Enable edge detection at the K0–K3 pins

IMODK.2		
	0	Falling edge detection
	1	Rising edge detection

NOTE:
1. To generate a key interrupt, the selected pins must be configured to input mode. If any one pin of the selected pins is configured to output mode, only falling edge can be detected.
2. To generate a key interrupt, first, configure pull-up resistors or external pull-down resistors. And then, select edge detection and pins by setting IMODK register.

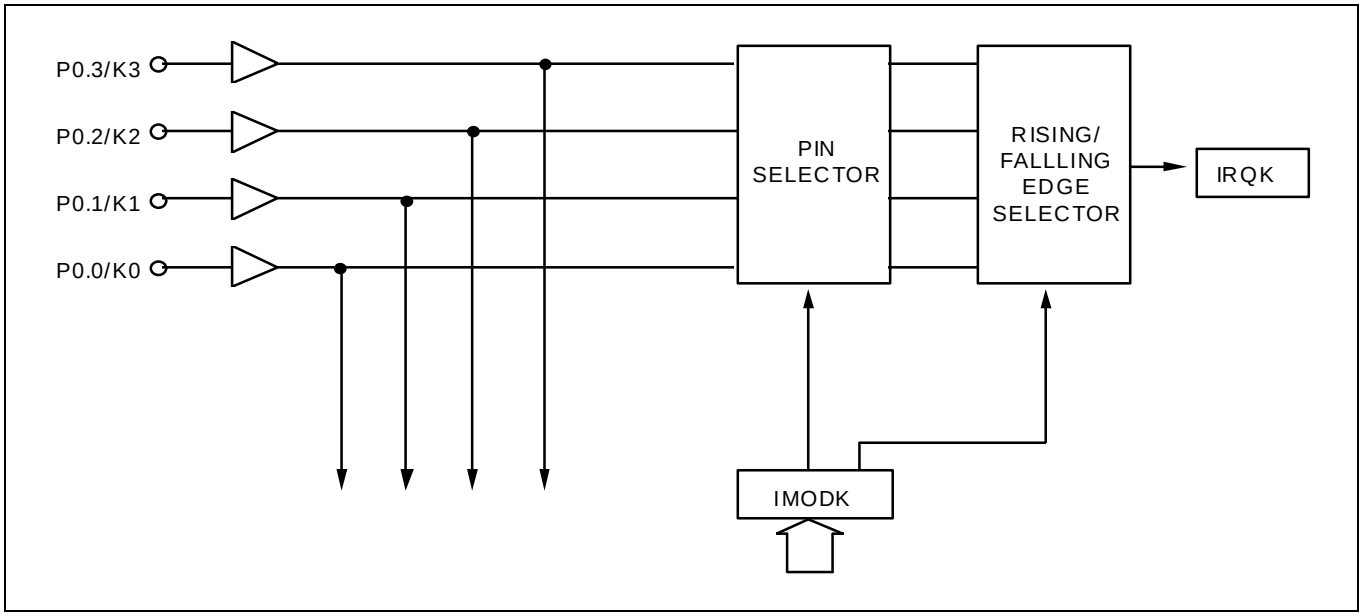


Figure 25. Circuit Diagram for INTK

POWER-DOWN

The S3C7254 microcontroller has two power-down modes to reduce power consumption: idle and stop. Idle mode is initiated by the IDLE instruction and stop mode by the instruction STOP. (Several NOP instructions must always follow an IDLE or STOP instruction in a program.) In idle mode, the CPU clock stops while peripherals and the oscillation source continue to operate normally.

In stop mode, main system clock oscillation is halted (assuming it is currently operating), and peripheral hardware components are powered-down. The effect of stop mode on specific peripheral hardware components — CPU, basic timer, serial I/O, timer/counter 0, watch timer, and LCD controller — and on external interrupt requests, is detailed in Table 15.

Table 15. Hardware Operation During Power-Down Modes

Operation	Stop Mode (STOP)	Idle Mode (IDLE)
System clock status	Can be changed only if the main system clock is used	Can be changed if the main system clock or subsystem clock is used
Clock oscillator	Main system clock oscillation stops	CPU clock oscillation stops (main and subsystem clock oscillation continues)
Basic timer	Basic timer stops	Basic timer operates (with IRQB set at each reference interval)
Serial I/O interface	Operates only if external SCK input is selected as the serial I/O clock	Operates if a clock other than the CPU clock is selected as the serial I/O clock
Timer/counter 0	Operates only if TCL0 is selected as the counter clock	Timer/counter 0 operates
Watch timer	Operates only if subsystem clock (fxt) is selected as the counter clock	Watch timer operates
LCD controller	Operates only if a subsystem clock is selected as LCDCK	LCD controller operates
External interrupts	INT1, INT2, INT4, and INTK are acknowledged; INT0 is not serviced	INT1, INT2, INT4, INT0, and INTK are acknowledged (NOTE)
CPU	All CPU operations are disabled	All CPU operations are disabled
Mode release signal	Interrupt request signals (except INT0) are enabled by an interrupt enable flag or by RESET input	Interrupt request signals are enabled by an interrupt enable flag or by RESET input (NOTE)

NOTE: INT0 can be operated in idle mode only when fxx/64 is selected as a sampling clock.

☞ PROGRAMMING TIP — Reducing Power Consumption for Key Input Interrupt Processing

The following code shows real-time clock and interrupt processing for key inputs to reduce power consumption. In this example, the system clock source is switched from the main system clock to a subsystem clock and the LCD display is turned on:

```
KEYCLK  DI
        CALL    MA2SUB      ;  Main system  clock → subsystem clock switch
                            subroutine
        SMB     15
        LD      EA,#00H
        LD      P2,EA       ;  All key strobe outputs to low level
        LD      A,#3H
        LD      IMODK,A     ;  Select K0–K3 enable
        SMB     0
        BITR    IRQW
        BITR    IRQK
        BITS    IEW
        BITS    IEK
CLKS1   CALL    WATDIS      ;  Execute clock and display changing subroutine
        BTSTZ   IRQK
        JR      CIDLE
        CALL    SUB2MA      ;  Subsystem clock → main system clock switch
                            subroutine
        EI
        RET
CIDLE   IDLE                ;  Engage idle mode
        NOP
        NOP
        JPS     CLKS1
```

RECOMMENDED CONNECTIONS FOR UNUSED PINS

To reduce overall power consumption, please configure unused pins according to the guidelines described in Table 16.

Table 16. Unused Pin Connections for Reduced Power Consumption

Pin/Share Pin Names	Recommended Connection
P0.0 / SCK / K0 P0.1 / SO / K1 P0.2 / SI / K2 P0.3 / BUZ / K3	Input mode: Connect to V_{DD} Output mode: No connection
P1.0 / CIN0 / INT0 P1.1 / CIN1 /INT1 P1.2 / INT2 P1.3 / INT4	Connect to V_{DD} (1)
P2.0–P2.3	Input mode: Connect to V_{DD} Output mode: No connection
P3.0–P3.1 P3.2 / LCDSY P3.0 / LCDCK P4.0 / CLO P4.1 / TCL0 P4.2 / TCLO0	Input mode: Connect to V_{DD} Output mode: No connection
P5.0 / SEG32–P5.7 / SEG39	No connection (2)
SEG0–SEG29 SEG30–SEG31 COM0–COM7	No connection
V_{LC1}–V_{LC5}	No connection
XT_{in}	Connect XT_{in} to V_{SS} or V_{DD}
XT_{out}	No connection
TEST	Connect to V_{SS}

NOTES
1. Digital mode at P1.0 and P1.1
2. Used as segment

RESET

Table 17 provides detailed information about hardware register values after a RESET occurs during power-down mode or during normal operation.

Table 17. Hardware Register Values After RESET

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
Program counter (PC)	Lower six bits of address 0000H are transferred to PC11–8, and the contents of 0001H to PC7–0.	Lower six bits of address 0000H are transferred to PC11–8, and the contents of 0001H to PC7–0.
Bank selection registers (SMB, SRB)	0, 0	0, 0
BSC register (BSC0–BSC3)	0	0
Program Status Word (PSW):		
Carry flag (C)	Retained	Undefined
Skip flag (SC0–SC2)	0	0
Interrupt status flags (IS0, IS1)	0	0
Bank enable flags (EMB, ERB)	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.
Stack pointer (SP)	Undefined	Undefined
Data Memory (RAM):		
Working registers E, A, L, H, X, W, Z, Y	Values retained	Undefined
General-purpose registers	Values retained (note)	Undefined
Clocks:		
Power control register (PCON)	0	0
Clock output mode register (CLMOD)	0	0
System clock mode register (SCMOD)	0	0
Interrupts:		
Interrupt request flags (IRQx)	0	0
Interrupt enable flags (IEx)	0	0
Interrupt priority flag (IPR)	0	0
Interrupt master enable flag (IME)	0	0
INT0 mode register (IMOD0)	0	0
INT1 mode register (IMOD1)	0	0
INT2 mode register (IMOD2)	0	0
INTK mode register (IMODK)	0	0

NOTE: The values of the 0F8H-0FDH are not retained when a RESET signal is input.

Table 17. Hardware Register Values After RESET (Continued)

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
I/O Ports:		
Output buffers	Off	Off
Output latches	0	0
Port mode flags (PM)	0	0
Pull-up resistor mode reg (PUMOD1/2)	0	0
Basic Timer:		
Count register (BCNT)	Undefined	Undefined
Mode register (BMOD)	0	0
Timer/Counters 0 and 1:		
Count registers (TCNT0)	0	0
Reference registers (TREF0)	FFH	FFH
Mode registers (TMOD0)	0	0
Output enable flags (TOE0)	0	0
Watch Timer:		
Watch timer mode register (WMOD)	0	0
LCD Driver/Controller:		
LCD mode register (LMOD)	0	0
LCD control register (LCON)	0	0
Display data memory	Values retained	Undefined
Output buffers	Off	Off
Serial I/O Interface:		
SIO mode register (SMOD)	0	0
SIO interface buffer (SBUF)	Values retained	Undefined
N-Channel Open-Drain Mode Register		
PNE1/2/3	0	0
Comparator		
Comparator mode register (CMOD)	0	0
Comparison result register	Undefined	Undefined

I/O PORTS

The S3C7254 has 6 ports. There are total of 4 input pins, 8 output pin and 15 configurable I/O pins, for a maximum number of 27 pins.

PORT MODE FLAGS (PM FLAGS)

Port mode flags (PM) are used to configure I/O ports to input or output mode by setting or clearing the corresponding I/O buffer.

When a PM flag is "0", the port is set to input mode; when it is "1", the port is enabled for output. RESET clears all port mode flags to logical zero, automatically configuring the corresponding I/O ports to input mode.

Table 18. Port Mode Group Flags

PM Group ID	Address	Bit 3	Bit 2	Bit 1	Bit 0
PMG1	FE6H	PM0.3	PM0.2	PM0.1	PM0.0
	FE7H	"0"	PM4.2	PM4.1	PM4.0
PMG2	FE8H	PM2.3	PM2.2	PM2.1	PM2.0
	FE9H	PM3.3	PM3.2	PM3.1	PM3.0

NOTE: If bit = "0", the corresponding I/O pin is set to input mode. If bit ="1", the pin is set to output mode: PM0.0 for P0.0, PM0.1 for P0.1, etc,. All flags are cleared to logic zero following RESET.

☞ PROGRAMMING TIP — Configuring I/O Ports to Input or Output

Configure ports 0 and 2 as an output port:

```
BITS    EMB
SMB     15
LD      EA,#7FH
LD      PMG1,EA          ;  P0 and P4 ← Output
```

PORT 1 MODE REGISTER (P1MOD)

P1MOD register settings determine if port 1 is used for digital input or for analog input. The P1MOD register is a 4-bit write only register. P1MOD is mapped to address FE2H. A reset operation initializes all P1MOD values to logic zero, configuring port 1 as an analog input port.

When a P1MOD bit is "0", the corresponding pin is configured as a analog input pin. When set to "1", it is configured as an digital input pin: P1MOD.0 corresponds to P1.0, and P1MOD.1 to P1.1.

NOTE

INT0 and INT1 can occur only when the port is configured to digital input. If you change the input mode from digital to analog using P1MOD settings, IRQ0 and IRQ1 will be set. **When you use analog input, you must clear the corresponding interrupt enable flag (IEx).** That is, clear IE0 when P1.0 is an analog input and clear IE1 when P1.1 is an analog input.

PULL-UP RESISTOR MODE REGISTER (PUMOD)

The pull-up resistor mode registers (PUMOD1 and PUMOD2) are used to assign internal pull-up resistors by software to specific ports. When a configurable I/O port pin is used as an output pin, its assigned pull-up resistor is automatically disabled, even though the pin's pull-up is enabled by a corresponding PUMOD bit setting.

Table 19. Pull-Up Resistor Mode Register (PUMOD) Organization

PUMOD ID	Address	Bit 3	Bit 2	Bit 1	Bit 0
PUMOD1	FDCH	PUR3	PUR2	“0”	PUR0
	FDDH	0	0	0	PUR4
PUMOD2	FDEH	PUR1.3	PUR1.2	PUR1.1	PUR1.0

NOTE: When bit = "1", a pull-up resistor is assigned to the corresponding I/O port: PUR3 for port 3, PUR2 for port 2, and so on.

☞ PROGRAMMING TIP — Enabling and Disabling I/O Port Pull-Up Resistors

P6 and P7 enable pull-up resistors.

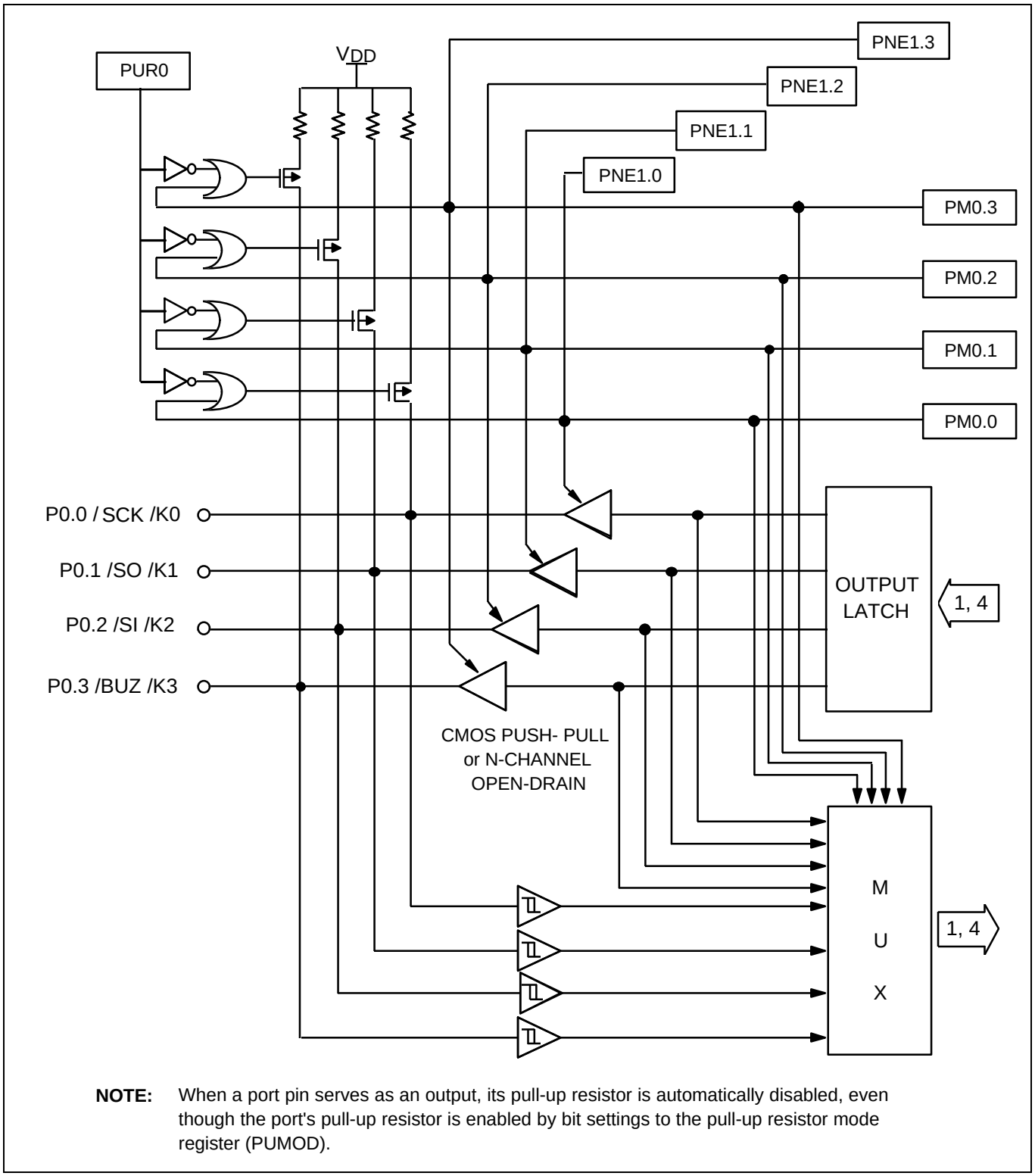
```
BITS    EMB
SMB     15
LD      EA,#0CH
LD      PUMOD1,EA          ;  P2 and P3 enable
```

N-CHANNEL OPEN-DRAIN MODE REGISTER

The n-channel open-drain mode register (PNE) is used to configure ports 0, 2, 3 and 4 to n-channel open-drain or as push-pull outputs. When a bit in the PNE register is set to "1", the corresponding output pin is configured to n-channel, open-drain; when set to "0", the output pin is configured to push-pull. The PNE register consists of an 8-bit register and a 4-bit register; PNE1 and PNE3 can be addressed by 4-bit write instructions only and PNE2 by 8-bit write instructions only.

PNE ID	ADDRESS	Bit 3	Bit 2	Bit 1	Bit 0
PNE1	FA6H	P0.3	P0.2	P0.1	P0.0
PNE2	FA8H	P2.3	P2.2	P2.1	P2.0
	FA9H	P3.3	P3.2	P3.1	P3.0
PNE3	FAAH	0	P4.2	P4.1	P4.0

PORT 0 CIRCUIT DIAGRAM



NOTE: When a port pin serves as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 26. Port 0 Circuit Diagram

PORT 1 CIRCUIT DIAGRAM

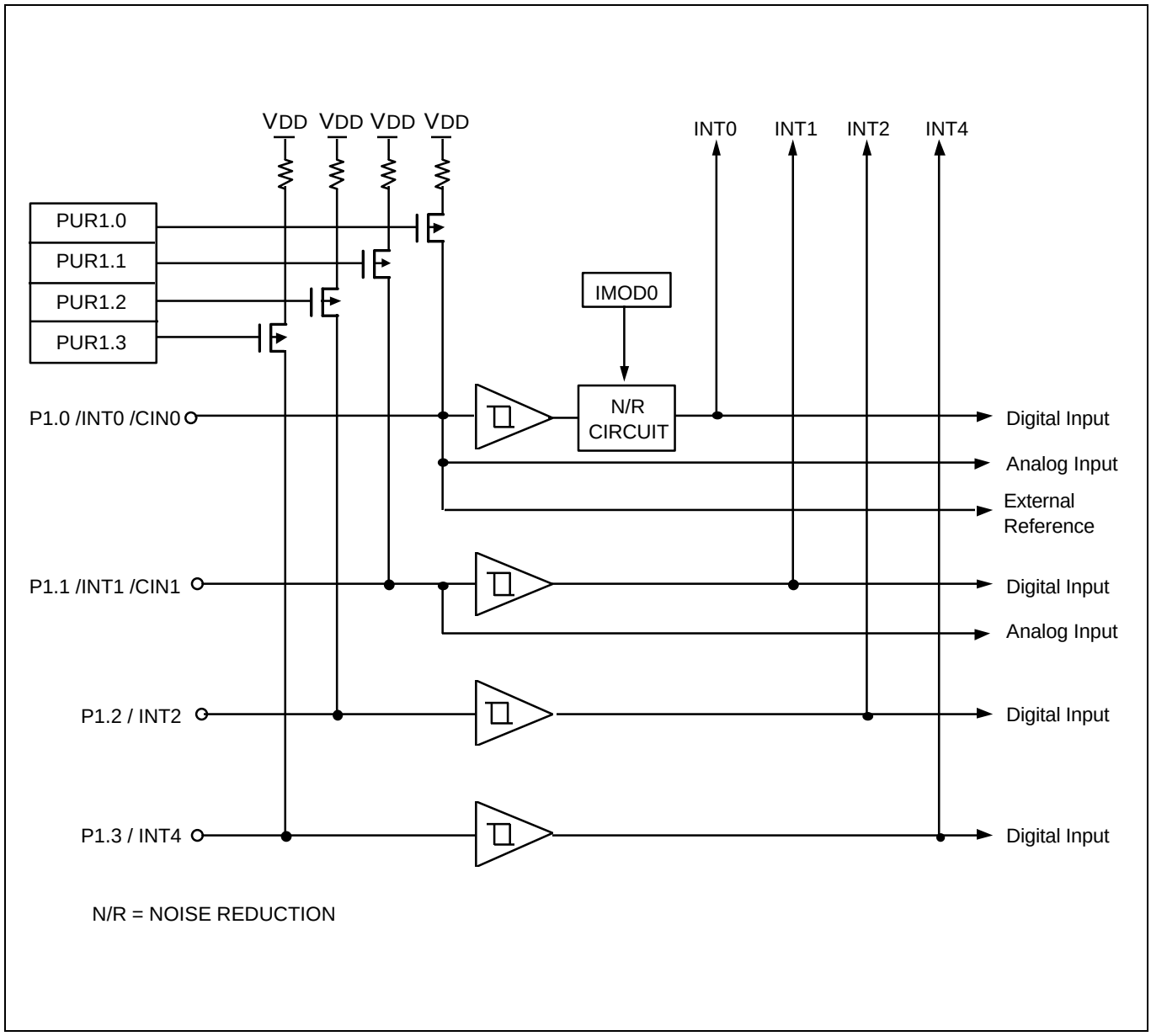
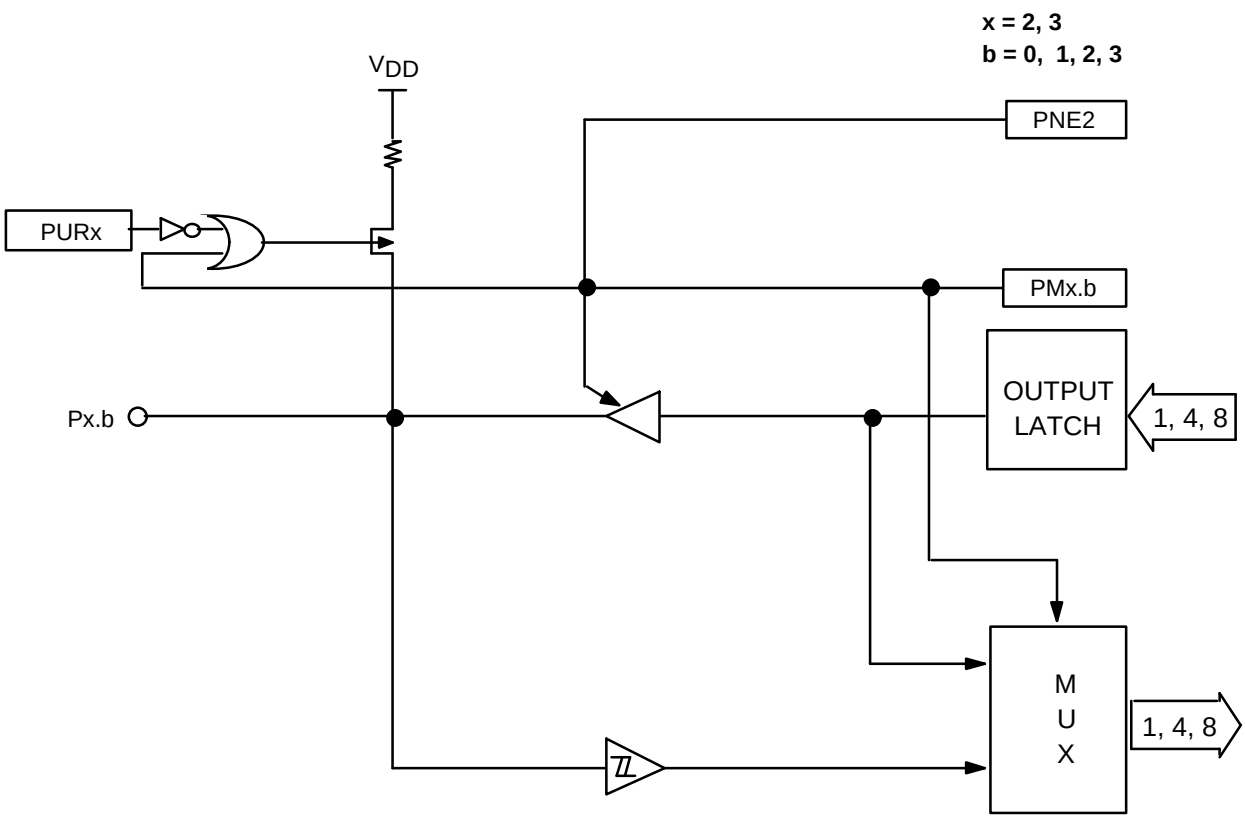


Figure 27. Input Port 1 Circuit Diagram

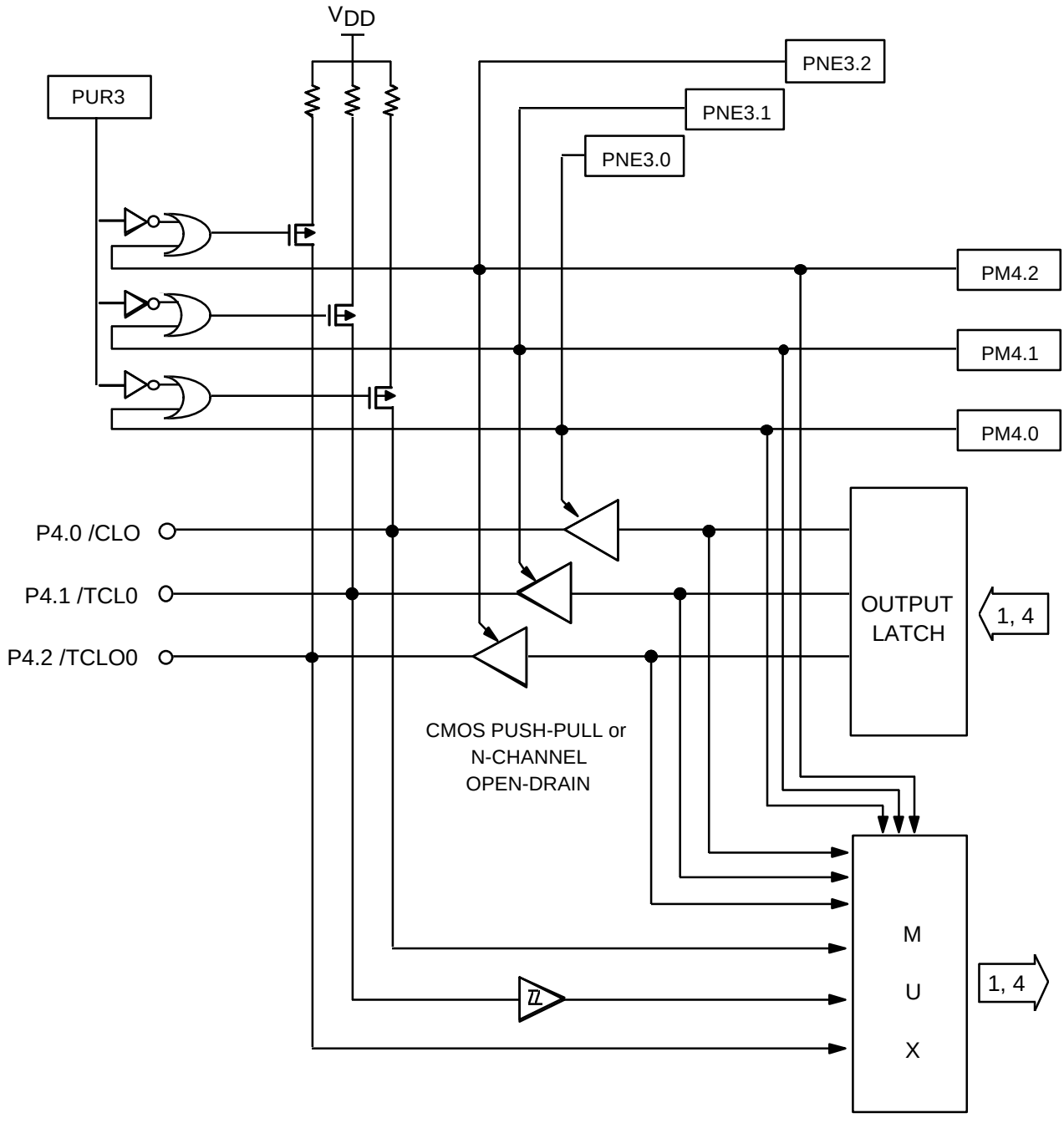
PORTS 2 AND 3 CIRCUIT DIAGRAM



NOTE: When a port pin serves as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 28. Ports 2 and 3 Circuit Diagram

PORT 4 CIRCUIT DIAGRAM



NOTE: When a port pin serves as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 29. Port 4 Circuit Diagram

BASIC TIMER (BT)

The basic timer generates interrupt requests at precise intervals, based on the frequency of the system clock.

You can use the basic timer as a "watchdog" timer for monitoring system events or use BT output to stabilize clock oscillation when stop mode is released by an interrupt and following RESET.

Interval Timer Function

The measurement of elapsed time intervals is the basic timer's primary function. The standard interval is 256 BT clock pulses.

To restart the basic timer, set bit 3 of the mode register BMOD to logic one. The input clock frequency and the interrupt and stabilization interval are selected by loading the appropriate bit values to BMOD.2–BMOD.0.

The 8-bit counter register, BCNT, is incremented each time a clock signal is detected that corresponds to the frequency selected by BMOD. BCNT continues incrementing as it counts BT clocks until an overflow occurs.

An overflow causes the BT interrupt request flag (IRQB) to be set to logic one to signal that the designated time interval has elapsed. An interrupt request is then generated, BCNT is cleared to logic zero, and counting continues from 00H.

Oscillation Stabilization Interval Control

Bits 2–0 of the BMOD register are used to select the input clock frequency for the basic timer. This setting also determines the time interval (also referred to as 'wait time') required to stabilize clock signal oscillation when power-down mode is released by an interrupt. When a RESET signal is generated, the standard stabilization interval for system clock oscillation following a RESET is 31.3 ms at 4.19 MHz.

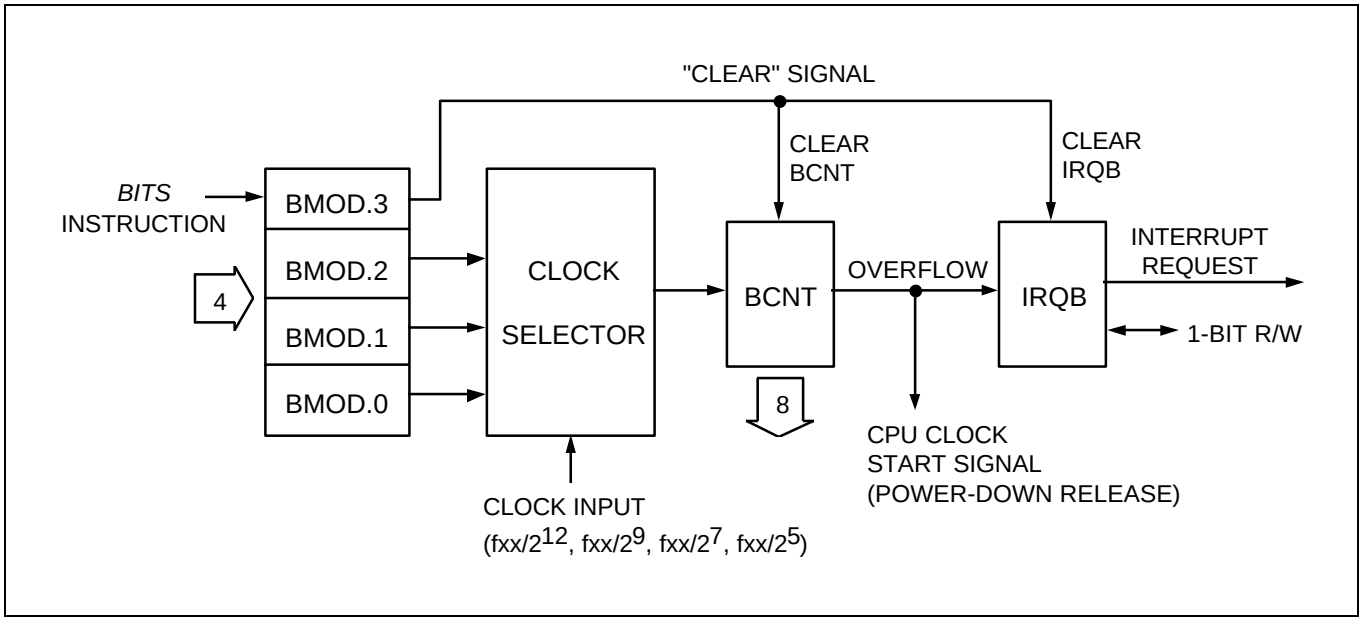


Figure 30. Basic Timer Circuit Diagram

BASIC TIMER MODE REGISTER (BMOD)

The basic timer mode register, BMOD, is used to select the input frequency and the oscillation stabilization time.

The most significant bit of the BMOD register, BMOD.3, is used to restart the basic timer. When BMOD.3 is set to logic one (enabled) by a 1-bit write instruction, the contents of the BT counter register (BCNT) and the BT interrupt request flag (IRQB) are both cleared to logic zero, and timer operation is restarted.

Table 20. Basic Timer Mode Register (BMOD) Organization

BMOD.3	Basic Timer Restart Bit
1	Restart basic timer; clear IRQB, BCNT, and BMOD.3 to "0"

BMOD.2	BMOD.1	BMOD.0	Basic Timer Input Clock	Oscillation Stabilization
0	0	0	fxx/2^{12} (1.02 kHz)	2^{20}/fxx (250 ms)
0	1	1	fxx/2^{9} (8.18 kHz)	2^{17}/fxx (31.3 ms)
1	0	1	fxx/2^{7} (32.7 kHz)	2^{15}/fxx (7.82 ms)
1	1	1	fxx/2^{5} (131 kHz)	2^{13}/fxx (1.95 ms)

NOTES:
1. Clock frequencies and stabilization intervals assume a system oscillator clock frequency (fxx) of 4.19 MHz.
2. fxx = selected system clock frequency.
3. Oscillation stabilization time is the time required to stabilize clock signal oscillation after stop mode is released. The data in the table column 'Oscillation Stabilization' can also be interpreted as "Interrupt Interval Time."
4. The standard stabilization time for system clock oscillation following a RESET is 31.3 ms at 4.19 MHz.

BASIC TIMER COUNTER (BCNT)

BCNT is an 8-bit counter for the basic timer. It can be addressed by 8-bit read instructions.

When BCNT has incremented to hexadecimal 'FFH' (255 clock pulses), it is cleared to '00H' and an overflow is generated. The overflow causes the interrupt request flag, IRQB, to be set to logic one. When the interrupt request is generated, BCNT immediately resumes counting incoming clock signals.

NOTE

Always execute a BCNT read operation twice to eliminate the possibility of reading unstable data while the counter is incrementing. If, after two consecutive reads, the BCNT values match, you can select the latter value as valid data. Until the results of the consecutive reads match, however, the read operation must be repeated until the validation condition is met.

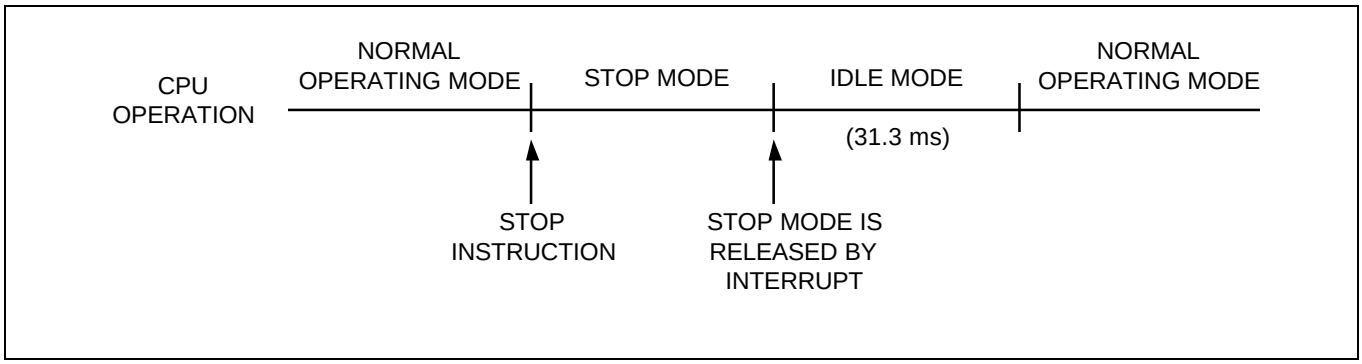
☞ PROGRAMMING TIP — Using the Basic Timer

1. To read the basic timer count register (BCNT):

```
        BITS    EMB
        SMB     15
BCNTR   LD      EA,BCNT
        LD      YZ,EA
        LD      EA,BCNT
        CPSE    EA,YZ
        JR      BCNTR
```

2. When stop mode is released by an interrupt, set the oscillation stabilization interval to 31.3 ms:

```
        BITS    EMB
        SMB     15
        LD      A,#0BH
        LD      BMOD,A          ;  Wait time is 31.3 ms
        STOP                    ;  Set stop power-down mode
        NOP
        NOP
```



3. To set the basic timer interrupt interval time to 1.95 ms (at 4.19 MHz):

```
        BITS    EMB
        SMB     15
        LD      A,#0FH
        LD      BMOD,A
        EI
        BITS    IEB             ;  Basic timer interrupt enable flag is set to "1"
```

4. Clear BCNT and the IRQB flag and restart the basic timer:

```
        BITS    EMB
        SMB     15
        BITS    BMOD.3
```

8-BIT TIMER/COUNTER 0 (TC0)

OVERVIEW

Timer/counter 0 (TC0) is used to count system 'events' by identifying the transition (high-to-low or low-to-high) of incoming square wave signals. To indicate that an event has occurred, or that a specified time interval has elapsed, TC0 generates an interrupt request. By counting signal transitions and comparing the current counter value with the reference register value, TC0 can be used to measure specific time intervals.

TC0 has a reloadable counter that consists of two parts: an 8-bit reference register (TREF0) into which you write the counter reference value, and an 8-bit counter register (TCNT0) whose value is automatically incremented by counter logic.

An 8-bit mode register, TMOD0, is used to activate the timer/counter and to select the basic clock frequency to be used for timer/counter operations. To dynamically modify the basic frequency, new values can be loaded into the TMOD0 register during program execution.

Timer/counter 0 can supply a clock signal to the clock selector circuit of the serial I/O interface for data shifter and clock counter operations. (These internal SIO operations are controlled in turn by the SIO mode register, SMOD). This clock generation function enables you to adjust data transmission rates across the serial interface.

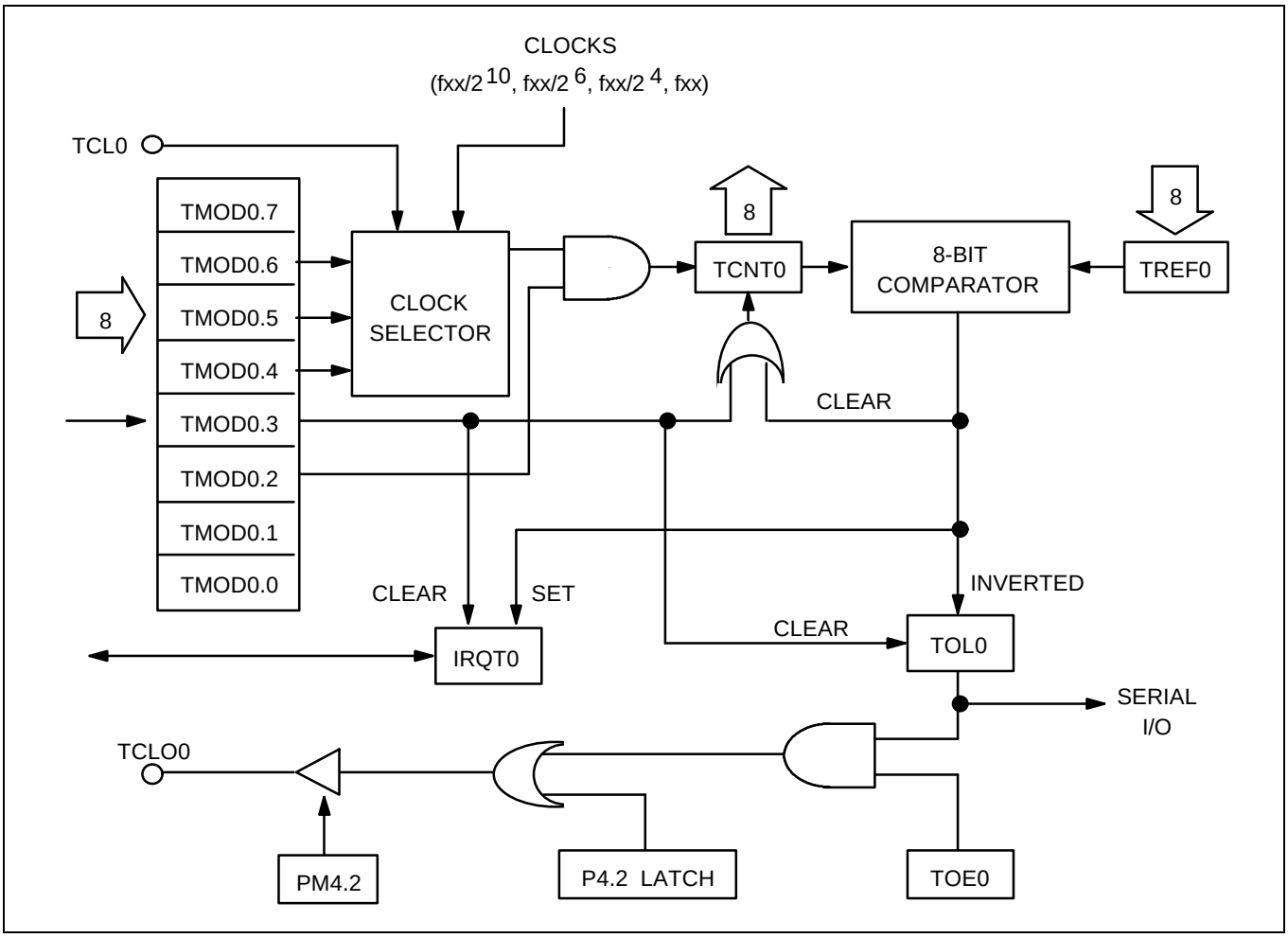


Figure 31. TC0 Circuit Diagram

TC0 PROGRAMMABLE TIMER/COUNTER FUNCTION

Timer/counter 0 can be programmed to generate interrupt requests at various intervals based on the selected system clock frequency. Its 8-bit TC0 mode register TMOD0 is used to activate the timer/counter and to select the clock frequency.

The reference register TREF0 stores the value for the number of clock pulses to be generated between interrupt requests. The counter register, TCNT0, counts the incoming clock pulses, which are compared to the TREF0 value as TCNT0 is incremented. When there is a match (TREF0 = TCNT0), an interrupt request is generated.

To generate an interrupt request, the TC0 interrupt request flag (IRQT0) is set to logic one, the status of TOL0 is inverted, and the interrupt is generated. The content of TCNT0 is then cleared to 00H and TC0 continues counting. The interrupt request mechanism for TC0 includes an interrupt enable flag (IET0) and an interrupt request flag (IRQT0).

TC0 EVENT COUNTER FUNCTION

Timer/counter 0 can monitor or detect system 'events' by using the external clock input at the TCL0 pin as the counter source. The TC0 mode register selects rising or falling edge detection for incoming clock signals. The counter register TCNT0 is incremented each time the selected state transition of the external clock signal occurs.

With the exception of the different TMOD0.4–TMOD0.6 settings, the operation sequence for TC0's event counter function is identical to its programmable timer/counter function. To activate the TC0 event counter function, P4.1/TCL0 must be set to input mode.

.

Table 20-1. TMOD0 Settings for TCL0 Edge Detection

TMOD0.5	TMOD0.4	TCL0 Edge Detection
0	0	Rising edges
0	1	Falling edges

TC0 CLOCK FREQUENCY OUTPUT

Using timer/counter 0, a modifiable clock frequency can be output to the TC0 clock output pin, TCLO0. To select the clock frequency, load the appropriate values to the TC0 mode register, TMOD0. The clock interval is selected by loading the desired reference value into the reference register TREF0. To enable the output to the TCLO0 pin, the following conditions must be met:

— TC0 output enable flag TOE0 must be set to "1"

— I/O mode flag for P4.2 must be set to output mode ("1")

— Output latch value for P4.2 must be set to "0"

☞ PROGRAMMING TIP — TC0 Signal Output to the TCLO0 Pin

Output a 30 ms pulse width signal to the TCLO0 pin:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
LD      EA,#40H
LD      PMG1,EA         ;  P4.2 ← output mode
BITR    P4.2            ;  P4.2 clear
BITS    TOE0
```

TC0 MODE REGISTER (TMOD0)

TMOD0 is the 8-bit mode control register for timer/counter 0. TMOD0.2 is the enable/disable bit for timer/counter 0. When TMOD0.3 is set to "1", the contents of TCNT0, IRQT0, and TOL0 are cleared, counting starts from 00H, and TMOD0.3 is automatically reset to "0" for normal TC0 operation. When TC0 operation stops (TMOD0.2 = "0"), the contents of the TC0 counter register TCNT0 are retained until TC0 is re-enabled.

Table 21. TC0 Mode Register (TMOD0) Organization

Bit Name	Setting	Resulting TC0 Function	Address
TMOD0.7	0	Always logic zero	F91H
TMOD0.6 TMOD0.5 TMOD0.4	0,1	Specify input clock edge and internal frequency	
TMOD0.3	1	Clear TCNT0, IRQT0, and TOL0 and resume counting immediately (This bit is automatically cleared to logic zero immediately after counting resumes.)	F90H
TMOD0.2	0	Disable timer/counter 0; retain TCNT0 contents	
	1	Enable timer/counter 0	
TMOD0.1	0	Always logic zero	
TMOD0.0	0	Always logic zero	

Table 22. TMOD0.6, TMOD0.5, and TMOD0.4 Bit Settings

TMOD0.6	TMOD0.5	TMOD0.4	Resulting Counter Source and Clock Frequency
0	0	0	External clock input (TCL0) on rising edges
0	0	1	External clock input (TCL0) on falling edges
1	0	0	$fxx/2^{10}$ (4.09 kHz)
1	0	1	$fxx/2^{6}$ (65.5 kHz)
1	1	0	$fxx/2^{4}$ (262 kHz)
1	1	1	fxx = 4.19 MHz

NOTE: 'fxx' = selected system clock of 4.19 MHz.

☞ PROGRAMMING TIP — Restarting TC0 Counting Operation

1. Set TC0 timer interval to 4.09 kHz:

```
BITS    EMB
SMB     15
LD      EA,#4CH
LD      TMOD0,EA
EI
BITS    IET0
```

2. Clear TCNT0, IRQT0, and TOL0 and restart TC0 counting operation:

```
BITS    EMB
SMB     15
BITS    TMOD0.3
```

TC0 REFERENCE REGISTER (TREF0)

TREF0 is used to store a reference value to be compared to the incrementing TCNT0 register in order to identify an elapsed time interval. Use the following formula to calculate the correct value to load to the TREF0 reference register:

$$\text{TC0 timer interval} = (\text{TREF0 value} + 1) \times \frac{1}{\text{TMOD0 frequency setting}}$$

(TREF0 value≠0)

TC0 OUTPUT ENABLE FLAG (TOE0)

The 1-bit timer/counter 0 output enable flag TOE0 controls output from timer/counter 0 to the TCLO0 pin.

	(MSB)			(LSB)
F92H	"0"	**TOE0**	"0"	"0"

When you set the TOE0 flag to "1", the contents of TOL0 can be output to the TCLO0 pin.

☞ PROGRAMMING TIP — Setting a TC0 Timer Interval

To set a 30 ms timer interval for TC0, given fxx = 4.19 MHz, follow these steps.

1. Select the timer/counter 0 mode register with a maximum setup time of 62.5 ms (assume the TC0 counter clock = fxx/2^{10}, and TREF0 is set to FFH):

2. Calculate the TREF0 value:

$$30\ \text{ms} = \frac{\text{TREF0 value} + 1}{4.09\ \text{kHz}}$$

$$\text{TREF0} + 1 = \frac{30\ \text{ms}}{244\ \mu\text{s}} = 122.9 = 7\text{AH}$$

$$\text{TREF0 value} = 7\text{AH} - 1 = 79\text{H}$$

3. Load the value 79H to the TREF0 register:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
```

WATCH TIMER

Watch timer functions include real-time and watch-time measurement and interval timing for the main and subsystem clock. It is also used as a clock source for the LCD controller and for generating buzzer (BUZ) output.

Real-Time and Watch-Time Measurement

To start watch timer operation, set bit 2 of the watch timer mode register (WMOD.2) to logic one. The watch timer starts, the interrupt request flag IRQW is automatically set to logic one, and interrupt requests commence in 0.5-second intervals.

Since the watch timer functions as a quasi-interrupt instead of a vectored interrupt, the IRQW flag should be cleared to logic zero by program software as soon as a requested interrupt service routine has been executed.

Using a Main System or Subsystem Clock Source

The watch timer can generate interrupts based on the main system clock frequency or on the subsystem clock. When the zero bit of the WMOD register is set to "1", the watch timer uses the subsystem clock signal (fxt) as its source; if WMOD.0 = "0", the main system clock (fx) is used as the signal source, according to the following formula:

$$\text{Watch timer clock (fw)} = \frac{\text{Main system clock (fx)}}{128}$$
$$= 32.768 \text{ kHz (fx = 4.19 MHz)}$$

This feature is useful for controlling timer-related operations during stop mode. When stop mode is engaged, the main system clock (fx) is halted, but the subsystem clock continues to oscillate. By using the subsystem clock as the oscillation source during stop mode, the watch timer can set the interrupt request flag IRQW to "1", thereby releasing stop mode.

Clock Source Generation for LCD Controller

The watch timer supplies the clock frequency for the LCD controller (f_{LCD}). Therefore, if the watch timer is disabled, the LCD controller does not operate.

Buzzer Output Frequency Generator

The watch timer can generate a steady 2 kHz, 4 kHz, 8 kHz, or 16 kHz signal to the BUZ pin. To select the desired BUZ frequency , load the appropriate value to the WMOD register. This output can then be used to actuate an external buzzer sound. To generate a BUZ signal, three conditions must be met:

— The WMOD.7 register bit is set to "1"

— The output latch for I/O port 0.3 is cleared to "0"

— The port 0.3 output mode flag (PM0.3) set to 'output' mode

Timing Tests in High-Speed Mode

By setting WMOD.1 to "1", the watch timer will function in high-speed mode, generating an interrupt every 3.91 ms. At its normal speed (WMOD.1 = '0'), the watch timer generates an interrupt request every 0.5 seconds. High-speed mode is useful for timing events for program debugging sequences.

Check Subsystem Clock Level Feature

The watch timer can also check the input level of the subsystem clock by testing WMOD.3. If WMOD.3 is "1", the input level at the XT_{in} pin is high; if WMOD.3 is "0", the input level at the XT_{in} pin is low.

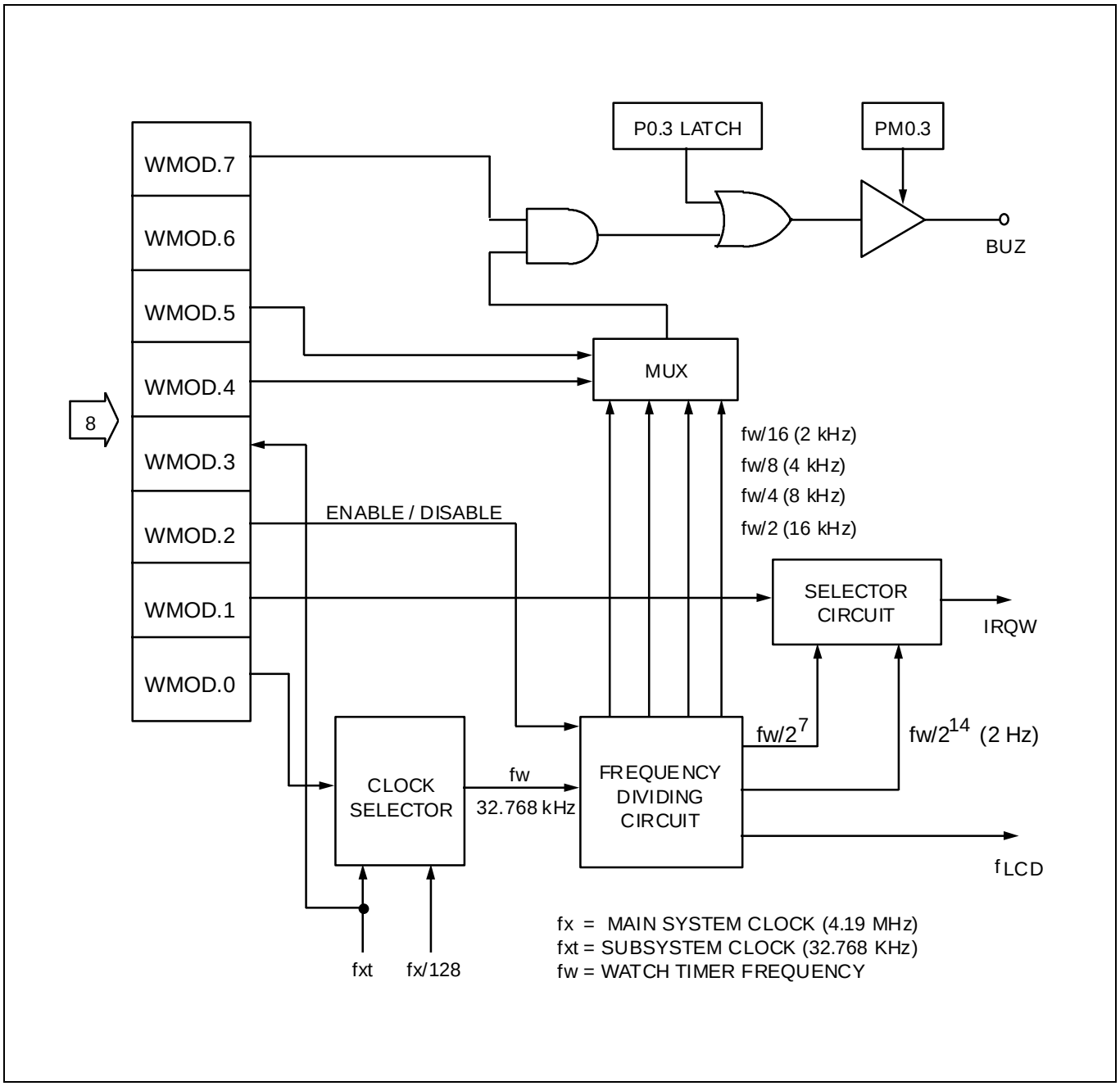


Figure 32. Watch Timer Circuit Diagram

WATCH TIMER MODE REGISTER (WMOD)

The watch timer mode register WMOD is used to select specific watch timer operations.

Table 23. Watch Timer Mode Register (WMOD) Organization

Bit Name	Values		Function	Address
WMOD.7	0		Disable buzzer (BUZ) signal output	F89H
	1		Enable buzzer (BUZ) signal output	
WMOD.6	0		Always logic zero	
WMOD.5 – .4	0	0	2 kHz buzzer (BUZ) signal output	
	0	1	4 kHz buzzer (BUZ) signal output	
	1	0	8 kHz buzzer (BUZ) signal output	
	1	1	16 kHz buzzer (BUZ) signal output	
WMOD.3	0		Input level to XT_{in} pin is low	F88H
	1		Input level to XT_{in} pin is high	
WMOD.2	0		Disable watch timer; clear frequency dividing circuits	
	1		Enable watch timer	
WMOD.1	0		Normal mode; sets IRQW to 0.5 seconds	
	1		High-speed mode; sets IRQW to 3.91 ms	
WMOD.0	0		Select (fx/128) as the watch timer clock (fw)	
	1		Select subsystem clock as watch timer clock (fw)	

NOTE: Main system clock frequency (fx) is assumed to be 4.19 MHz; subsystem clock (fxt) is assumed to be 32.768 kHz.

☞ PROGRAMMING TIP — Using the Watch Timer

1. Select a subsystem clock as the LCD display clock, a 0.5 second interrupt, and 2 kHz buzzer enable:

```
BITS    EMB
SMB     15
LD      EA,#8H
LD      PMG1,EA          ;  P0.3 ← output mode
BITR    P0.3
LD      EA,#85H
LD      WMOD,EA
BITS    IEW
```

2. Sample real-time clock processing method:

```
CLOCK   BTSTZ   IRQW      ;  0.5 second check
        RET               ;  No, return
        •                 ;  Yes, 0.5 second interrupt generation
        •
        •                 ;  Increment HOUR, MINUTE, SECOND
```

LCD CONTROLLER/DRIVER

The S3C7254 microcontroller can directly drive an up-to-320–dot (40 segments x 8 commons) LCD panel.

Data written to the LCD display RAM can be transferred to the segment signal pins automatically without program control.

When a subsystem clock is selected as the LCD clock source, the LCD display is enabled even during main clock stop and idle modes.

LCD RAM ADDRESS AREA

RAM addresses of bank 1 are used as LCD data memory. These locations can be addressed by 1-bit, 4-bit, or 8-bit instructions. When the bit value of a display segment is "1", the LCD display is turned on; when the bit value is "0", the display is turned off.

Display RAM data are sent out through segment pins SEG0–SEG40 using a direct memory access (DMA) method that is synchronized with the f_{LCD} signal. RAM addresses in this location that are not used for LCD display can be allocated to general-purpose use.

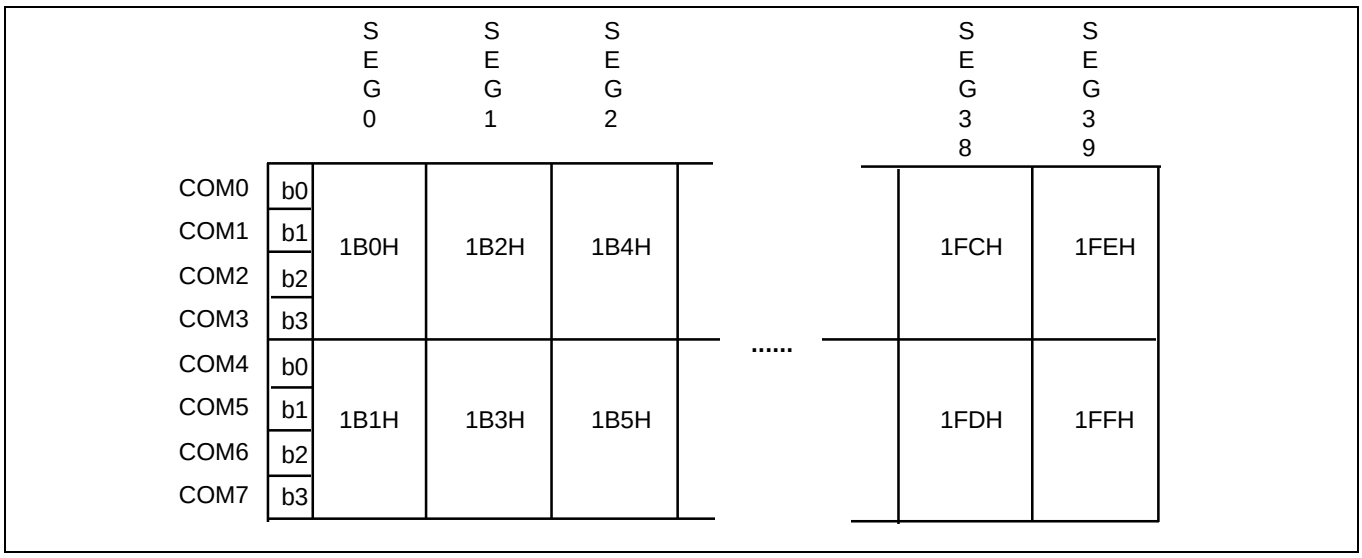


Figure 33. LCD Display Data RAM Organization

Table 24. Common and Segment Pins per Duty Cycle

Duty	Common Pins	Segment Pins	Dot Number
1/8	COM0–COM7	32–40 pins	256 dots–320 dots
1/4	COM0–COM3		128 dots–160 dots
1/3	COM0–COM2		96 dots–120 dots

1-BIT OUTPUT

The eight output pins (P5.0-P5.7) of the 40-segment output pins can be set in 4 bits for 1-bit level output by LMOD.6 and LMOD.7. At this time, the bit 0 of the even addressed display RAM is used as the output latch of 1-bit output pins. The 1F0H.0 in LCD display RAM is used as the output latch for P5.0, 1F2H.0 is for P5.1,…… and 1FEH.0 is for P5.7. These 1-bit output pins cannot be used as 4 bits and 8 bits.

LCD CIRCUIT DIAGRAM

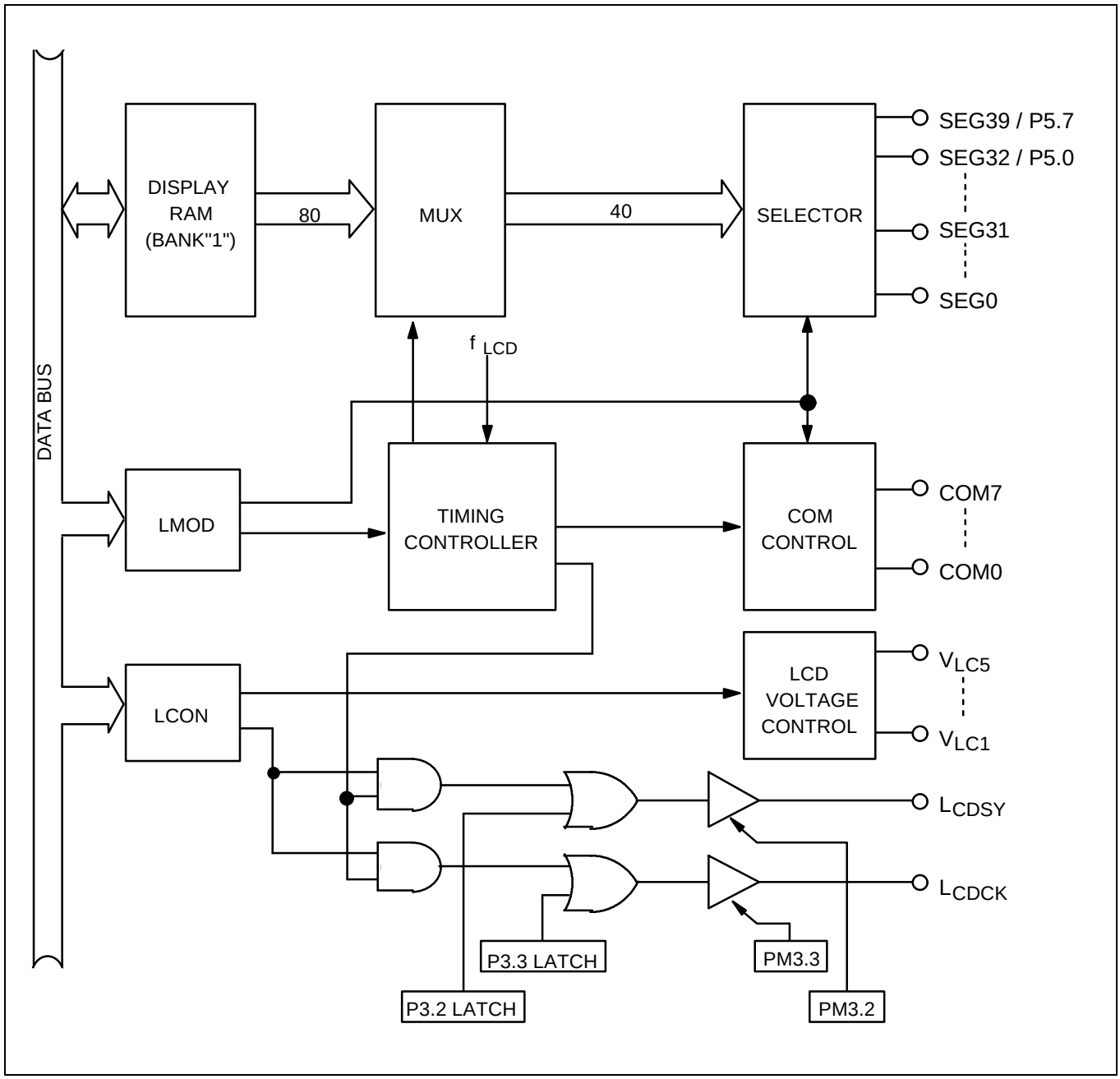


Figure 34. LCD Circuit Diagram

LCD CONTROL REGISTER (LCON)

The LCD control register (LCON) is used to turn the LCD display on and off, to output LCD clock (LCDCK) and synchronizing signal (LCDSY) for LCD display expansion, and to control the flow of current to dividing resistors in the LCD circuit. The effect of the LCON.0 setting is dependent upon the current setting of bits LMOD.0 and LMOD.1.

Table 25. LCD Control Register (LCON) Organization

LCON Bit	Setting	Description
LCON.3	0	1/4 bias select
	1	1/3 bias select
LCON.2	0	Disable LCDCK and LCDSY signal outputs.
	1	Enable LCDCK and LCDSY signal outputs.
LCON.1, LCON.0	0,0	LCD display off
	1,0	LCD display on when using an external resistor for contrast control.
	1,1	LCD display on when not using an external resistor for contrast control.

NOTES:
1. In case of LCON.0, you should turn on/off ‘LCD display’ using internal resistor. If you want to turn on/off LCD or to control ‘LCD contrast’’ internally, you should set the LCON.0 to “0”.
2. To select LCD bias, you must use both the LCON.3 setting and an external LCD bias circuit connection.
3. If you turn the LCD display off (LCON.0 = "0"), you reduce the current flowing through the LCD dividing resistorrs.

Table 26. LMOD.1–0 Bits Settings

LMOD.1–LMOD.0	COM0–COM 7	SEG0–SEG39	SEG32/P5.0–SEG39/P5.7	Power Supply to the Dividing Resistor
0, 0	All of the LCD dots off		1-bit output function	On
0, 1	All of the LCD dots on			
1, 0	Common and segment signal output corresponds to display data (normal display mode)			

LCD MODE REGISTER (LMOD)

The LCD mode control register LMOD is used to control display mode; LCD clock, segment or port output, and display on/off. LMOD can be manipulated using 8-bit write instructions.

The LCD clock signal, LCDCK, determines the frequency of COM signal scanning of each segment output. This is also referred to as the 'frame frequency. Since LCDCK is generated by dividing the watch timer clock (fw), **the watch timer must be enabled when the LCD display is turned on.**

The LCD display can continue to operate during idle and stop modes if a subsystem clock is used as the watch timer source. The LCD mode register LMOD controls the output mode of the 8 pins used for normal outputs (P5.0–P5.7). Bits LMOD.7–5 define the segment output and normal bit output configuration.

Table 27. LCD Clock Signal (LCDCK) Frame Frequency

LCDCK Display Duty Cycle	128 Hz	256 Hz	512 Hz	1024 Hz	2048 Hz	4096 Hz
1/8	–	–	64 Hz	128 Hz	256 Hz	512 Hz
1/4	–	64 Hz	128 Hz	256 Hz	512 Hz	–
1/3	42.7 Hz	85.3 Hz	170.7 Hz	341.3 Hz	–	–

NOTE: fw = 32.768 kHz

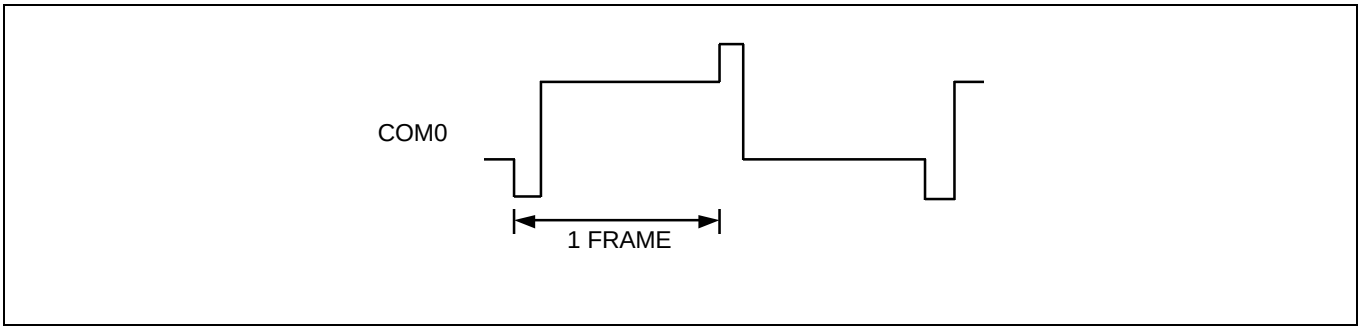


Table 28. LCD Mode Register (LMOD) Organization

Segment /Output Port Selection Bits

LMOD.7	LMOD.6	SEG39–36	SEG35–32	Total Number of Segment
0	0	SEG port	SEG port	40
0	1	SEG port	Output port	36
1	0	Output port	SEG port	36
1	1	Output port	Output port	32

LCD Clock Selection Bits

LMOD.5	LMOD.4	LCD Clock (LCDCK)		
		1/8 duty (COM0–COM7)	1/4 duty (COM0–COM3)	1/3 duty (COM0–COM2)
0	0	fw/ 2^6 (512 Hz)	fw/ 2^7 (256 Hz)	fw/ 2^8 (128 Hz)
0	1	fw/ 2^5 (1024 Hz)	fw/ 2^6 (512 Hz)	fw/ 2^7 (256 Hz)
1	0	fw/ 2^4 (2048 Hz)	fw/ 2^5 (1024 Hz)	fw/ 2^6 (512 Hz)
1	1	fw/ 2^3 (4096 Hz)	fw/ 2^4 (2048 Hz)	fw/ 2^5 (1024 Hz)

NOTE: LCDCK is supplied only when the watch timer operates. To use the LCD controller, bit 2 in the watch mode register WMOD should be set to 1.

Duty Selection Bits

LMOD.3	LMOD.2	Duty
0	0	1/8 duty (COM0–COM7 select)
1	0	1/4 duty (COM0–COM3 select)
1	1	1/3 duty (COM0–COM2 select)

Display Mode Selection Bits

LMOD.1	LMOD.0	Function
0	0	All LCD dots off
0	1	All LCD dots on
1	0	Normal display

LCD VOLTAGE DIVIDING RESISTORS

On-chip voltage dividing resistors for the LCD drive power supply can be configured by mask option to the V_{LC1}–V_{LC5} pins. Power can be supplied without an external dividing resistor. Figure 12–4 shows the bias connections for the S3C7254 LCD drive power supply.

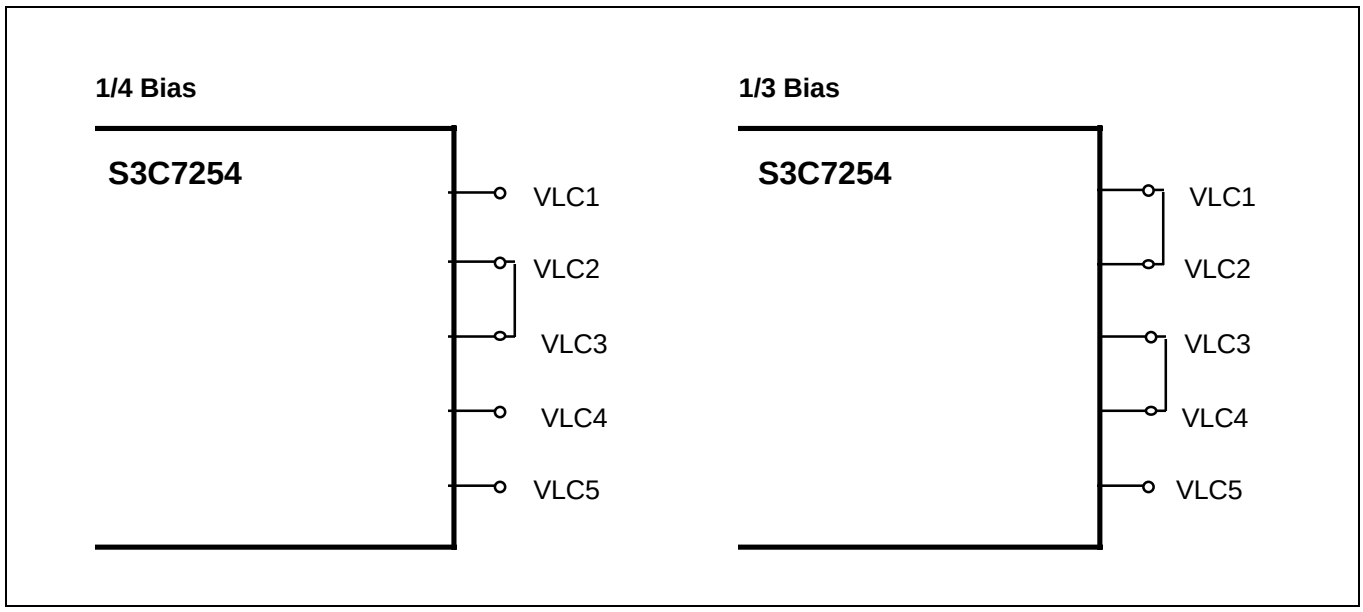


Figure 35. LCD Bias Circuit Connection

APPLICATION WITHOUT CONTRAST CONTROL

If you use an internal transistor (LCON.0) to turn on/off 'LCD display', you can get a merit that peripheral circuits are simple. But in that case, you can't control LCD contrast.

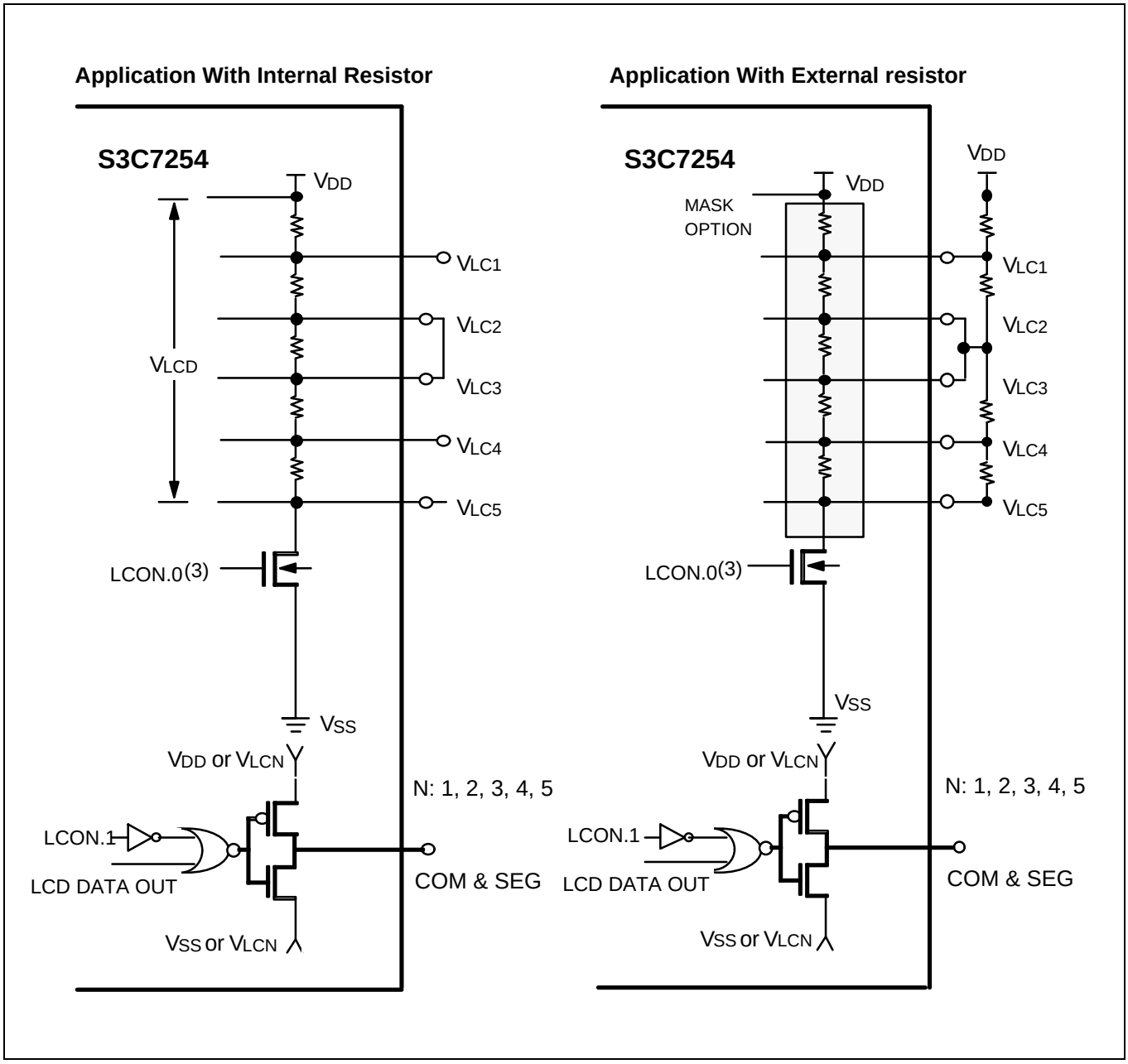


Figure 36. Connection For LCD On/Off Using Internal Transistor

NOTES:
1. A 1/4 bias is assumed for the above circuits; a 1/3 bias is assumed for Figure 35.
2. When you turn off the LCD display using LCON settings, the amount of current flowing through the dividing resistors is reduced more than when you use LMOD to turn off the display.
3. When LCON.0–.1 = #00B, LCD display is turned off. When LCON.0–.1 = #11B, LCD display is turned on.

APPLICATION WITH CONTRAST CONTROL

If you turn on/off 'LCD display' using external output pin, you can control LCD contrast using variable resistor.

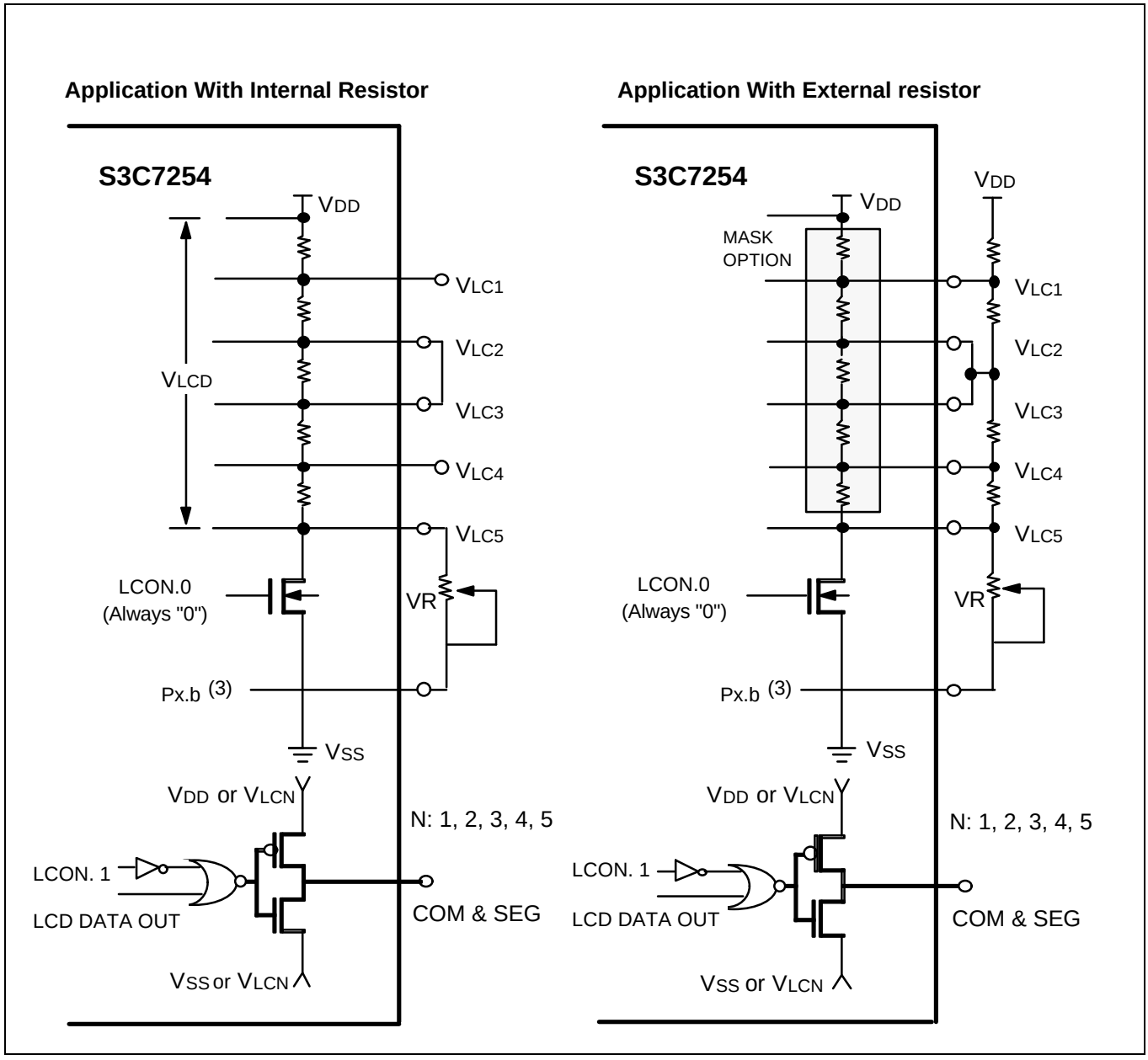


Figure 37. Connection For LCD On/Off Using External Output Pin

NOTES:
1. A 1/4 bias is assumed for the above circuits; a 1/3 bias is assumed for Figure 35.
2. When you turn off the LCD display using LCON settings, the amount of current flowing through the dividing resistors is reduced more than when you use LMOD to turn off the display.
3. When LCON.0–.1 = #00B and Px.b = #1B, LCD display is turned off.
   When LCON.0–.1 = #10B and Px.b = #0B, LCD display is turned on.

COMMON (COM) SIGNALS

The common signal output pin selection (COM pin selection) varies according to the selected duty cycle.

— In 1/8 duty mode, COM0–COM7 pins are selected
— In 1/4 duty mode, COM0–COM3 pins are selected
— In 1/3 duty mode, COM0–COM2 pins are selected

SEGMENT (SEG) SIGNALS

The 40 LCD segment signal pins are connected to corresponding display RAM locations at bank 1. Bits of the display RAM are synchronized with the common signal output pins.

When the bit value of a display RAM location is "1", a select signal is sent to the corresponding segment pin. When the display bit is "0", a 'no-select' signal is sent to the corresponding segment pin.

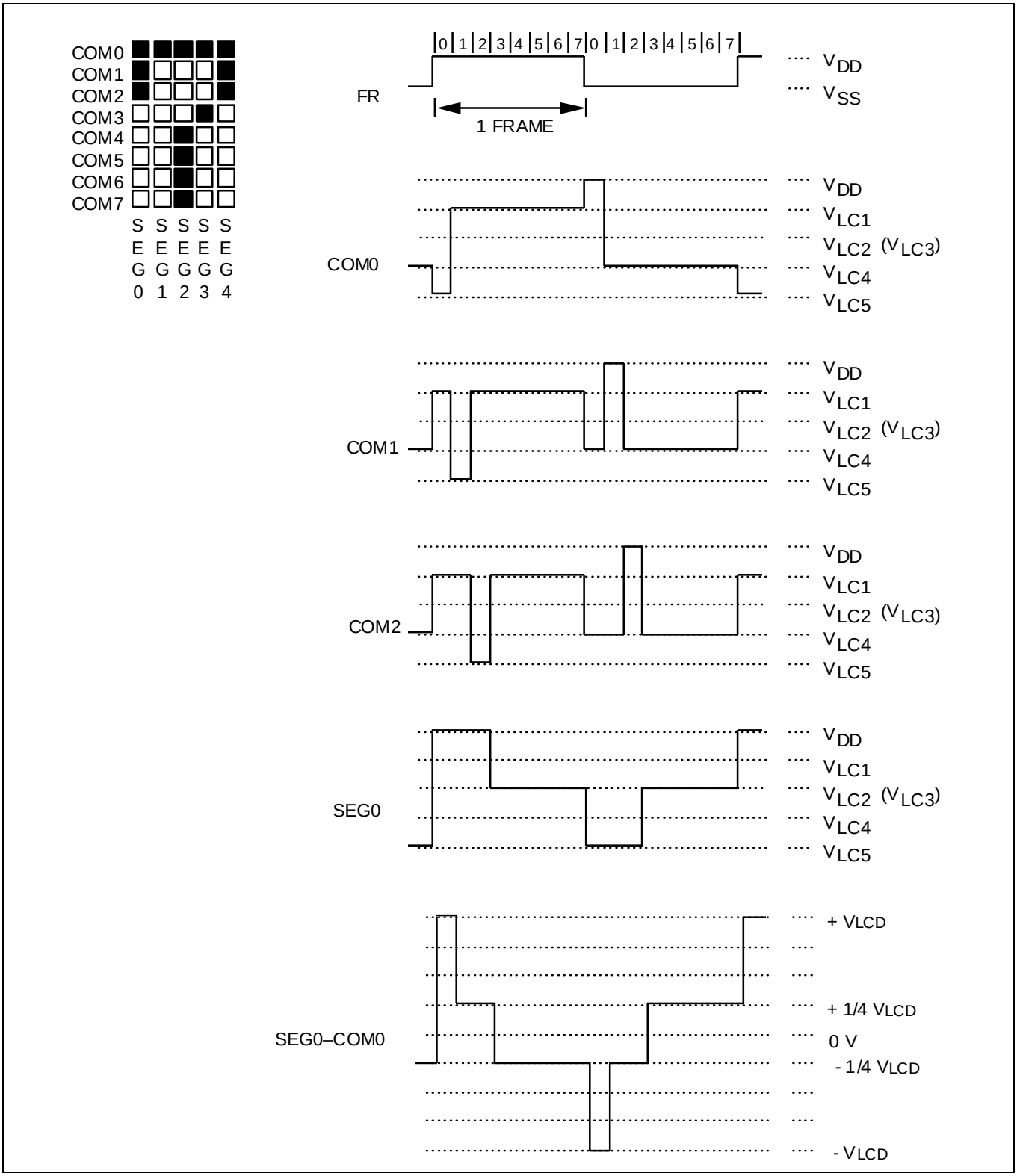


Figure 38. LCD Signal Waveforms (1/8 Duty, 1/4 Bias)

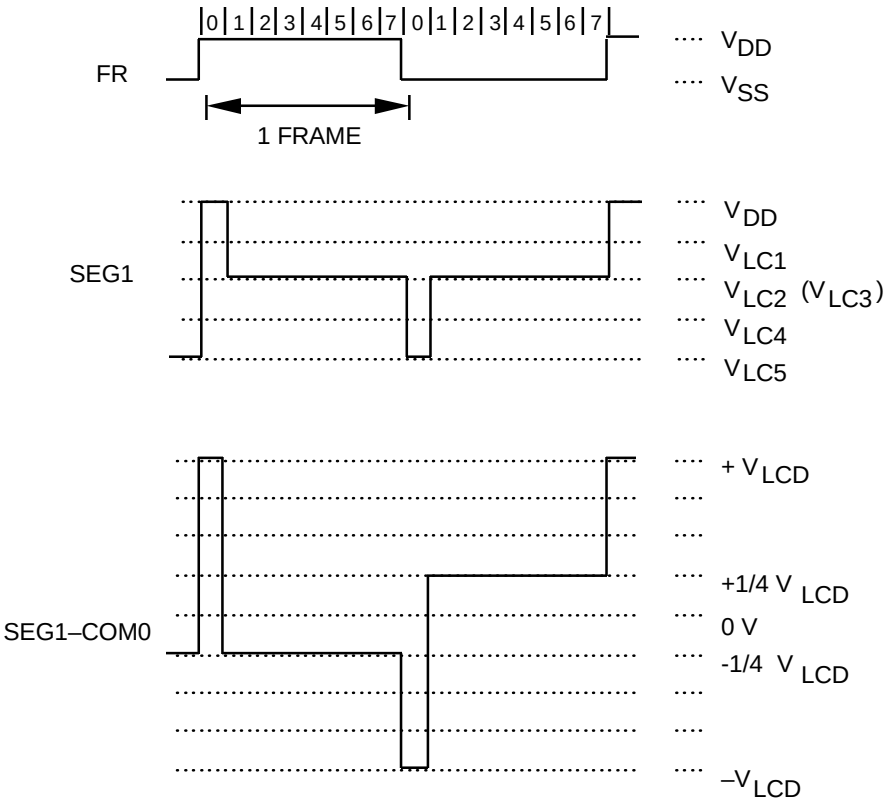


Figure 39. LCD Signal Waveforms (1/8 Duty, 1/4 Bias) (Continued)

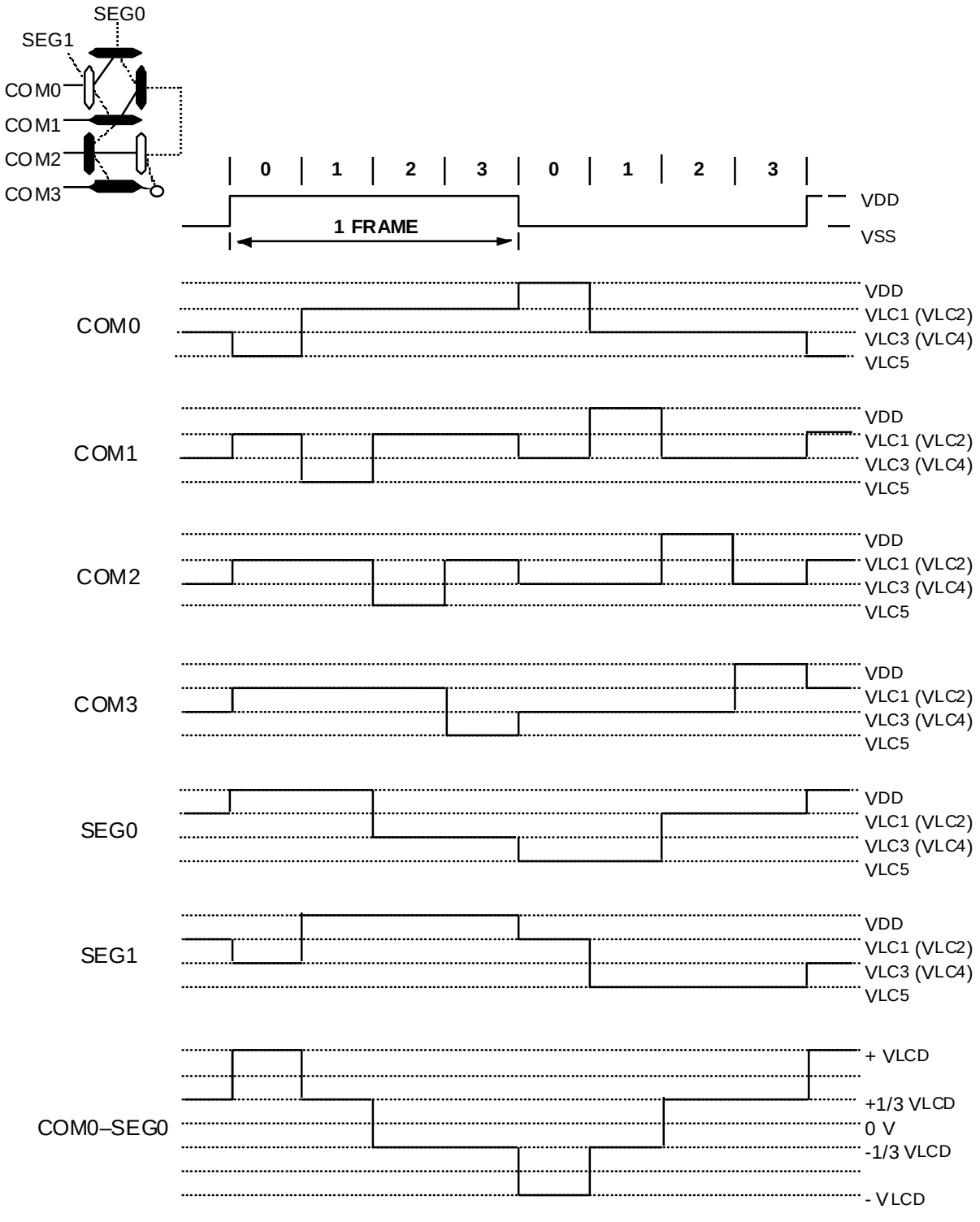


Figure 40. LCD Signal Waveforms (1/4 Duty, 1/3 Bias)

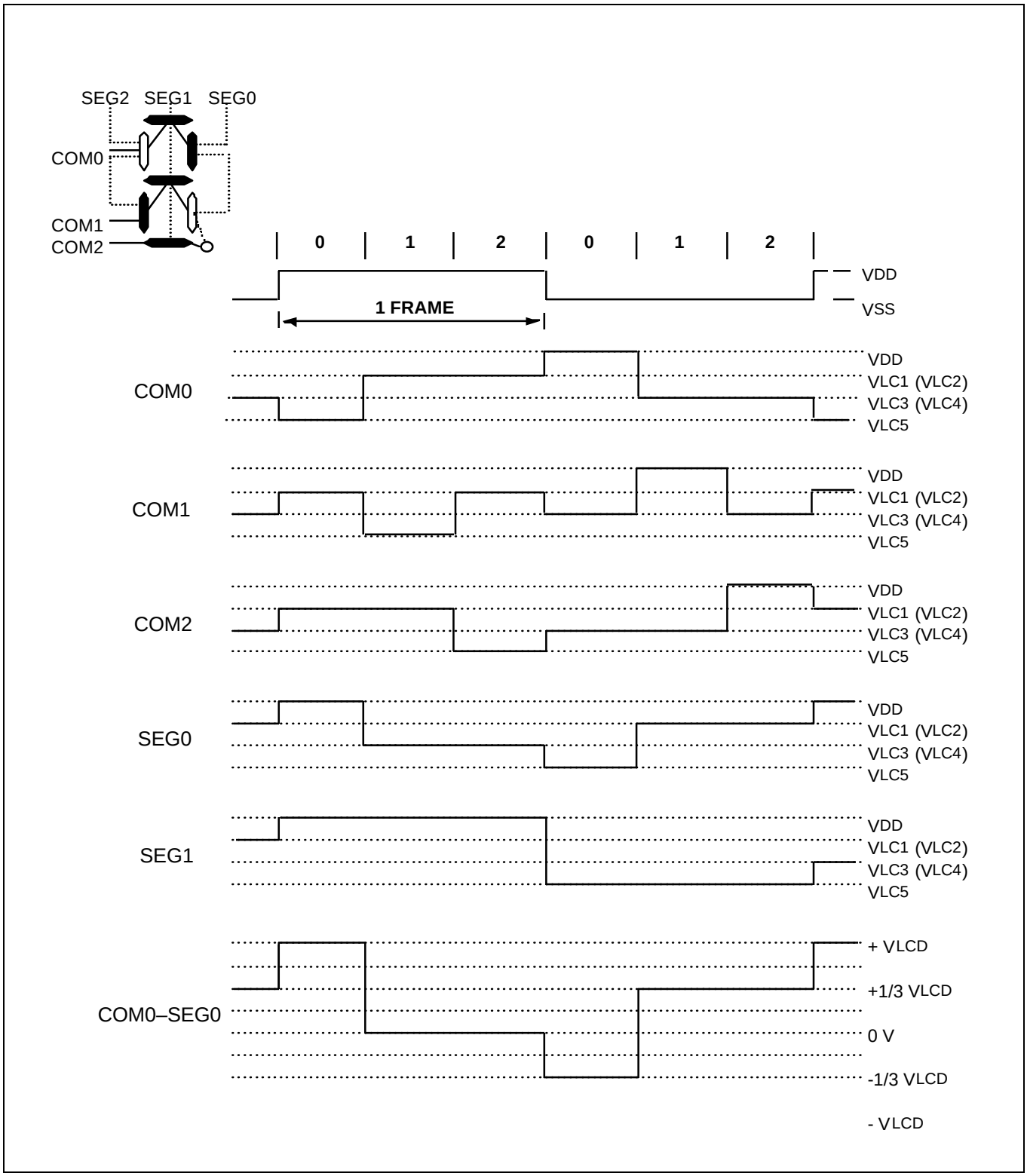
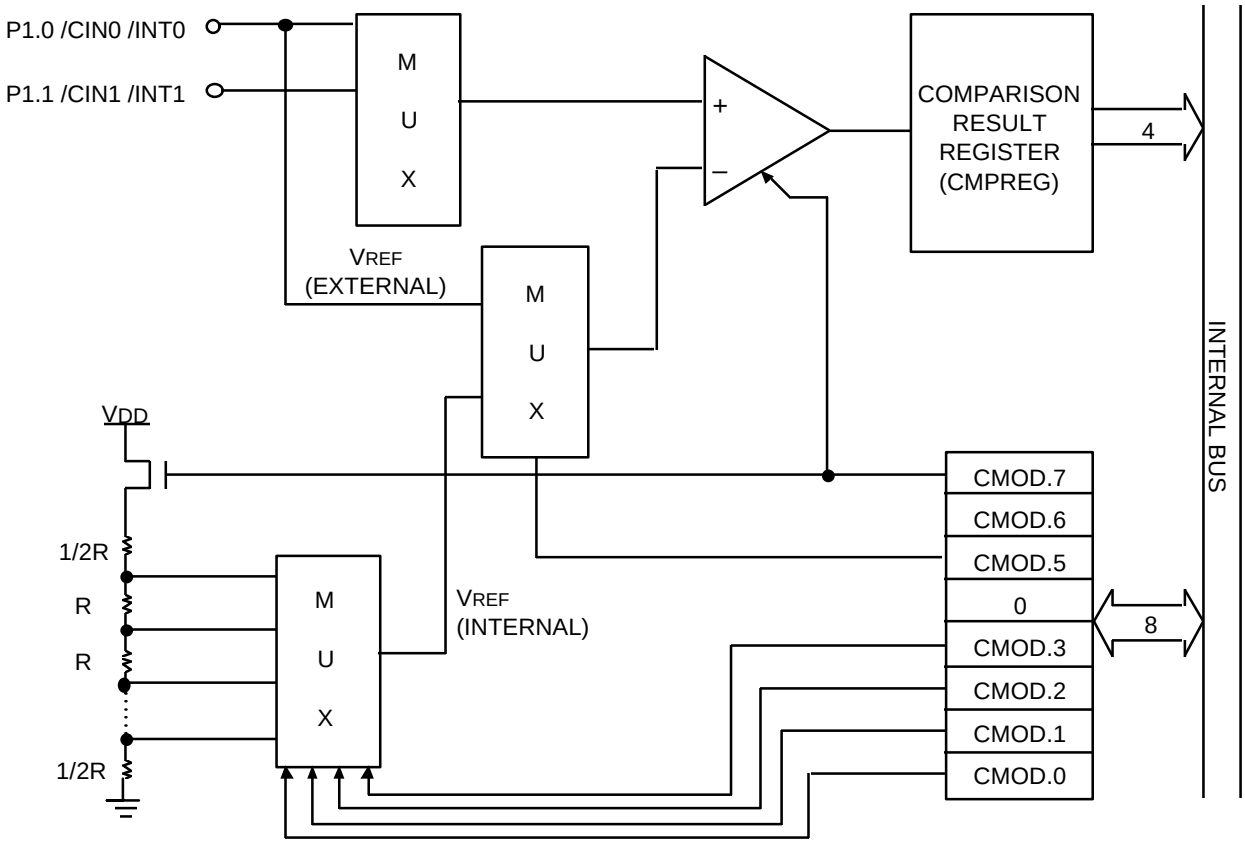


Figure 41. LCD Signal Waveforms (1/3 Duty, 1/3 Bias)

COMPARATOR

P1.0 and P1.1 can be used as a analog input port for a comparator. The reference voltage for the 2-channel comparator can be supplied either internally or externally at P1.0. When an internal reference voltage is used, two channels (P1.0–P1.1) are used for analog inputs and the internal reference voltage is varied in 16 levels. If an external reference voltage is input at P1.0, the other P1.1 pins are used for analog input.

When a conversion is completed, the result is saved in the comparison result register CMPREG. The initial values of the CMPREG are undefined and the comparator operation is disabled by a RESET. The comparator module has the following components:



Note: INT occures only for digital input selecting: for analog input, any INT doesn't.

Figure 42. Comparator Circuit Diagram

COMPARATOR MODE REGISTER (CMOD)

The comparator mode register CMOD is an 8-bit register that is used to select the operation mode of the comparator.

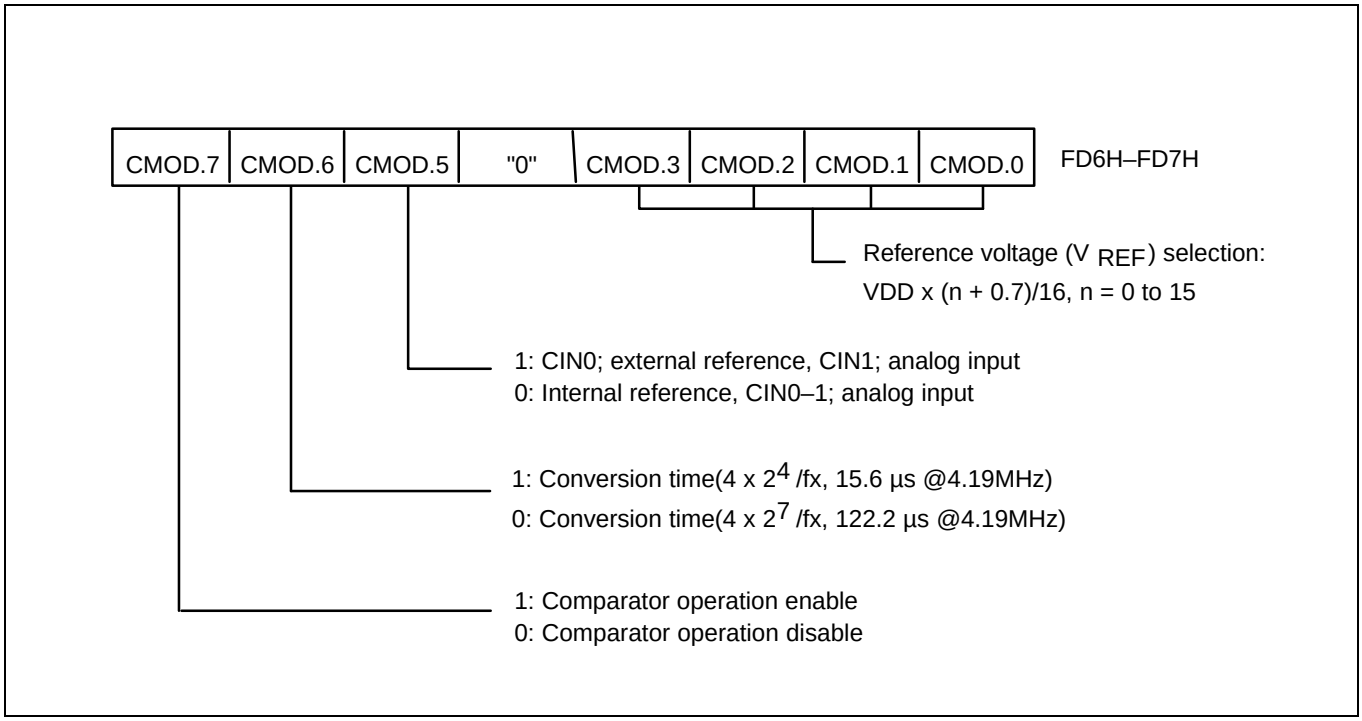


Figure 43. Comparator Mode Register (CMOD) Organization

PORT 1 MODE REGISTER (P1MOD)

P1MOD register settings determine if P1.0 and P1.1 are used for analog or digital input. The P1MOD register is 4-bit write-only register. P1MOD is mapped to address FE2H. A reset operation initializes all P1MOD register values to zero, configuring P1.0 and P1.1 as a analog input port.

COMPARATOR OPERATION

The comparator compares analog voltage input at CIN0-CIN1 with an external or internal reference voltage (V_{REF}) that is selected by the CMOD register. The result is written to the comparison result register CMPREG at address FD4H. The comparison result at internal reference is calculated as follows:

If "1" Analog input voltage >=V_{REF} + 150 mV

If "0" Analog input voltage <= V_{REF} – 150 mV

To obtain a comparison result, the data must be read out from the CMPREG register after V_{REF} is updated by changing the CMOD value after a conversion time has elapsed.

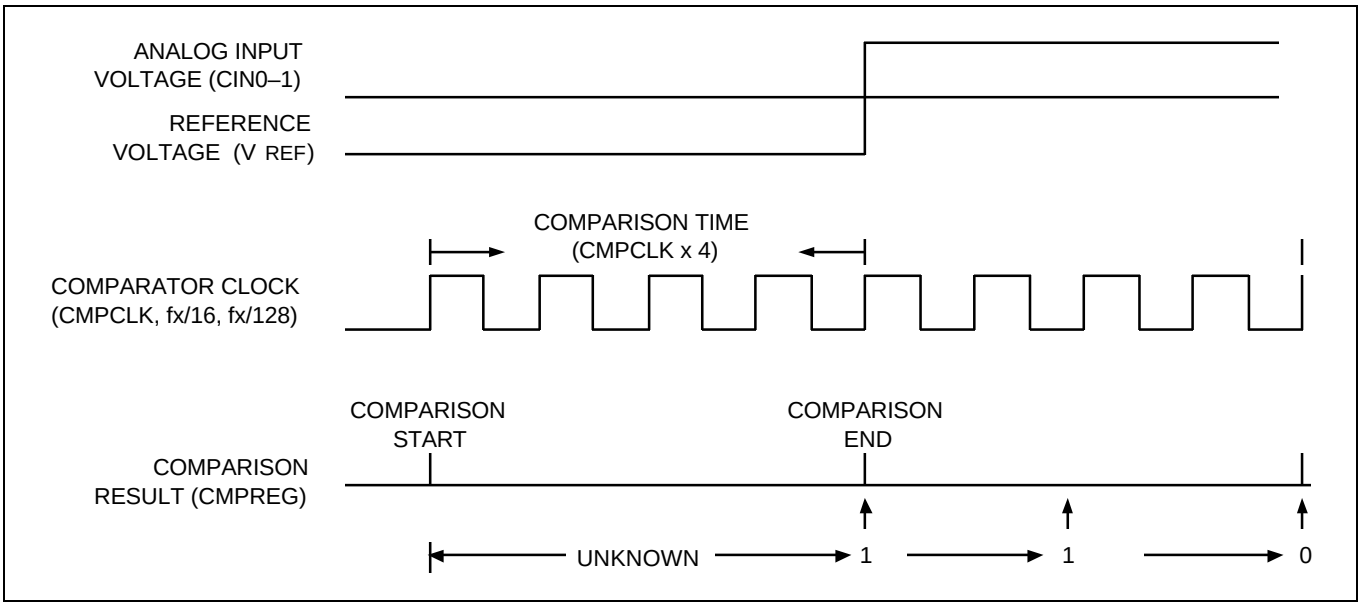


Figure 44. Conversion Characteristics

☞ PROGRAMMING TIP — Programming the Comparator

The following code converts the analog voltage input at the CIN0–CIN1 pins into 4-bit digital code.

```
        BITR    EMB
        LD      A,#3H
        LD      P1MOD,A         ;  Analog input selection (CIN0–CIN1)
        LD      EA,#0CXH        ;  x = 0–F, comparator enable
                                ;  Internal reference, conversion time (15.6 µs at 4.19 MHz)
        LD      CMOD,EA
        LD      A,#0H
WAIT    INCS    A
        JR      WAIT
        LD      A,CMPREG        ;  Read the result
        LD      P2,A            ;  Output the result from port 2
```

SERIAL I/O INTERFACE

Using the serial I/O interface, 8-bit data can be exchanged with an external device. The transmission frequency is controlled by making the appropriate bit settings to the SMOD register.

The serial interface can run off an internal or an external clock source, or the TOL0 signal that is generated by the 8-bit timer/counter, TC0. If the TOL0 clock signal is used, you can modify its frequency to adjust the serial data transmission rate.

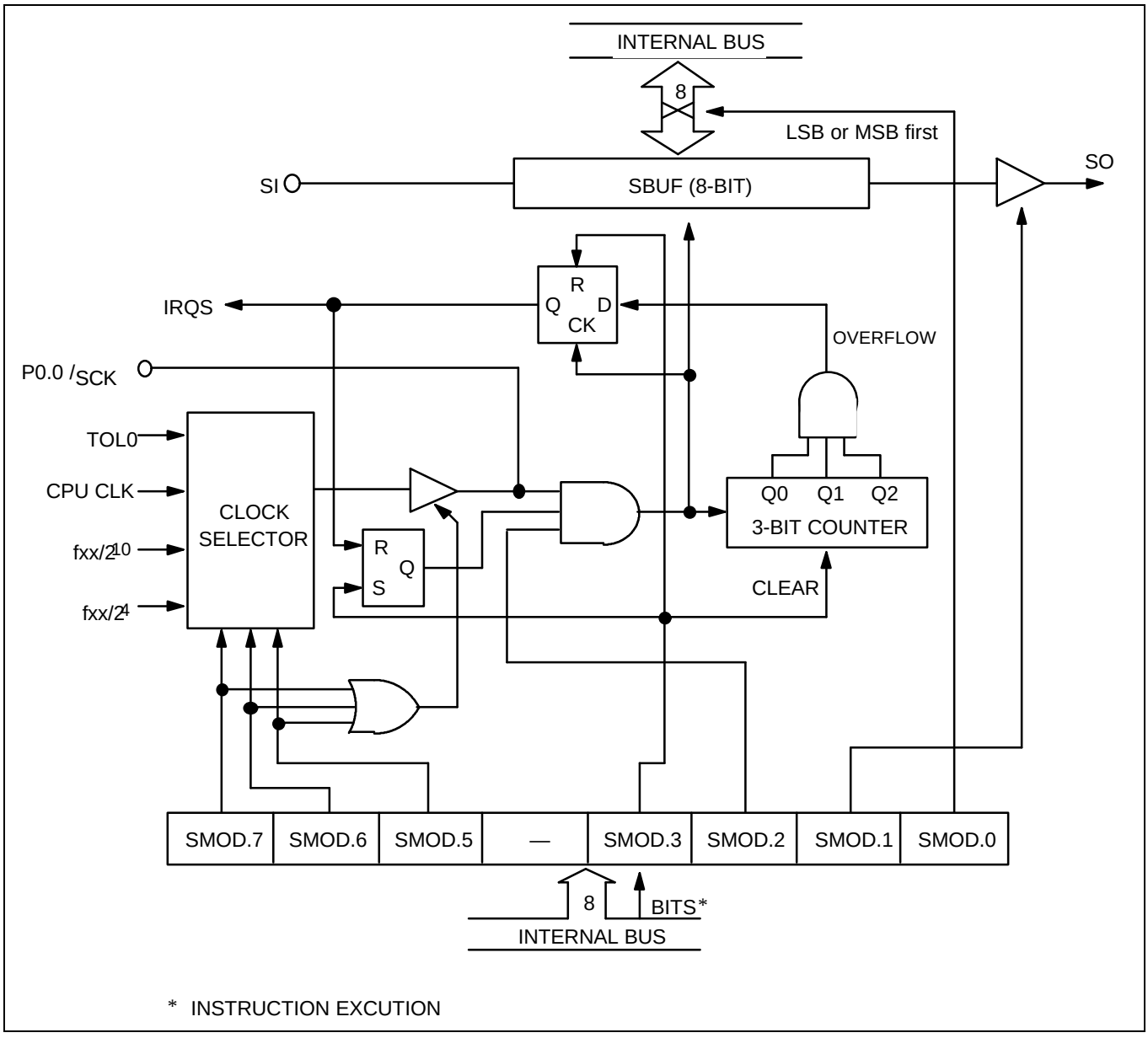


Figure 45. Serial I/O Interface Circuit Diagram

SERIAL I/O MODE REGISTER (SMOD)

The serial I/O mode register, SMOD, is an 8-bit register that specifies the operation mode of the serial interface. Its reset value is logical zero. SMOD is organized in two 4-bit registers, as follows:

SMOD register settings enable you to select either MSB-first or LSB-first serial transmission, and to operate in transmit-and-receive mode or receive-only mode. SMOD is a write-only register and can be addressed only by 8-bit RAM control instructions. One exception to this is SMOD.3, which can be written by a 1-bit RAM control instruction. When SMOD.3 is set to 1, the contents of the serial interface interrupt request flag, IRQS, and the 3-bit serial clock counter are cleared, and SIO operations are initiated. When the SIO transmission starts, SMOD.3 is cleared to logical zero.

Table 29. SIO Mode Register (SMOD) Organization

SMOD.0	0	Most significant bit (MSB) is transmitted first
	1	Least significant bit (LSB) is transmitted first
SMOD.1	0	Receive-only mode
	1	Transmit-and-receive mode
SMOD.2	0	Disable the data shifter and clock counter; retain contents of IRQS flag when serial transmission is halted
	1	Enable the data shifter and clock counter; set IRQS flag to "1" when serial transmission is halted
SMOD.3	1	Clear IRQS flag and 3-bit clock counter to "0"; initiate transmission and then reset this bit to logic zero
SMOD.4	0	Bit not used; value is always "0"

SMOD.7	SMOD.6	SMOD.5	Clock Selection	R/W Status of SBUF
0	0	0	External clock at SCK pin	SBUF is enabled when SIO operation is halted or when SCK goes high.
0	0	1	Use TOL0 clock from TC0	
0	1	x	CPU clock: fxx/4, fxx/8, fxx/64	Enable SBUF read/write
1	0	0	4.09 kHz clock: $fxx/2^{10}$	SBUF is enabled when SIO operation is halted or when SCK goes high.
1	1	1	262 kHz clock: $fxx/2^4$	

NOTES:
1. 'fxx' = system clock; 'x' means 'don't care.'
2. kHz frequency ratings assume a system clock (fxx) running at 4.19 MHz.
3. The SIO clock selector circuit cannot select a $fxx/2^4$ clock if the CPU clock is fxx/64.

SERIAL I/O TIMING DIAGRAMS

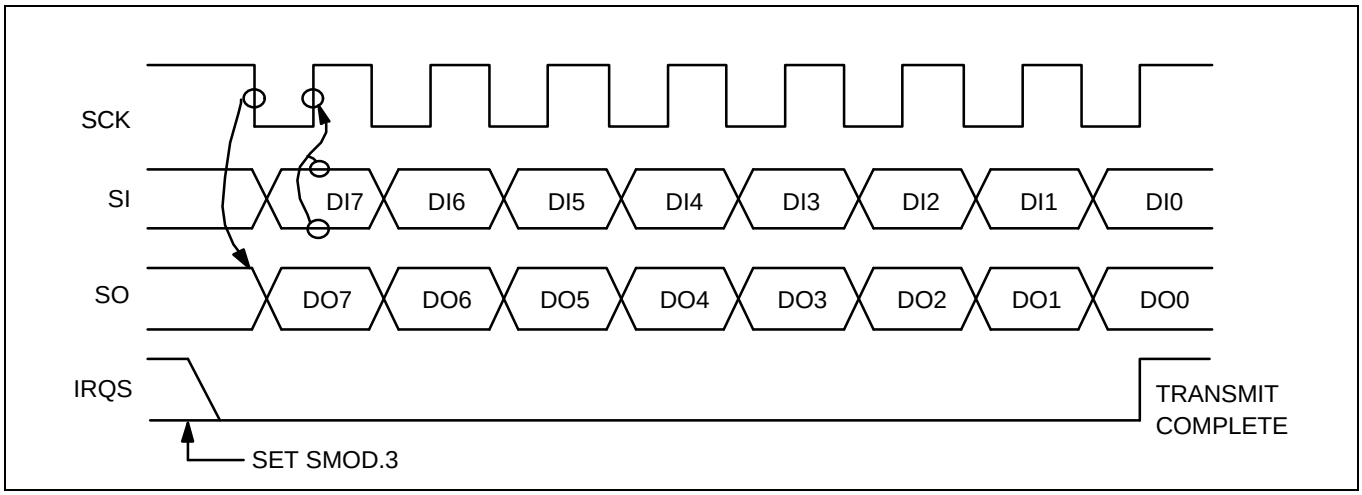


Figure 46. SIO Timing in Transmit/Receive Mode

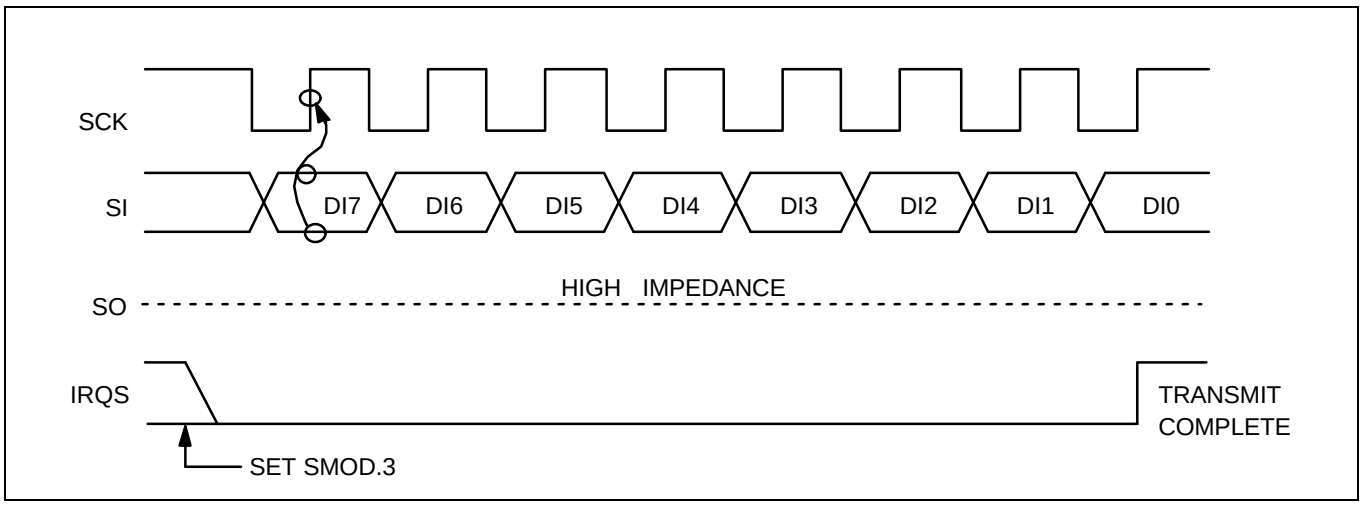
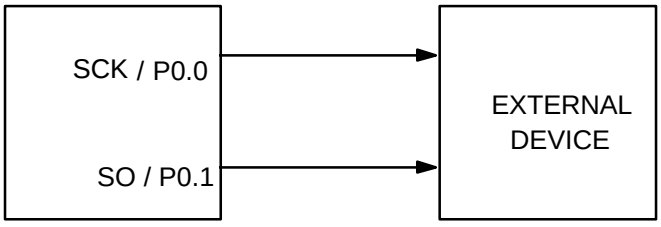


Figure 47. SIO Timing in Receive-Only Mode

☞ PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O

1. Transmit the data value 48H through the serial I/O interface using an internal clock frequency of fxx/2^4 and in MSB-first mode:

```
        BITS    EMB
        SMB     15
        LD      EA,#03H
        LD      PMG1,EA     ;  P0.0 / SCK and P0.1 / SO ← Output
        LD      EA,#48H     ;
        LD      SBUF,EA     ;
        LD      EA,#0EEH
        LD      SMOD,EA     ;  SIO data transfer
```



S3C7254

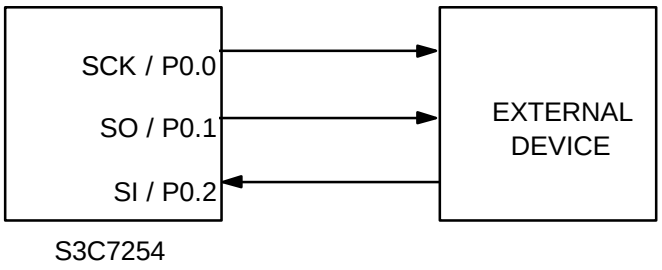
2. Use CPU clock to transfer and receive serial data at high speed:

```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA     ;  P0.0 / SCK and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA    ;  TDATA address = BANK0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#4FH
        LD      SMOD,EA     ;  SIO start
        BITR    IES
STEST   BTSTZ   IRQS
        JR      STEST
        LD      EA,SBUF
        LD      RDATA,EA    ;  RDATA address = BANK0 (20H–7FH)
```

☞ PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)

3. Transmit and receive an internal clock frequency of 4.09 kHz (at 4.19 MHz) in LSB-first mode:

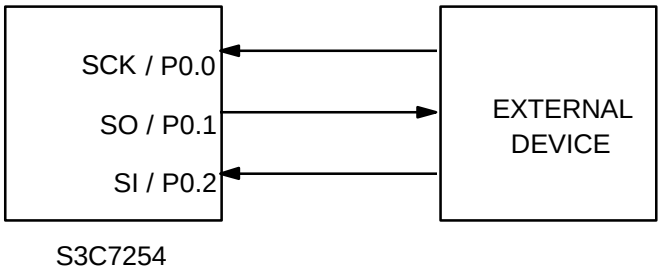
```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ; P0.0 / SCK and P0.1 / SO ← Output, P0.2/SI ← Input
        LD      EA,TDATA        ; TDATA address = BANK0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#8FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES
        .
        .
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data,
                                ; TDATA address = BANK0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ↔ Receive data
        LD      RDATA,EA        ; RDATA address = BANK0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```



☞ PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)

4. Transmit and receive an external clock in LSB-first mode:

```
        BITR    EMB
        LD      EA,#02H
        LD      PMG1,EA         ; P0.1 / SO ← Output, P0.0 / SCK and P0.2 / SI ← Input
        LD      EA,TDATA        ; TDATA address = BANK0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#0FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES
        .
        .
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data,
                                ; TDATA address = BANK0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ← Receive data
        LD      RDATA,EA        ; RDATA address = BANK0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```



High Speed SIO Transmission

ELECTRICAL DATA

Table 30. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 7.0	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value)	mA
			+ 15 note	
		All I/O port, total	+ 100 (Peak value)	
			+ 60 note	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 31. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 2, 3, P4.0 and P4.2	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, P4.1 and RESET	0.8 V_{DD}	–	V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT} and XT_{IN}	V_{DD} – 0.5	–	V_{DD}	
Input Low Voltage	V_{IL1}	Ports 2, 3, P4.0 and P4.2	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, P4.1 and RESET	–	–	0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT} and XT_{IN}	–	–	0.4	
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 3 mA Ports 0, 2, 3 and 4	V_{DD} – 2.0	V_{DD} – 0.4	–	V
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 100 µA Port 5	V_{DD} – 2.0	–	–	
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Ports 0, 2, 3 and 4	–	0.4	2	V
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 100 µA Port 5	–	–	1	

Table 31. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I_{LIH1}	$V_{IN} = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_{IN} = V_{DD}$ X_{IN}, X_{OUT} and XT_{IN}	–	–	20	µA
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, XT_{IN} and RESET	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT}, and XT_{IN}	–	–	– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	
Pull-Up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 0–4	15	40	80	KΩ
		V_{DD} = 3 V ± 10%	30	80	200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% RESET	150	220	350	KΩ
		V_{DD} = 3 V ± 10%	300	400	800	
LCD Voltage Dividing Resistor	R_{LCD}	–	40	55	90	KΩ
$\lvert V_{DD-COMi} \rvert$ voltage drop (i = 0–7)	V_{DC}	V_{DD} = 2.7 V to 6.0 V – 15 µA per common pin	–	–	120	mV
$\lvert V_{DD-SEGx} \rvert$ voltage drop (x = 0–39)	V_{DS}	V_{DD} = 2.7 V to 6.0 V – 15 µA per segment pin	–	–	120	
V_{LC1} output voltage	V_{LC1}	V_{DD} = 3.5 V to 6.0 V (1) LCD clock = 0 Hz, V_{LC5} = 0 V	0.8 V_{DD} – 0.15	0.8 V_{DD}	0.8 V_{DD} + 0.15	V
V_{LC2} output voltage	V_{LC2}		0.6 V_{DD} – 0.15	0.6 V_{DD}	0.6 V_{DD}+ 0.15	
V_{LC3} output voltage	V_{LC3}		0.4 V_{DD} – 0.15	0.4 V_{DD}	0.4 V_{DD}+ 0.15	
V_{LC4} output voltage	V_{LC4}		0.2 V_{DD} – 0.15	0.2 V_{DD}	0.2 V_{DD} + 0.15	

Table 31. D.C. Electrical Characteristics (Concluded)

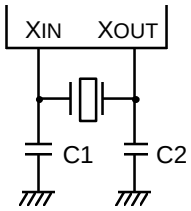
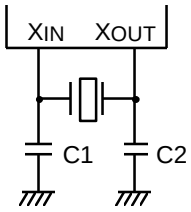
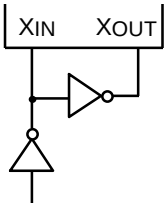
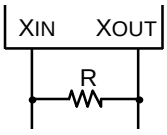
(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply (6) Current	I_{DD1} (2)	V_{DD} = 5 V ± 10% (3) 4.19 MHz crystal oscillator	–	2.7	8	mA
		V_{DD} = 3 V ± 10% (4)		0.27	1.2	
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10% 4.19 MHz crystal oscillator	–	1.2	1.8	
		V_{DD} = 3 V ± 10%		0.26	1.0	
	I_{DD3} (5)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator	–	17	90	µA
	I_{DD4} (5)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator	–	6	15	µA
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	–	0.5	5	
		V_{DD} = 3 V ± 10%		0.2	3	

NOTES:
1. 1/5 bias for test only. In 1/4 bias LCD operation mode, V_{DD} condition is 2.7 V to 6.0 V.
2. Data includes power consumption for subsystem clock oscillation.
3. For high-speed controller operation, the power control register (PCON) must be set to 0011B.
4. For low-speed controller operation, the power control register (PCON) must be set to 0000B.
5. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
6. Currents in the following circuits are not included; on-chip pull-up resistors, output port drive currents, internal LCD voltage dividing resistors, comparator.

Table 32. Main System Clock Oscillator Characteristics

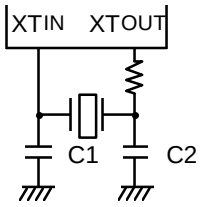
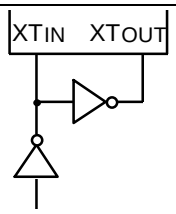
(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	4.5	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	4.19	4.5	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 6.0 V	–	–	10	ms
			V_{DD} = 2.7 V to 4.5 V	–	–	30	
External Clock		X_{IN} input frequency (1)	–	0.4	–	4.5	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	111	–	1250	ns
RC Oscillator		Frequency	V_{DD} = 5 V	0.4	—	2	MHz
			V_{DD} = 3 V	0.4	—	1	

NOTES:
1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval time required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 33. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 6.0 V	–	1.0	2	s
			V_{DD} = 2.7 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

RECOMMENDED OSCILLATOR CONSTANTS

Main System Clock: Ceramic Resonator (Ta = –40 °C – 85 °C)

Manufacturer	Product Name	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
		C1	C2	MIN	MAX	
TDK	FCR4.19MC5	–	–	2.7	6.0	On-chip Capacitor: 30 pF±20%, Leaded Type
	FCR4.19M5	33	33	2.7	6.0	Leaded Type
	CCR4.19MC3	–	–	2.7	6.0	On-chip Capacitor: 30 pF±20%, Leaded Type
	CCR1000K2	100	100	2.7	6.0	SMD Type

Table 34. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	—	—	15	pF
Output Capacitance	C_{OUT}		—	—	15	pF
I/O Capacitance	C_{IO}		—	—	15	pF

Table 35. Comparator Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 6.0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	–	–	0	–	V_{DD}	V
Reference Voltage Range	V_{REF}		0		V_{DD}	
Input Voltage Accuracy	V_{CIN}		–		± 150	mV
Input leakage Current	I_{CIN}, I_{REF}		- 3		3	µA

Table 36. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (NOTE)	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95	–	64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8		64	
		With subsystem clock (fxt)	114	122	125	
TCL0 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 4.5 V to 6.0 V	0	–	1	MHz
		V_{DD} = 2.7 V to 4.5V			275	kHz
TCL0 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 6.0 V	0.48	–	–	µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V External SCK source	800	–	–	ns
		Internal SCK source	950			
		V_{DD} = 2.7 V to 4.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V External SCK source	400	–	–	ns
		Internal SCK source	$t_{KCY}/2$ – 50			
		V_{DD} = 2.7 V to 4.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2$ – 150			
SI Setup Time to SCK High	t_{SIK}	External SCK source	100	–	–	ns
		Internal SCK source	150			
SI Hold Time to SCK High	t_{KSI}	External SCK source	400	–	–	ns
		Internal SCK source	400			

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

Table 36. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 2.7 V to 4.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(See Note)	–	–	µs
		INT1, INT2, INT4, K0–K3	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128 / fx as assigned by the IMOD0 register setting.

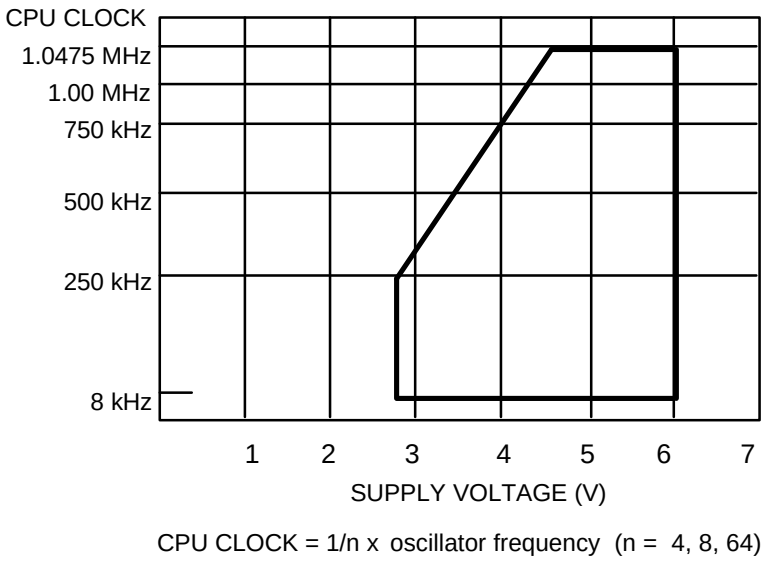


Figure 48. Standard Operating Voltage Range

Table 37. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

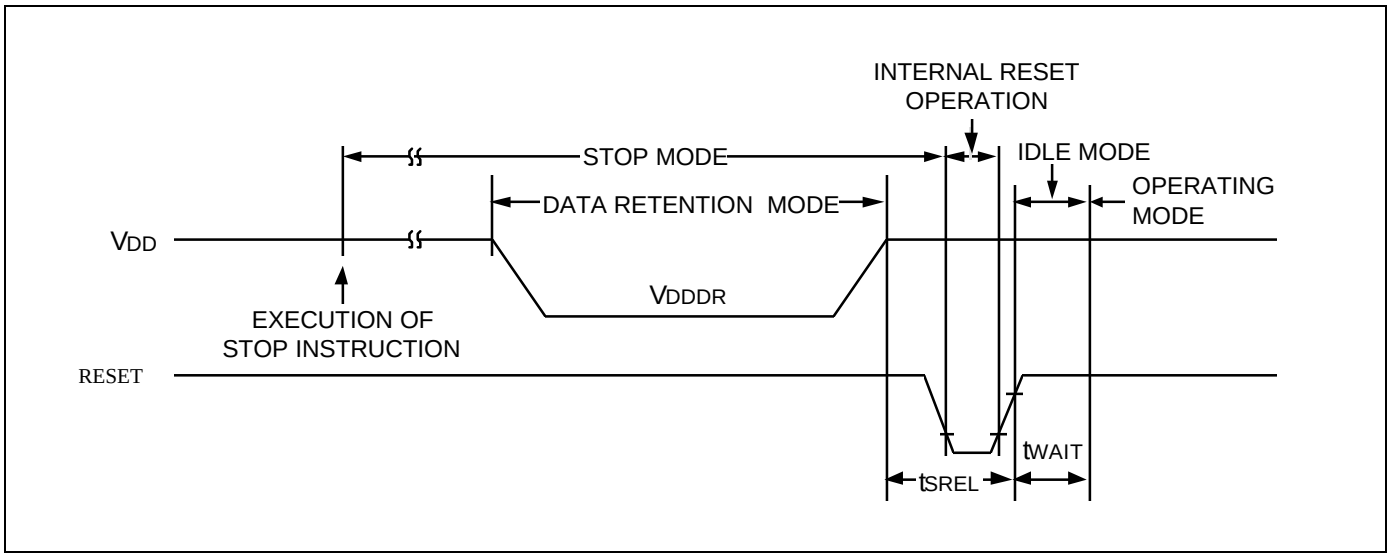


Figure 49. Stop Mode Release Timing When Initiated By RESET

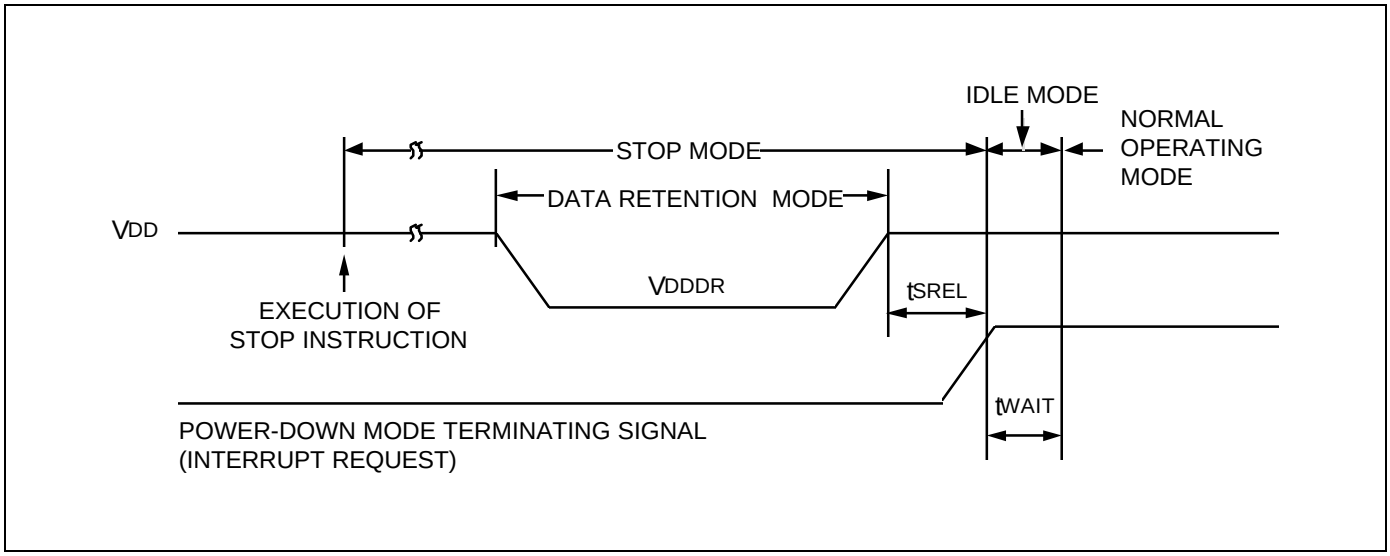


Figure 50. Stop Mode Release Timing When Initiated By Interrupt Request

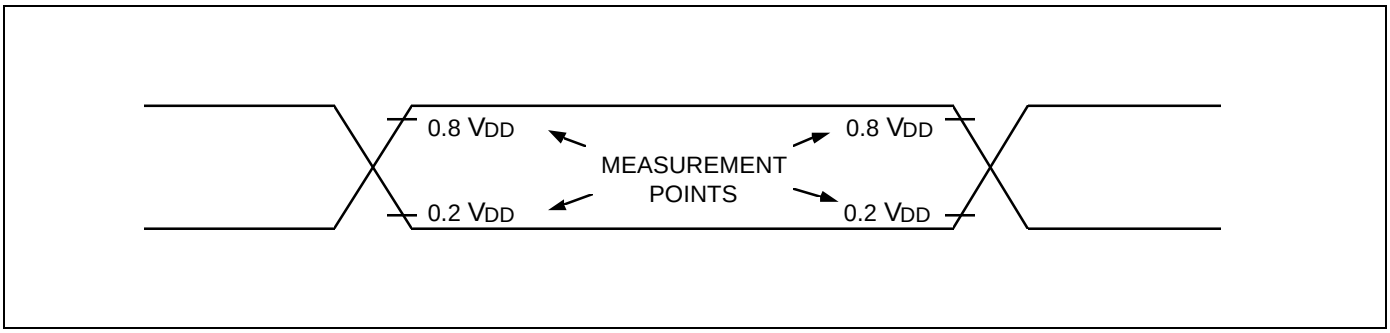


Figure 51. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

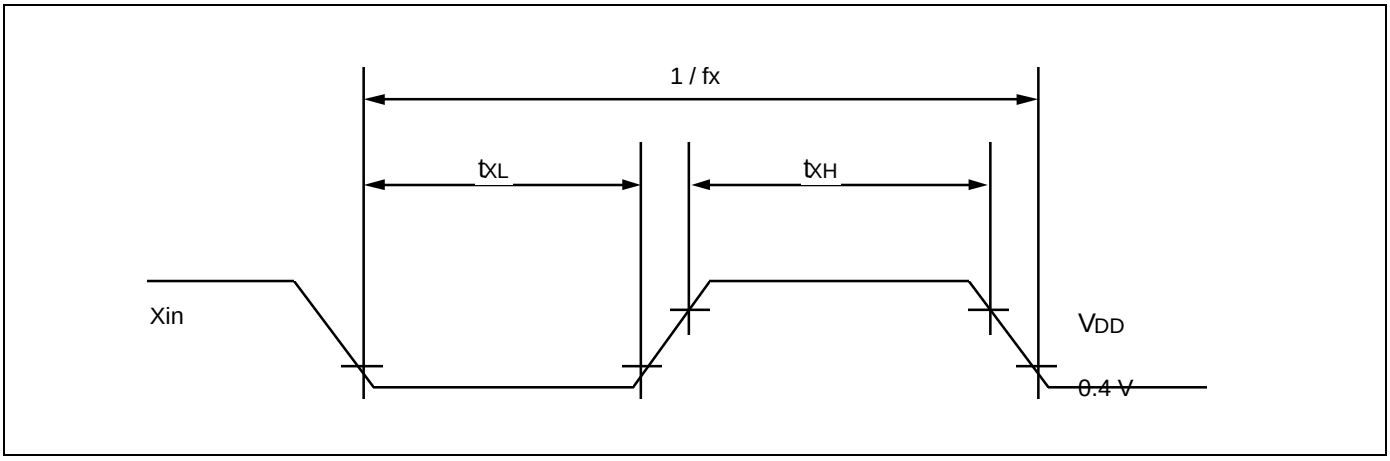


Figure 52. Clock Timing Measurement at X_{in}

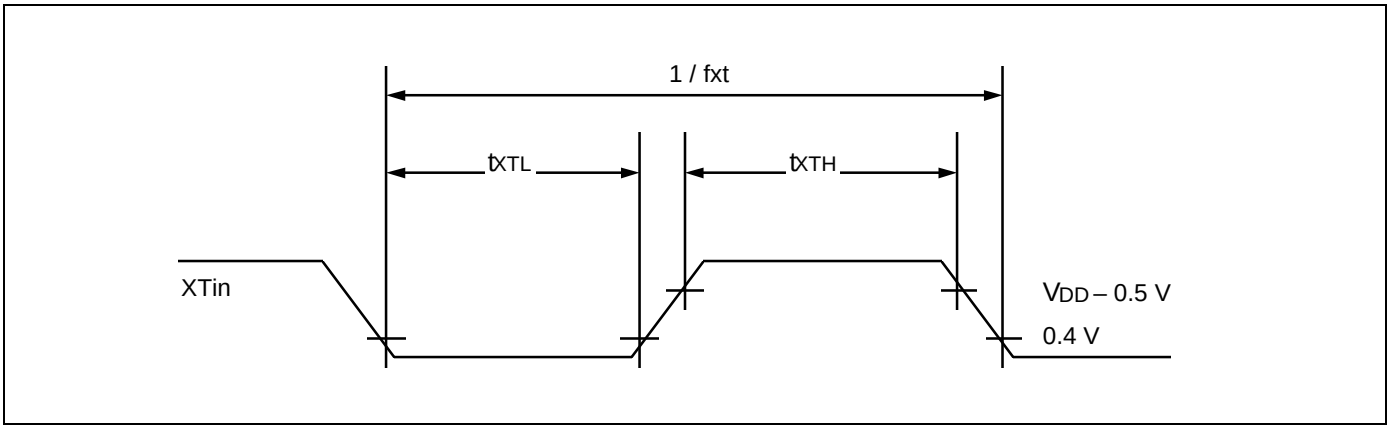


Figure 53. Clock Timing Measurement at XT_{in}

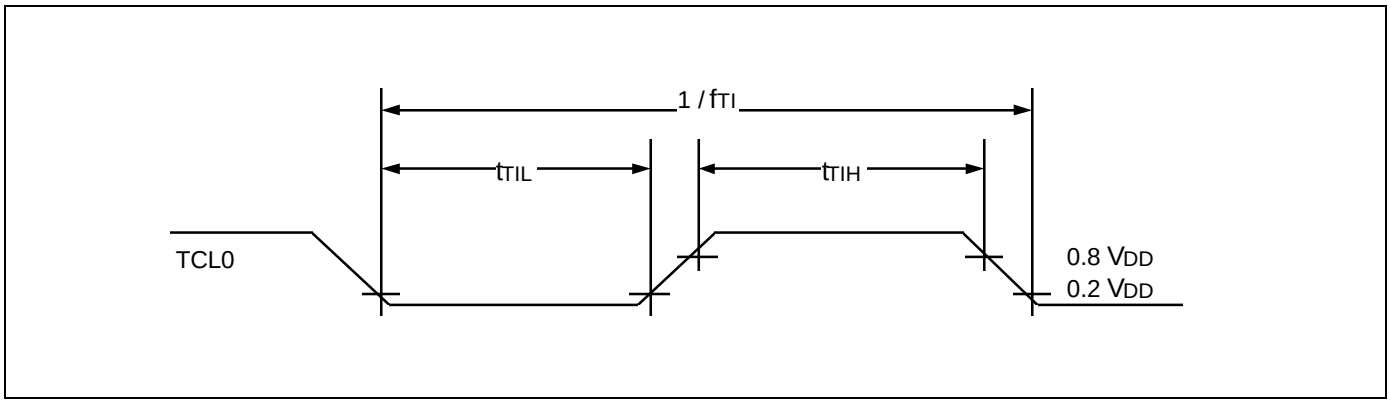


Figure 54. TCL Timing

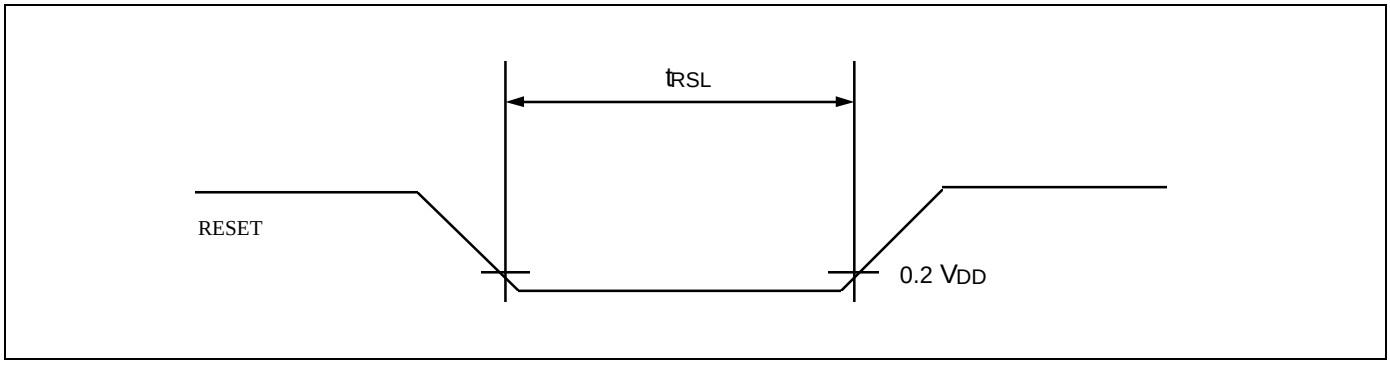


Figure 55. Input Timing for RESET Signal

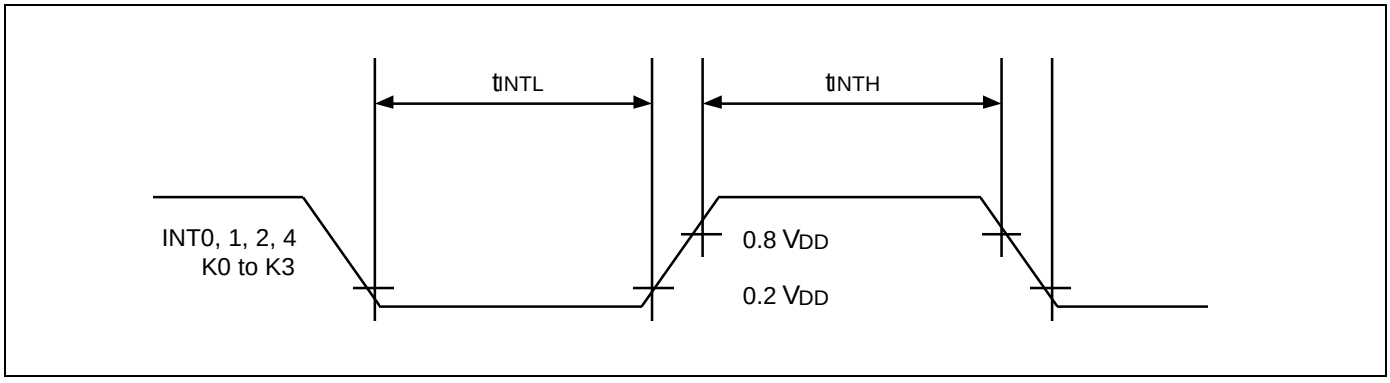


Figure 56. Input Timing for External Interrupts and Quasi-Interrupts

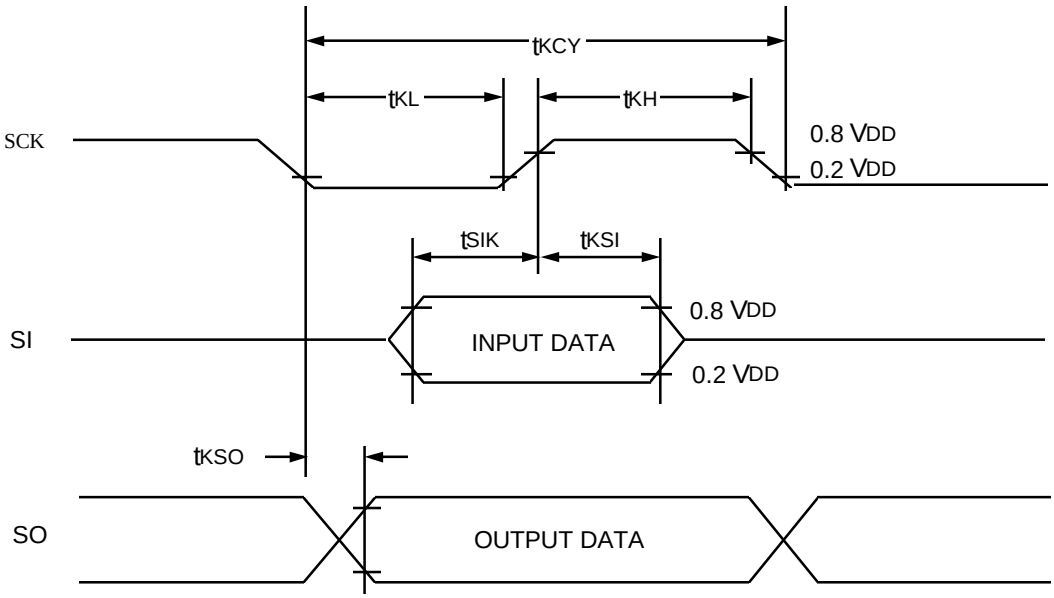


Figure 57. Serial Data Transfer Timing

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

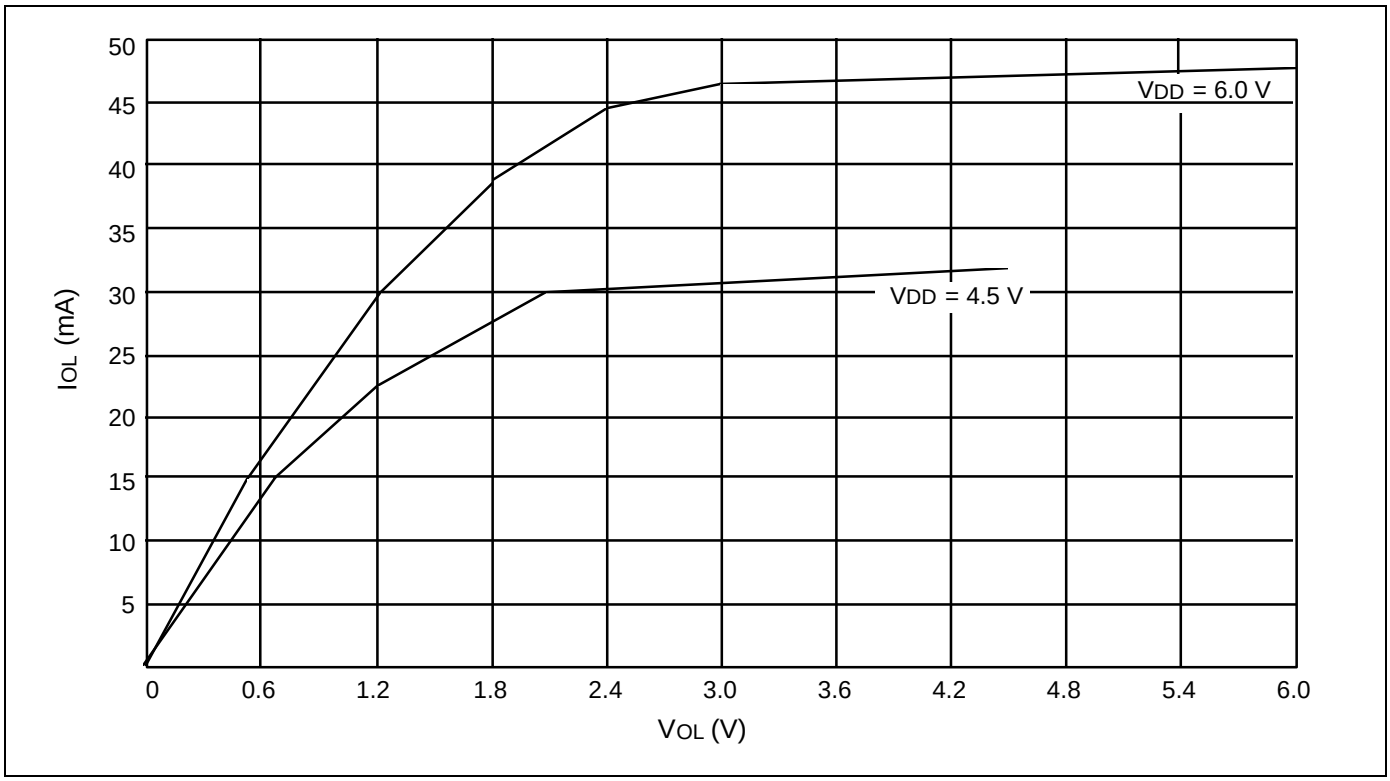


Figure 58. I_{OL} VS. V_{OL} (Ports 0,2,3,4)

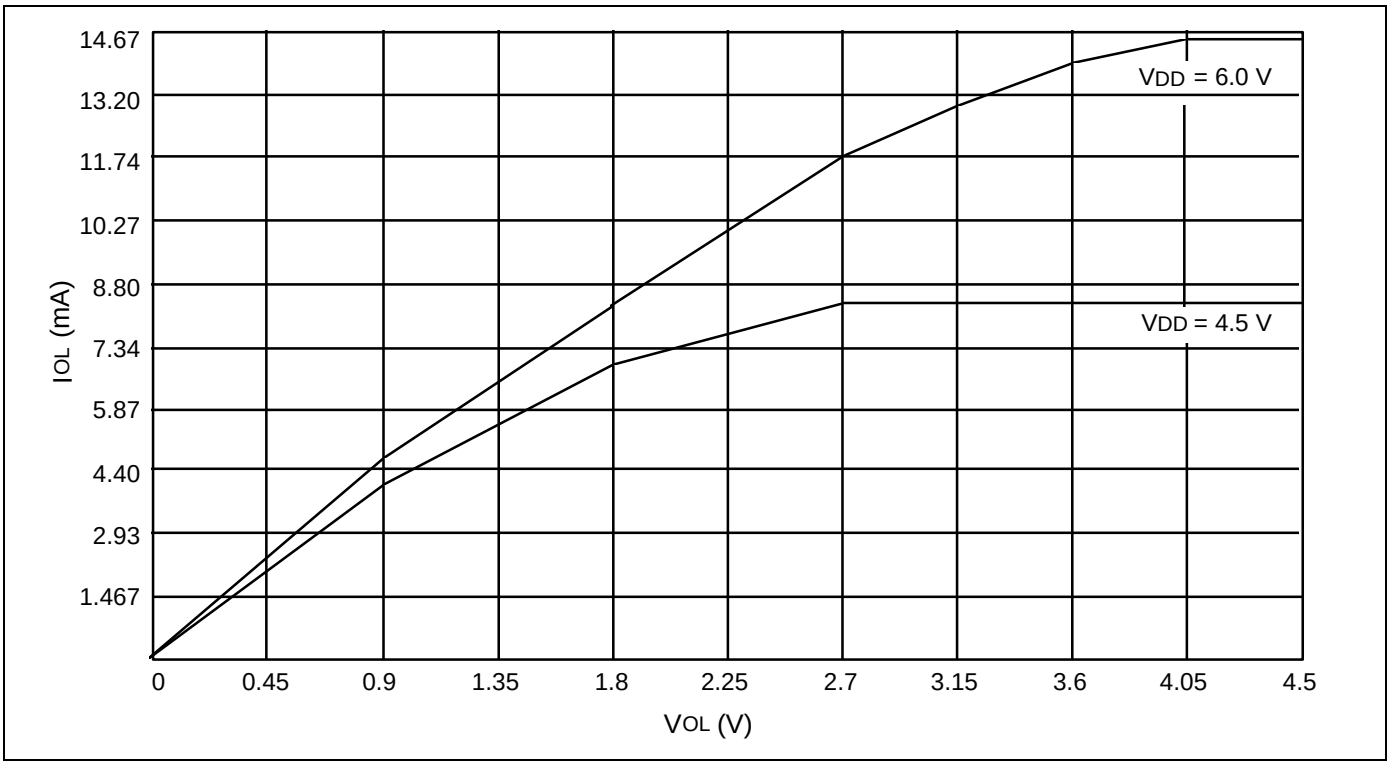


Figure 59. I_{OL} VS. V_{OL} (Port 5)

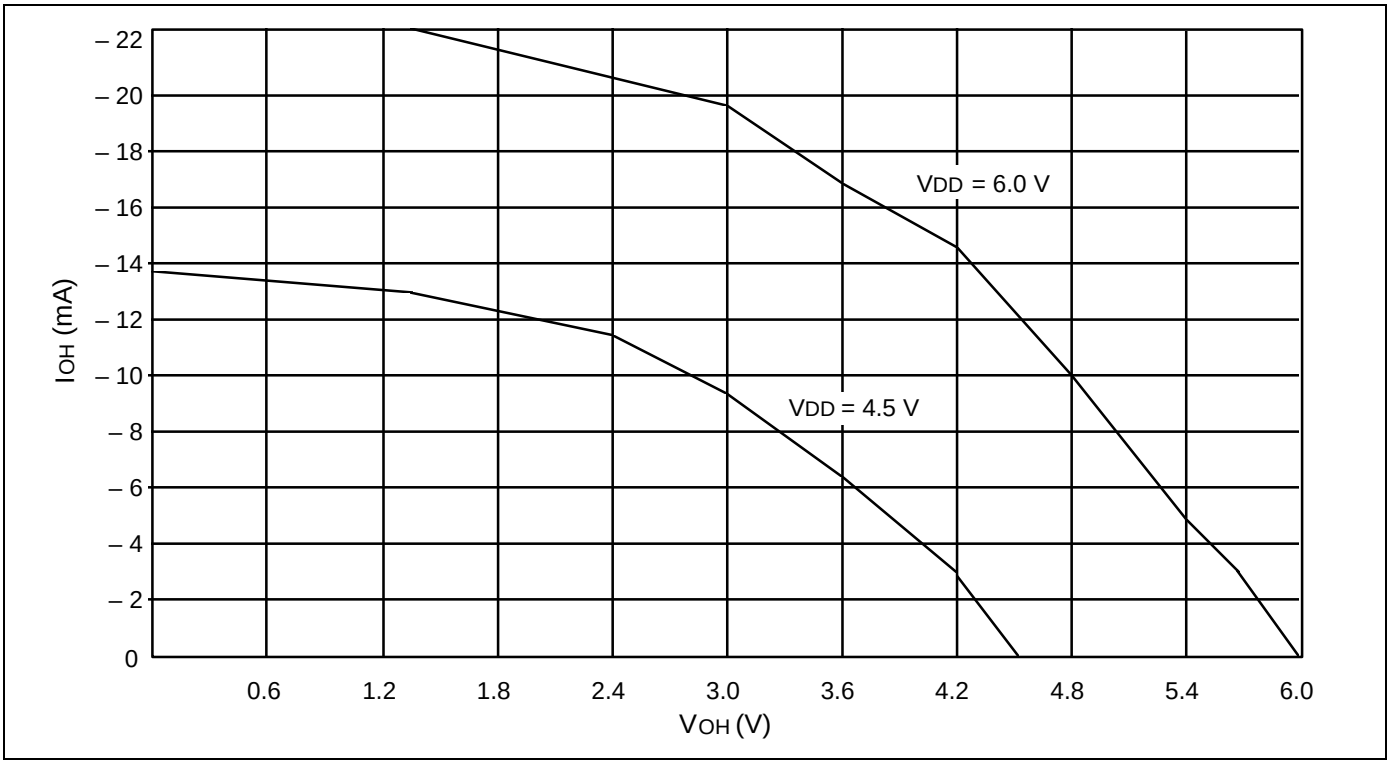


Figure 60. I_{OH} VS. V_{OH} (Ports 0,2,3,4)

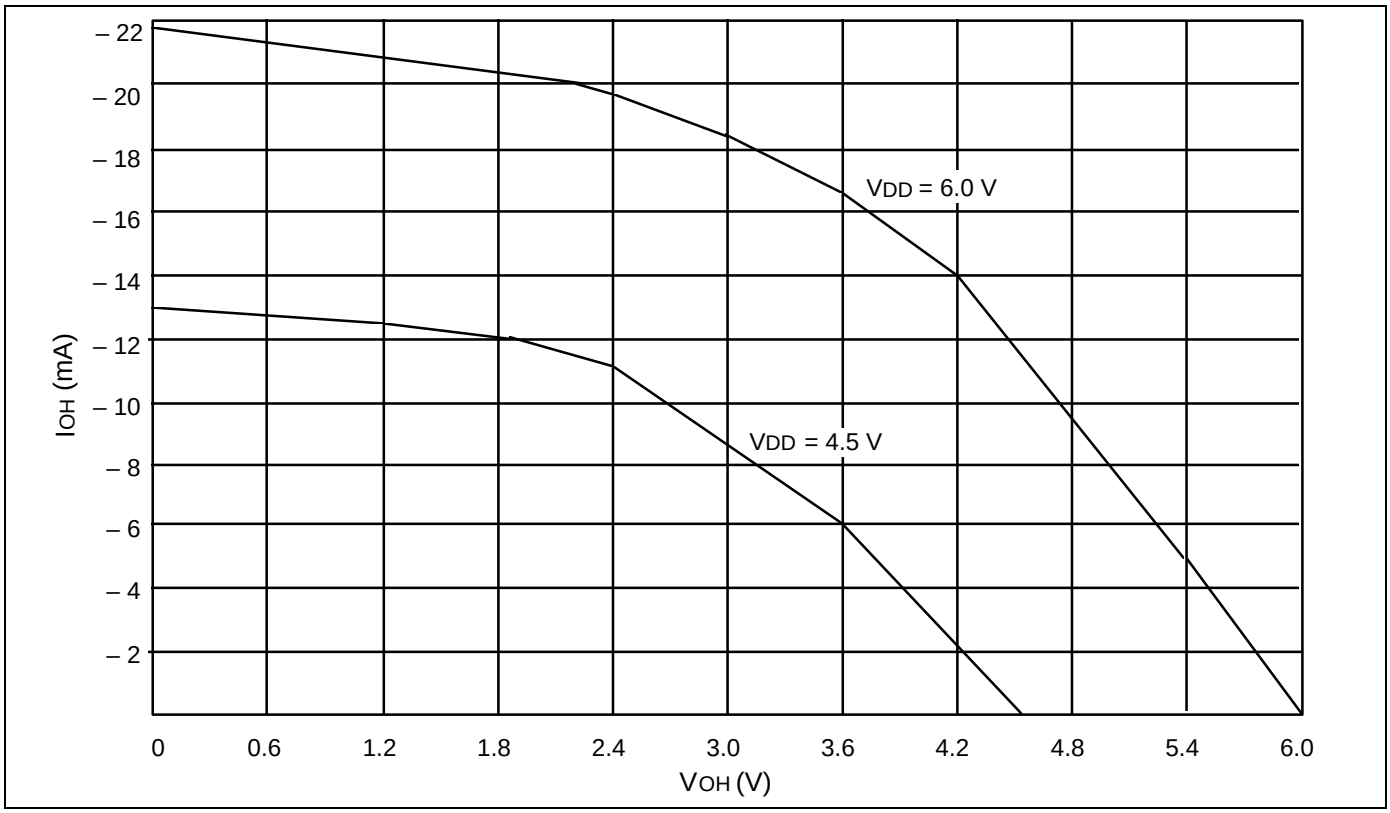


Figure 61. I_{OH} VS. V_{OH} (Port 5)

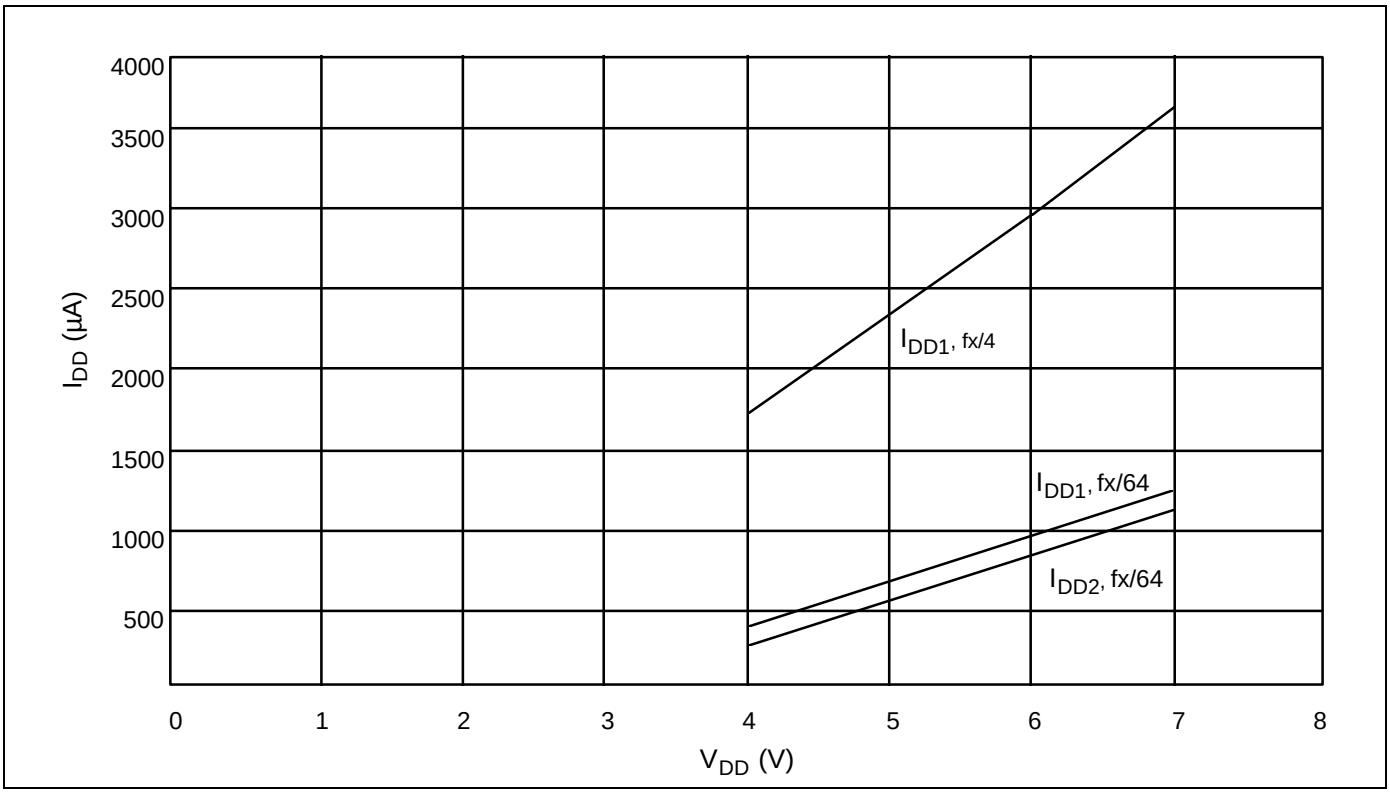


Figure 62. I_{DD} VS. V_{DD}

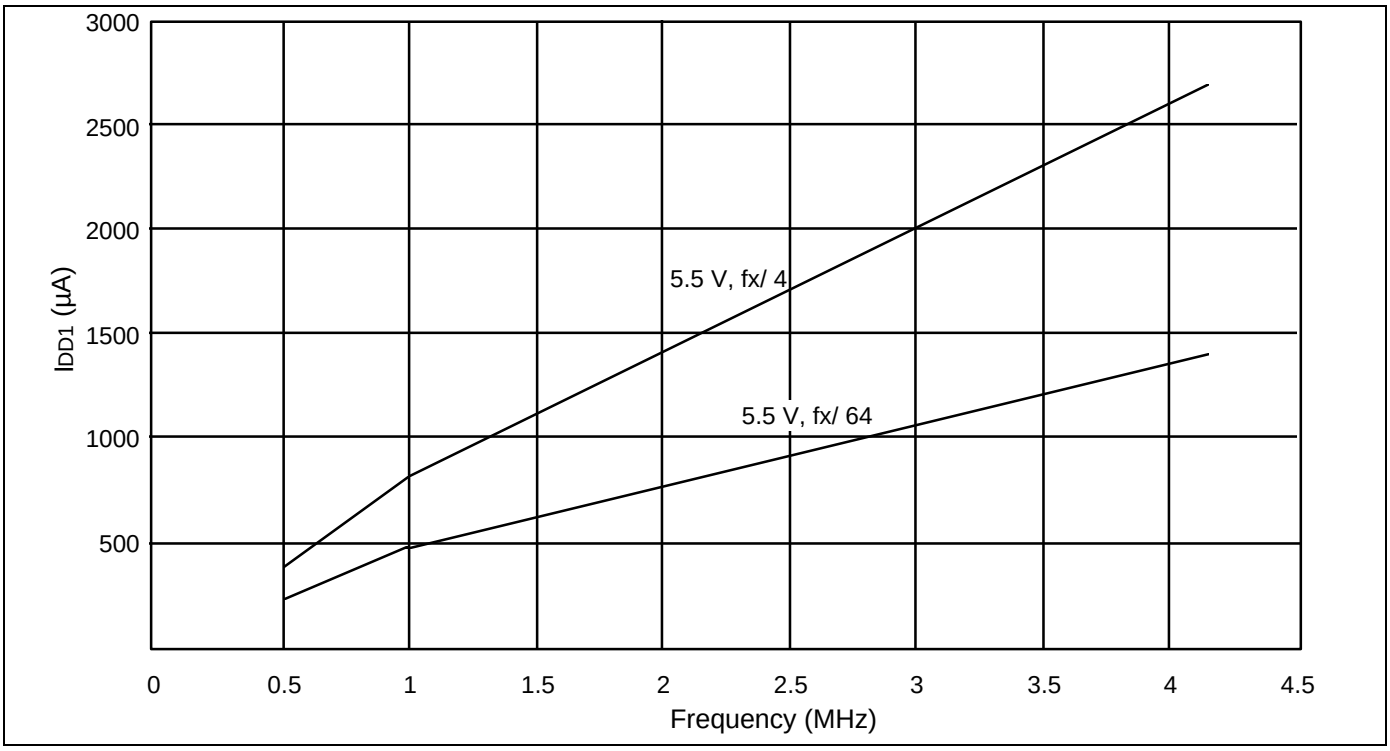


Figure 63. I_{DD1} VS. Frequency

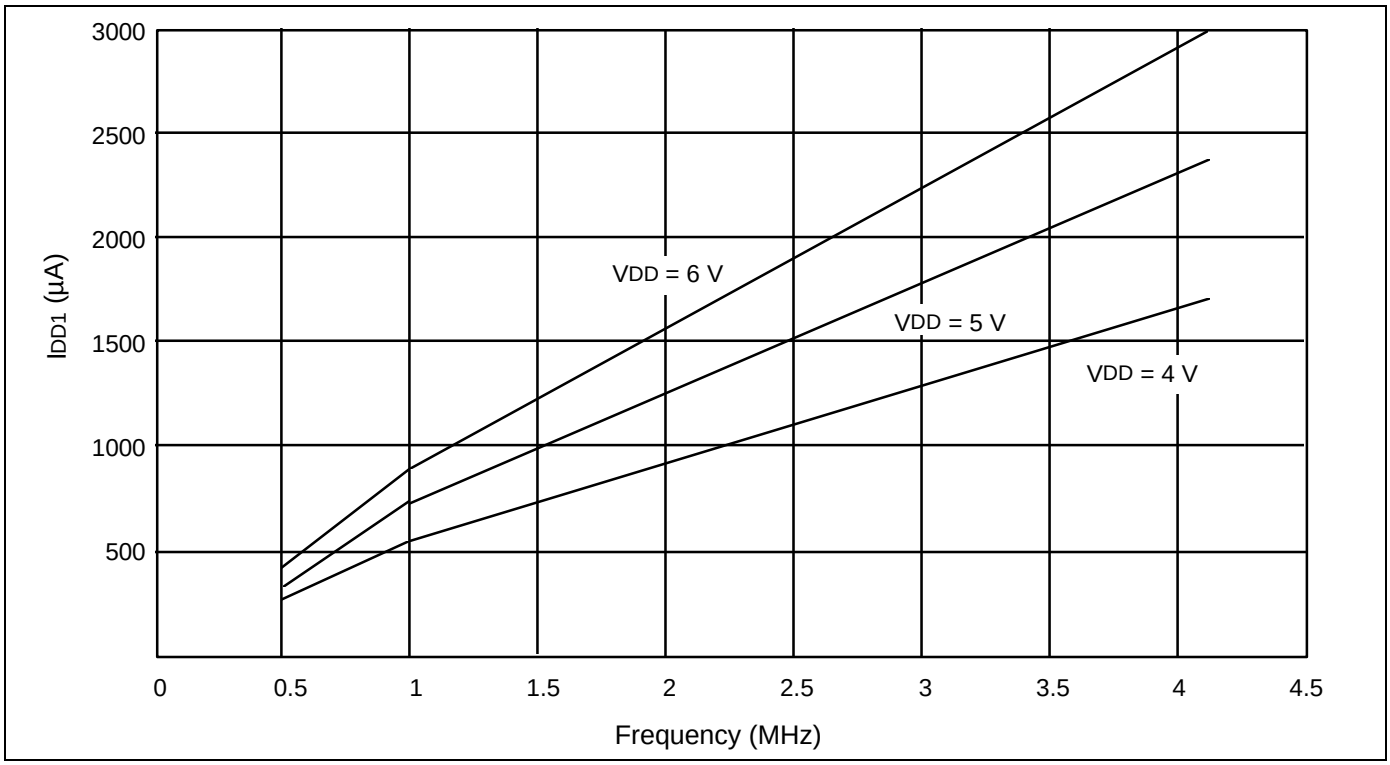


Figure 64. I_{DD1} vs. Frequency vs. V_{DD}

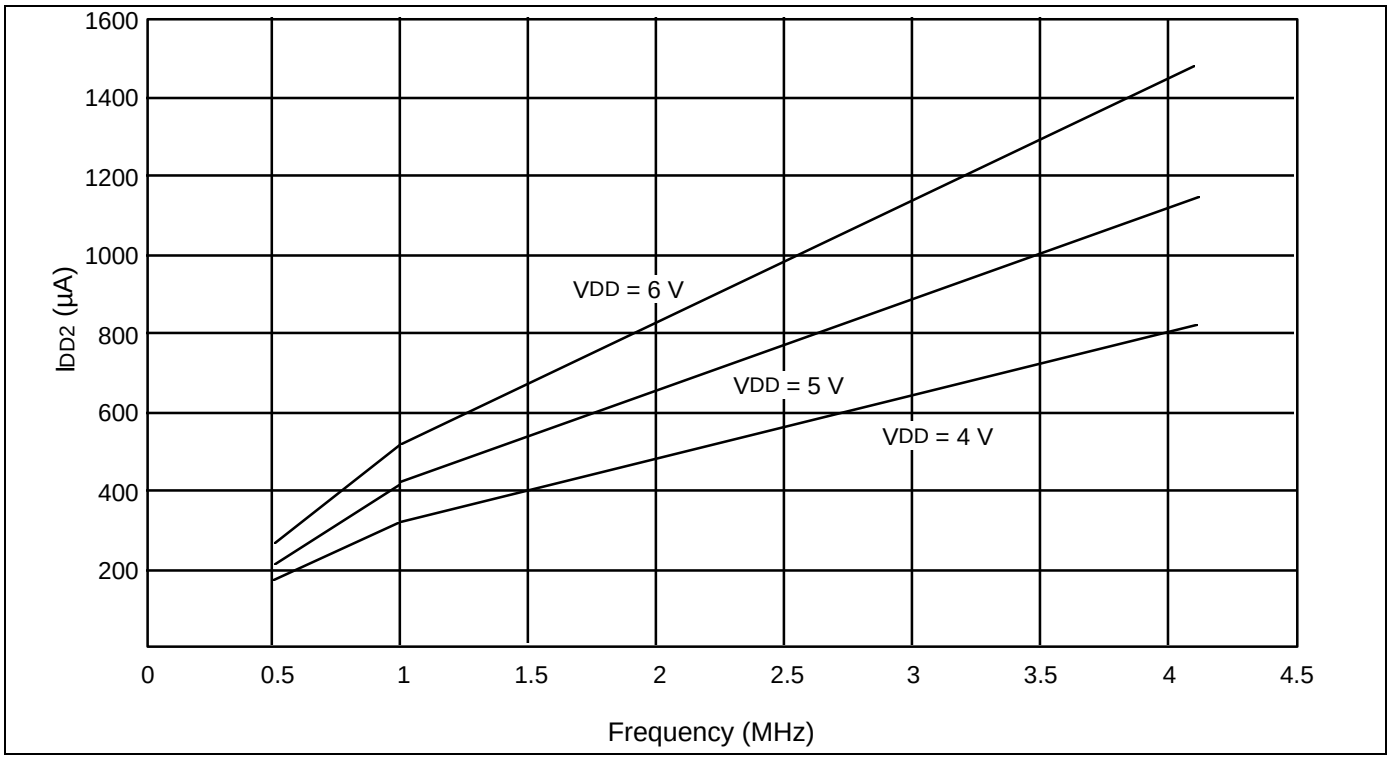


Figure 65. I_{DD2} vs. Frequency vs. V_{DD}

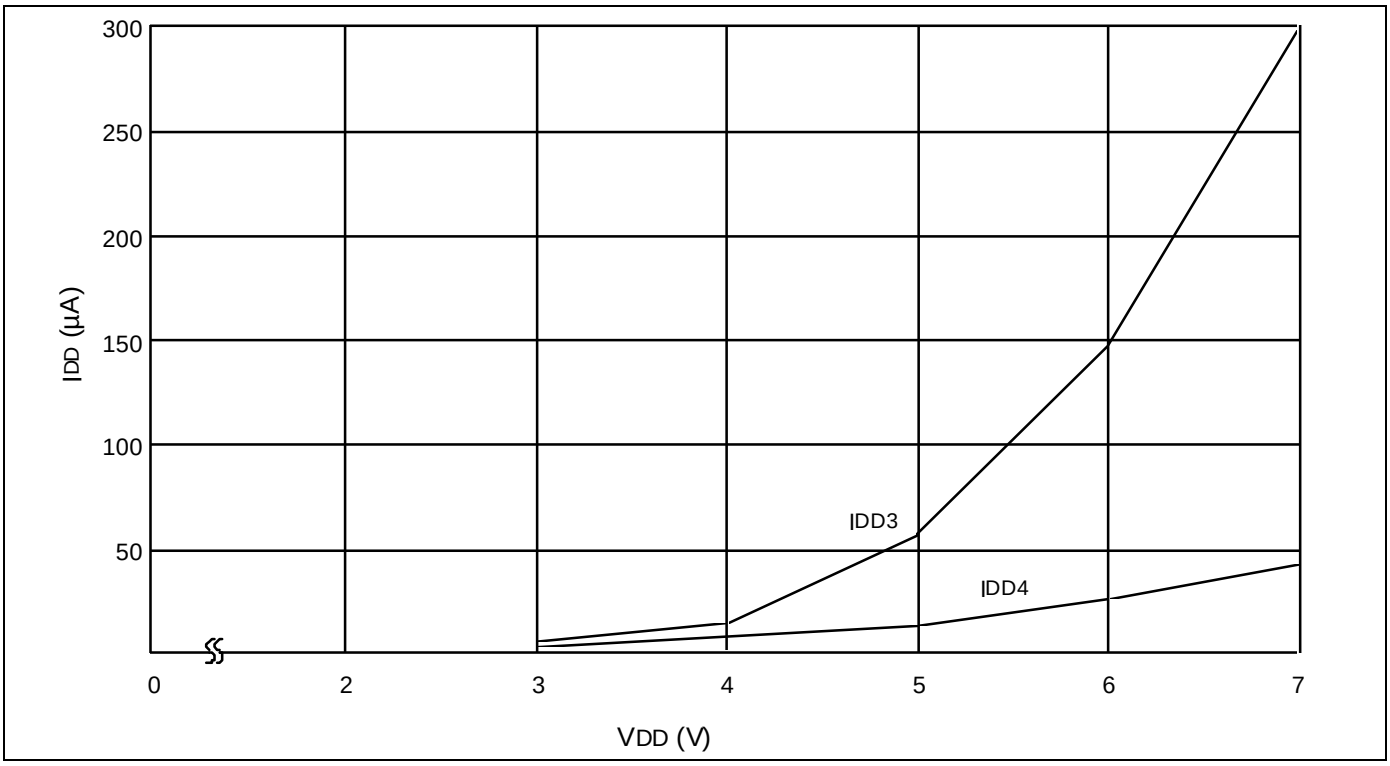


Figure 66. I_{DD3}, I_{DD4} VS. V_{DD}

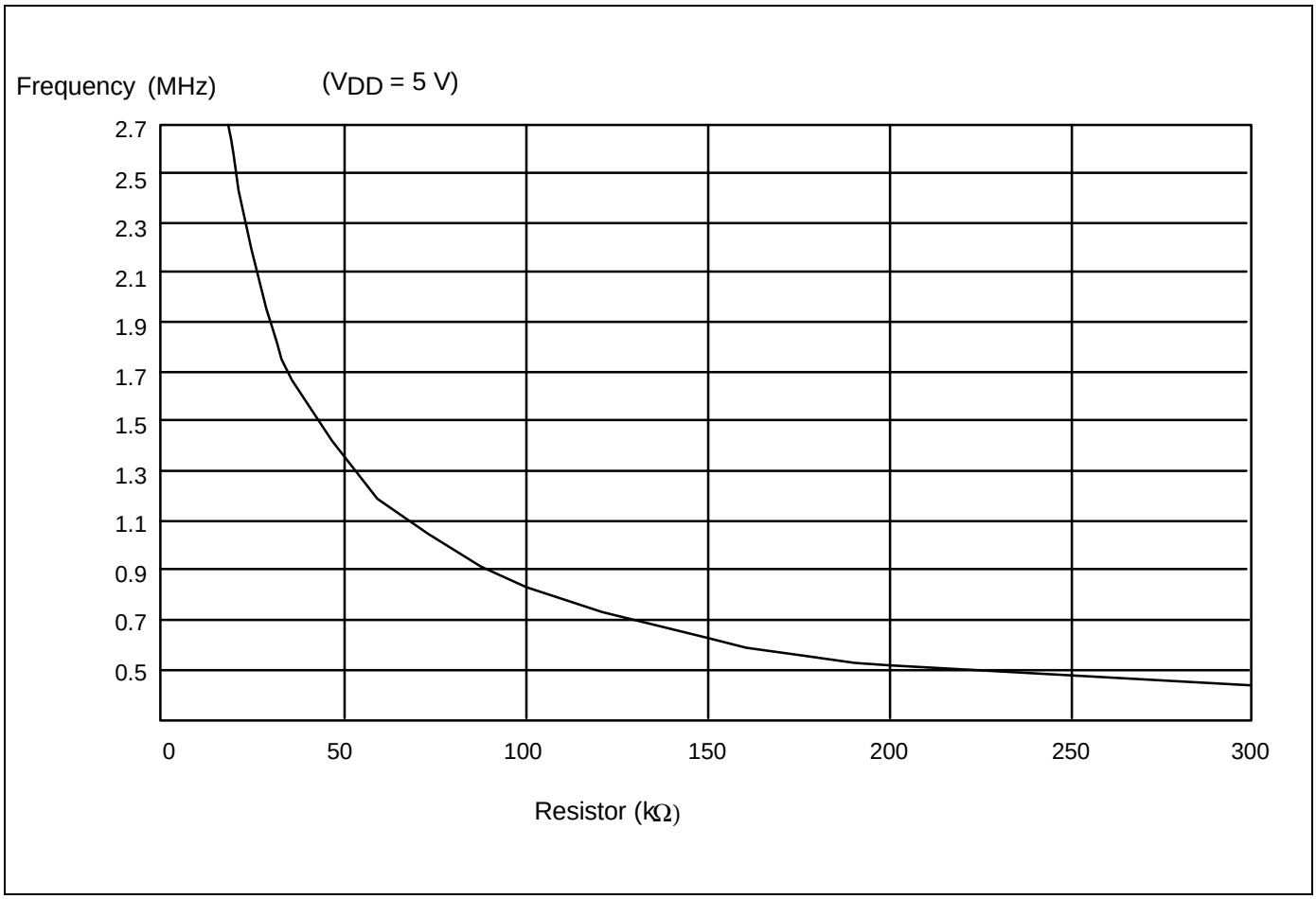


Figure 68. Frequency (fx) VS. Resistor