HD-SDI DATA RETIMER S8301

FEATURES

- HD-SDI Retimer
- 1.485 Gbps operation
- Lock detect
- Port bypass
- +3.3V Power supply
- SMPTE 292M Compliant
- 32 Pin TQFP

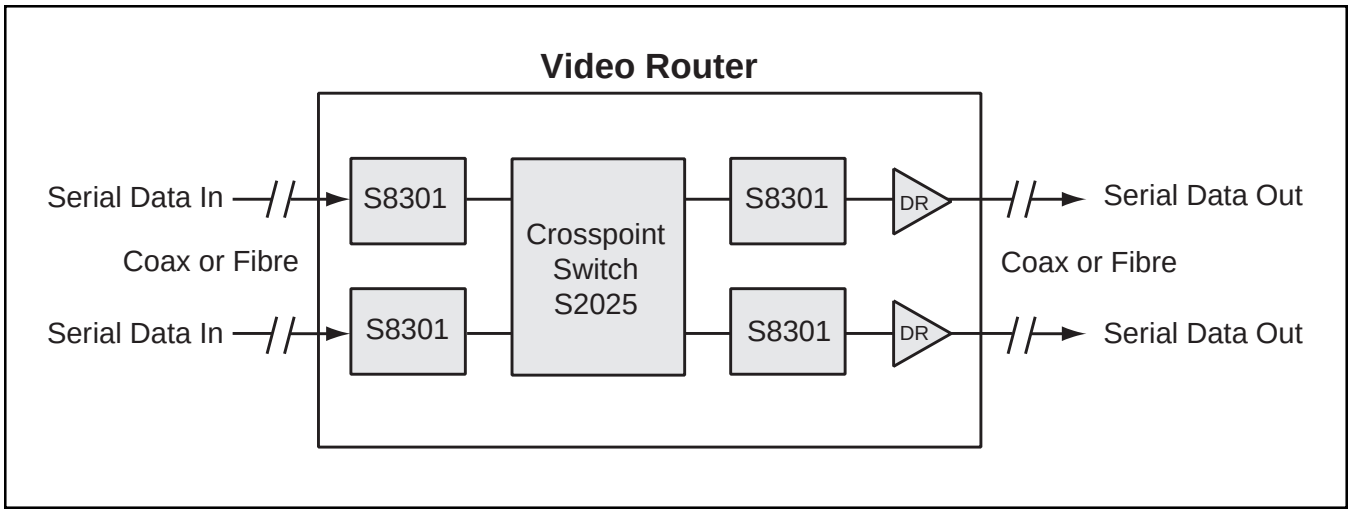
APPLICATIONS

- Routers
- Distribution Amplifiers
- Backplanes

GENERAL DESCRIPTION

The HD-SDI (High Definition Serial Digital Interface) Retimer Circuit is used in full-speed (1.485 Gb/s) HDTV bit stream switching and distribution systems. It contains a monolithic Clock Recovery Unit (CRU), a lock detect feature and a port bypass circuit. The CRU may be used alone to implement a general purpose repeater needed for applications where a re-timed and buffered signal is required. The Data Retimer performs the function of a port bypass circuit followed by a clock and data retiming Phase Locked Loop (CDR). The CDR re-times incoming serial data, detects whether a valid signal is present and outputs a low jitter serial data stream.

Figure 1. System Block Diagram



OVERVIEW

The Data Retimer performs two functions. The first is to perform the function of a Port Bypass Circuit for nodes in a multi-rate switch or router. The low jitter accumulation of the Port Bypass Path is essential in these systems. The second function is to retime and restore signal quality after transmission and equalization. The low jitter transfer peaking and the high jitter tolerance specifications of the Clock and Data Recovery PLL are essential in these applications. In addition, the Lock detect circuit monitors the incoming signals for run length, transition density and frequency. The output of this circuit is useful for link performance monitoring and detection of channel present.

JITTER PERFORMANCE

The Data Retimer complies with the minimum jitter tolerance requirements proposed by SMPTE 292M when used with differential inputs and outputs. In addition, the Data Retimer is designed for minimum jitter generation and jitter transfer specifications. This allows the optimum system design for arbitrated loop architectures.

Jitter Tolerance

Input jitter tolerance is defined as the amplitude of frequency dependent, random and deterministic jitter that causes the clock recovery PLL to violate the BER specifications.

Alignment Jitter

The variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter. Alignment jitter is out of band with respect to the PLL bandwidth.

Timing Jitter

The variation in a position of a signal's transitions occuring at a rate greater than a specified frequency, typically 10 Hz. Variations occuring below this specified frequency are termed wander and are not addressed by this practice. Timing jitter is in band with respect to the PLL bandwidth.

Deterministic Jitter Tolerance

Deterministic Jitter Tolerance is the amount of Deterministic jitter that the clock recovery PLL must tolerate.

Lock Detect

The Data Retimer lock detect circuit monitors the selected input signal to detect the presence of the channel. This is done by monitoring the run length, transition density and frequency content of the incoming data. The frequency monitor circuit checks the difference between the divided down recovered clock and the externally supplied reference clock (REFCLK). If the frequency difference of the recovered clock and the reference clock varies by more than ±240 ppm the part will be declared out of lock. In the out of lock state the PLL will lock to the local reference clock and periodically poll the serial data inputs looking for data with valid frequency content. The lock detect output transitions to a logic 1 when the PLL is locked to data, and transitions to a logic 0 when locked to the reference clock.

Figure 3. LOCKDET Function

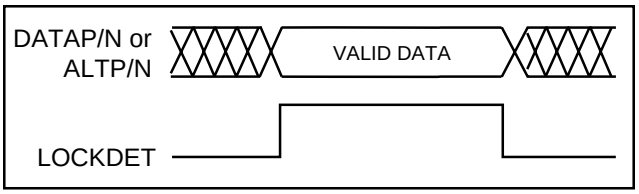


Figure 2. Functional Block Diagram

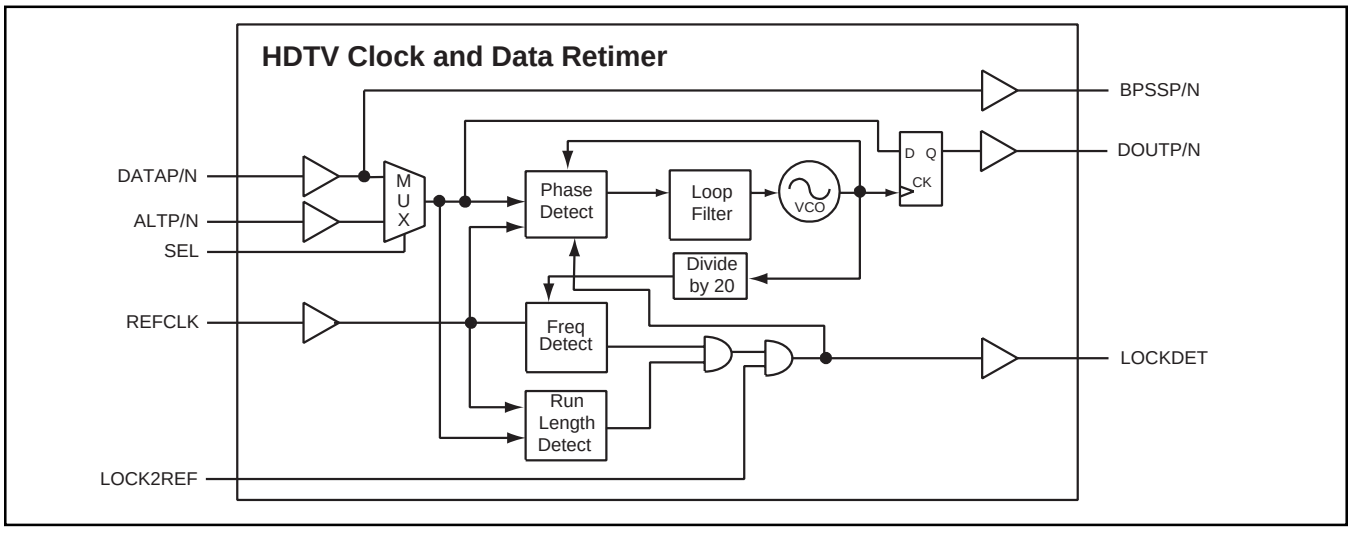


Table 1. Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
DOUTP DOUTN	Diff. LVPECL	O	4 5	Serial Output Data. This output has been retimed by the Clock and Data Recovery PLL. Open emitter (14-20 mA bias current needed).
DATAP DATAN	Diff. LVPECL	I	1 2	Serial Input Data. Differential LVPECL.
ALTN ALTP	Diff. LVPECL	I	28 29	Alternate Serial Input Data. Differential LVPECL. See Figure 9 if not used.
REFCLK	TTL	I	22	Reference clock for the PLL, nominally at 74.25 MHz, rising edge active. See Figure 10 for reference clock biasing.
LPF1 LPF2	Analog		12 11	Loop filter capacitor pins. LPF2 to 27Ω in series with 2.2µF in series with 27Ω to LPF2. See Figure 8.
LCKREFN	3 State TTL	I	24	Active Low. When active the CDR PLL will be forced to lock to the local reference clock (REFCLK). When disconnected, the data retimer will be put into test mode and the PLL will be bypassed for factory testing.
LOCKDET	TTL	O	17	Active High. When active, LOCKDET indicates the CDR PLL is locked to the serial data stream. When inactive, the CDR PLL will lock to the local reference clock indicating a loss of data condition.
BPSSP BPSSN	Diff. LVPECL	O	20 19	Port Bypass output.
SEL	TTL	I	30	When SEL is High, ALTP/N is selected. When SEL is Low, DATAP/N is selected.
REFSEL	TTL	I	15	Active Low. When active, allows 148.5 MHz reference clock. When inactive, allows 74.25 MHz clock.
TEST	3 Level TTL	I	16	Used for manufacturing test. Normal chip operation when held Low.
GND	Ground		6, 18, 23, 31	Ground pins are physically mounted to the die surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible.
VCC			7, 21, 25, 26	+3.3V Power Supply.
VCCA	Analog		3, 8, 14	Analog +3.3V Power Supply for the CRU.
GNDA	Analog		9, 13	Analog Ground for the CRU.
NC			10, 27, 32	No connect.

Figure 4. 32 TQFP Pinout

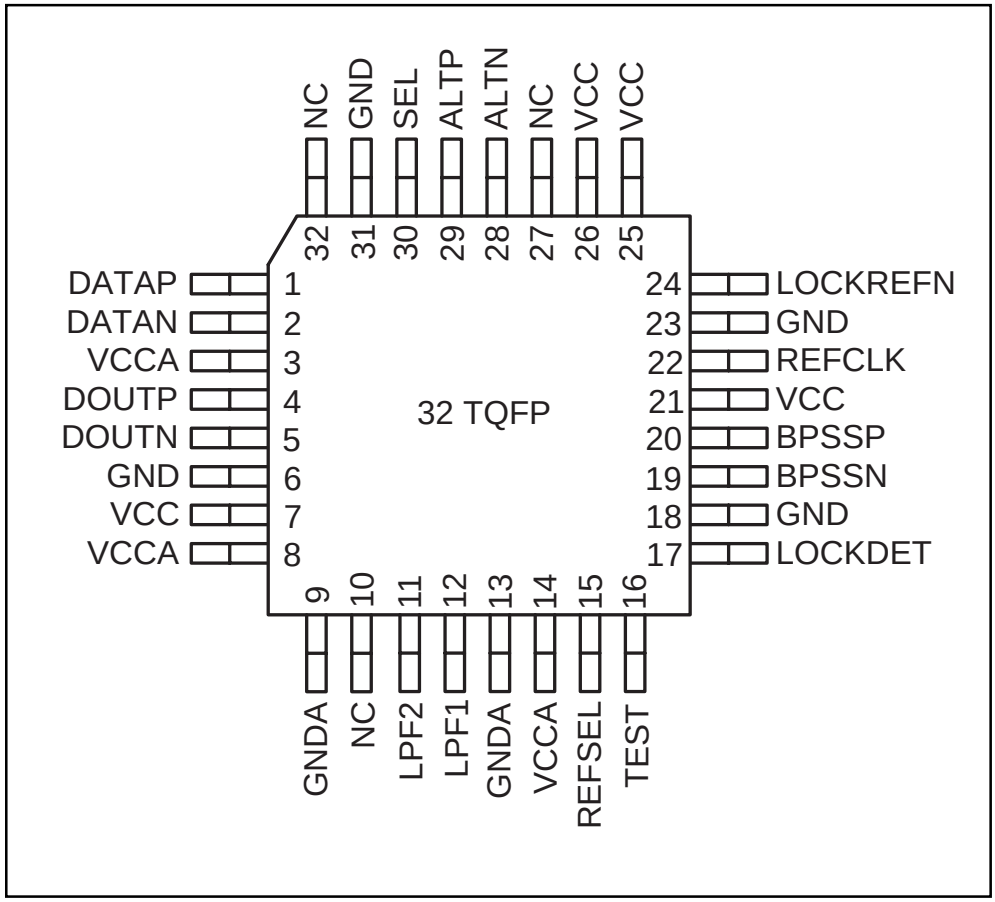
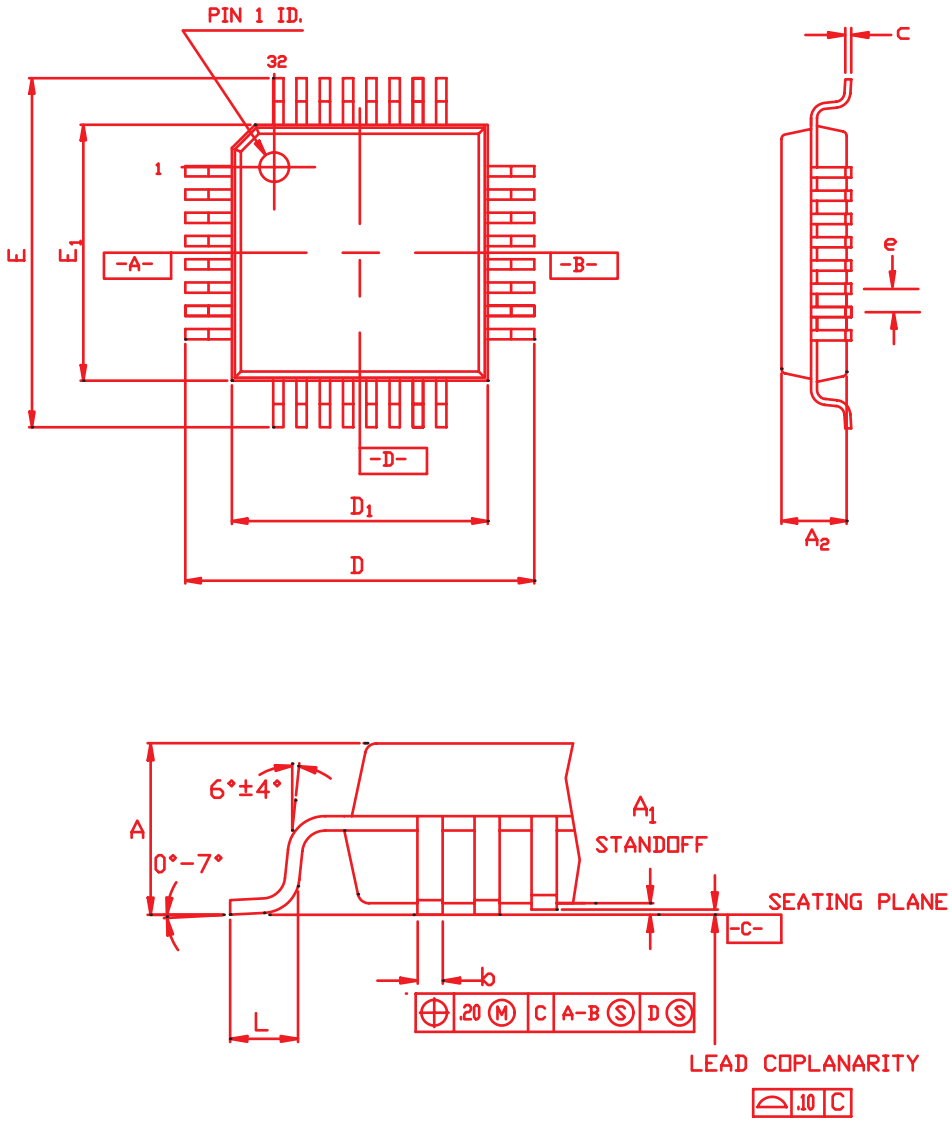


Figure 5. 32 TQFP (7 x 7 x 1.4mm) Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN		0.05	1.35	8.75	6.90	8.75	6.90	0.50	0.30	0.80 BSC.	0.127 BSC.
NOM			1.40	9.00	7.00	9.00	7.00	0.60	0.35		
MAX	1.60	0.15	1.45	9.25	7.10	9.25	7.10	0.75	0.40		

Table 2. Performance Summary

Parameter	S8301	Units
Operating Frequency	1485	Mbps
Serial Clock Period	.637	ns
Acquision Time	250	bit times
Reference Clock	74.25	MHz

Table 3. AC Characteristics

Parameters	Description	Min	Max	Units	Comments
T_R, T_F	REFCLK Rise and Fall Time		1.7	ns	
FT	REFCLK Frequency Tolerance		100	PPM	Difference between REFCLK and RX data frequency
DC	REFCLK Duty Cycle	40	60	%	
T_{SR}, T_{SF}	DOUTP/N		270	ps	50Ω to Vcc-2.0V (20-80%)
T_{SR}, T_{SF}	BPSSP/N		270	ps	50Ω to Vcc-2.0V (20-80%)
T_{PROP}	DATAP/N to BPSSP/N		2	ns	
Jitter Specifications					
RJOUT	Random Jitter (RMS) DOUTP/N		20	ps	
DJOUT	Deterministic Jitter (p-p) DOUTP/N		100	ps	
DJT	Alignment jitter tolerance DATAP/N		0.2	UI	Peak-to-Peak w/K28.5±pattern.
JXFR	Jitter Transfer peaking (input to output)		0.2	dB	Cut off freq. at 2.1 MHz with 1010 pattern.
TJT	Total Jitter Tolerance		1.0	UI	K28.5± alignment jitter out-of-band 0.2UI, jitter in-band 0.8UI.

Table 4. DC Characteristics (Over recommended operating conditions)

Parameters	Description	Min	Typ	Max	Units	Comments
V_{OH}	Output HIGH Voltage (TTL)	2.2			V	I_{OH} = -.1 mA
V_{OL}	Output LOW Voltage (TTL)			0.5	V	I_{OL} = +1.2 mA
V_{IH}	Input HIGH Voltage (TTL)	2.0		Vcc	V	
V_{IL}	Input LOW Voltage (TTL)			0.8	V	
I_{IH}	Input HIGH Current (TTL)			50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW Current (TTL)	-500		-50	µA	V_{IN} = 0.5V
V_{CC}	Supply Voltage	3.14		3.47	V	V_{CC} = 3.3V ± 5%
I_{CC}	Supply Current		135	200	mA	Outputs open. V_{CC} = V_{CC} max
P_D	Power Dissipation		.5	.7	W	Outputs open. V_{CC} = V_{CC} max
ΔV_{OUT}	LVPECL Output differential peak-to-peak voltage swing	1200		2200	mV_{p-p}	50Ω to V_{CC} -2.0V
ΔV_{IN}	Receiver differential peak-to-peak input sensitivity, RX and SI	200		2600	mV_{p-p}	V_{CC} = 3.3V, AC coupled. Internally DC biased to V_{CC} -0.65V

Table 5. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
TTL Power Supply Voltage (V_{CC})	0.5		4	V
PECL DC Input Voltage, (V_{INP})	-0.5		V_{CC} +0.5	V
TTL DC Input Voltage, (V_{INP})	-0.5		5.5	V
DC Voltage applied to Outputs for High Output State ($V_{IN,\ TTL}$)	-0.5		V_{CC} +0.5	V
TTL Output Current (I_{OUT}) (DC, Output High)			50	mA
PECL Output Current (I_{OUT}) (DC, Output High)			50	mA
Case Temperature Under Bias (T_C)	-55˚		125˚	C
Storage Temperature (T_{STG})	-65˚		150˚	C
Maximum Input ESD (expect for LPF1 and LPF2)	1000			V

Table 6. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{DD})	+3.1		3.5	V
Ambient Operating Temperature Range (T)	0˚		70˚	C

Notes:

1. CAUTION: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
2. AMCC guarantees the functional and parametric operation of the part under “Recommended Operating Conditions:" except where specifically noted in the AC and DC Parametric Tables.

Figure 6. Serial Output Load

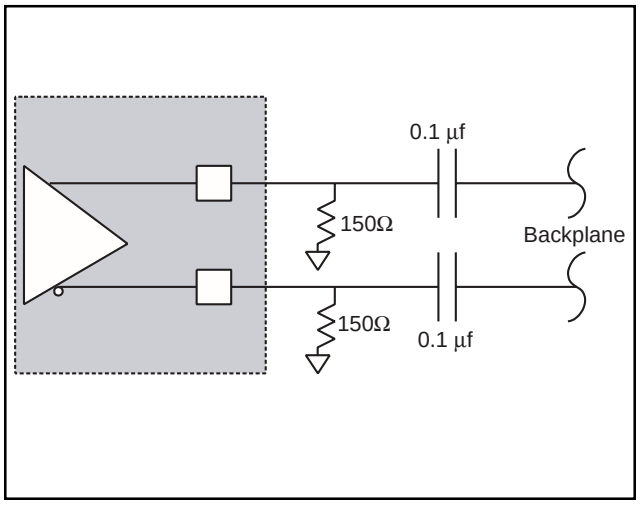
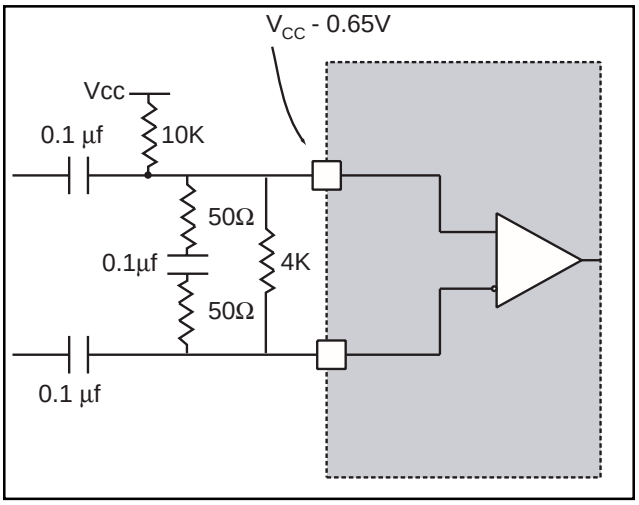


Figure 7. High Speed Differential Inputs



It is recommended that a 60-70mV DC offset be provided.

Figure 8. PLL Loop Bandwidth Components

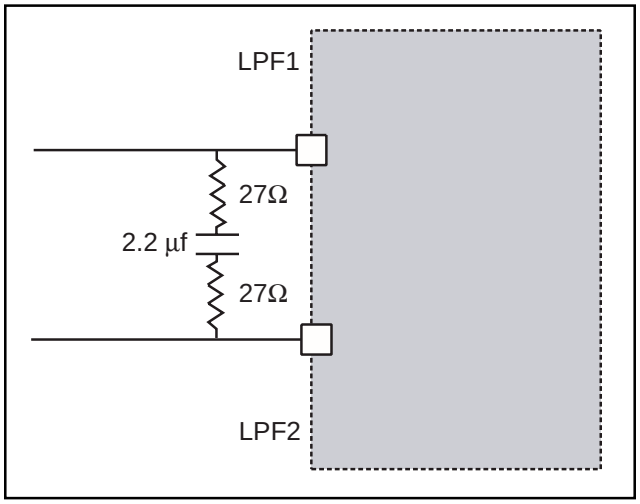


Figure 9. If ALTP/N or DATAP/N not used

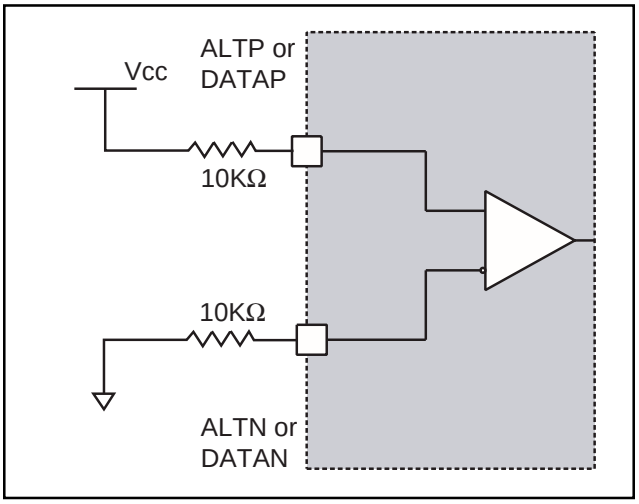
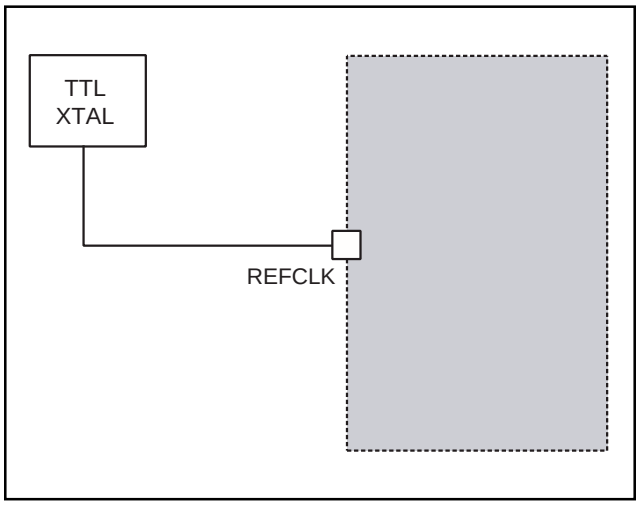


Figure 10. Reference Clock Biasing Circuit



It is recommended that a 148.5 or 74.25 MHz crystal be implemented.

Thermal Information

Device	Power	Θja Still Air
S8301	.52W	65 ˚ C/W

Ordering Information

GRADE	RECEIVER	PACKAGE	TEMPERATURE GRADE	SHIPPING CONFIGURATION
S- Integrated Circuits	8301	TF = 32 TQFP	C- Commercial	Blank = Trays
X Grade	XXXX Part Number	X Package	X Temperature Grade	X Configuration

Example: S8301TF—S8301 in a 32 TQFP package shipped in trays.

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