SE98

SO-DIMM SMBus/I²C-bus temperature sensor

Rev. 02 — 7 January 2008 Product data sheet

1. General description

The NXP Semiconductors SE98 measures temperature from −20 °C and +125 °C communicating via the I²C-bus/SMBus. It is typically mounted on a Dual In-Line Memory Module (DIMM) measuring the DRAM temperature in accordance with the new JEDEC (JC-42.4) *Mobile Platform Memory Module Thermal Sensor Component* specification.

Placing the Temp Sensor (TS) on DIMM allows accurate monitoring of the DIMM module temperature to better estimate the DRAM case temperature (T_{case}) to prevent it from exceeding the maximum operating temperature of 85 °C. The chip set throttles the memory traffic based on the actual temperatures instead of the calculated worst-case temperature or the ambient temperature using a temp sensor mounted on the motherboard. There is up to a 30 % improvement in thin and light notebooks that are using one or two 1G SO-DIMM modules, although other memory modules such as in server applications will also see an increase in system performance. Future uses of the TS will include more dynamic control over thermal throttling, the ability to use the Alarm Window to create multiple temperature zones for dynamic throttling and to save processor time by scaling the memory refresh rate.

The TS consists of an Analog-to-Digital Converter (ADC) that monitors and updates its own temperature readings 8 times per second, converts the reading to a digital data, and latches them into the data temperature registers. User-programmable registers, such as Shutdown or Low-power modes and the specification of temperature event and critical output boundaries, provide flexibility for DIMM temperature-sensing applications.

When the temperature changes beyond the specified boundary limits, the SE98 outputs an $\overline{\text{EVENT}}$ signal. The user has the option of setting the $\overline{\text{EVENT}}$ output signal polarity as either an active LOW or active HIGH comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems. The $\overline{\text{EVENT}}$ output can even be configured as a critical temperature output.

The SE98 supports the industry-standard 2-wire I²C-bus/SMBus serial interface. The SMBus TIMEOUT function is supported to prevent system lock-ups. Manufacturer and Device ID registers provide the ability to confirm the identify of the device. Three address pins allow up to eight devices to be controlled on a single bus. To maintain interchangeability with the I²C-bus/SMBus interface the electrical specifications are specified with the operating voltage of 3.0 V to 3.6 V.

DIMM applications normally use the C-grade accuracy SE98PW or SE98TK temp sensor. For applications requiring the higher B-grade accuracy, the SE98PW/1 or SE98TK/1 is available.

2. Features

2.1 General features

- JEDEC (JC-42.4) SO-DIMM temperature sensor
- Optimized for voltage range: 3.0 V to 3.6 V
- Shutdown/Standby current: 8 µA (typ.) and 15 µA (max.)
- 2-wire interface: I²C-bus/SMBus compatible, 0 Hz to 400 kHz
- SMBus ALERT and TIMEOUT (programmable)
- Available packages: TSSOP8 and HVSON8

2.2 Temperature sensor features

- Temperature-to-Digital converter
- Operating current: 200 µA (typ.) and 250 µA (max.)
- Programmable hysteresis threshold: 0 °C, 1.5 °C, 3 °C, 6 °C
- Over/under/critical temperature EVENT output
- B grade accuracy:
  - ±0.5 °C/±1 °C (typ./max.) → +75 °C to +95 °C
  - ±1 °C/±2 °C (typ./max.) → +40 °C to +125 °C
  - ±2 °C/±3 °C (typ./max.) → –20 °C to +125 °C
- C grade accuracy:
  - ±1 °C/±2 °C (typ./max.) → +75 °C to +95 °C
  - ±2 °C/±3 °C (typ./max.) → +40 °C to +125 °C
  - ±3 °C/±4 °C (typ./max.) → –20 °C to +125 °C

3. Applications

- DDR2 and DDR3 memory modules
- Laptops, personal computers and servers
- Enterprise networking
- Hard disk drives and other PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SE98PW	SE98	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
SE98TK	SE98	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1

5. Block diagram

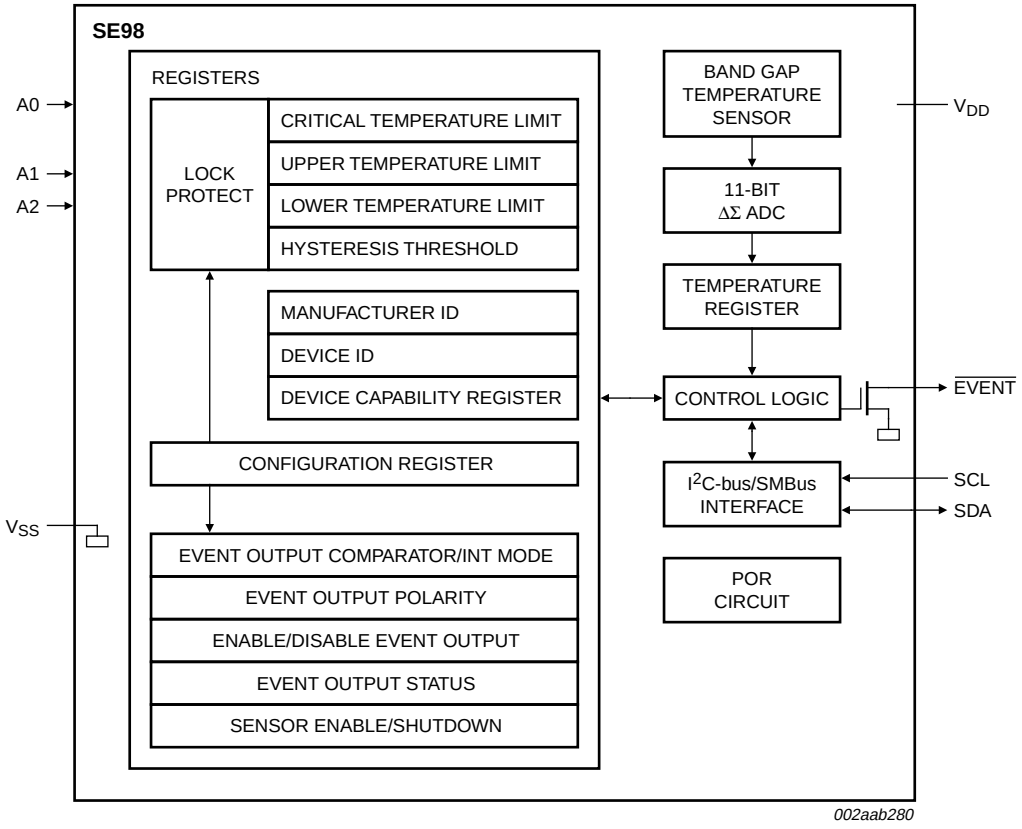


Fig 1. Block diagram of SE98

6. Pinning information

6.1 Pinning

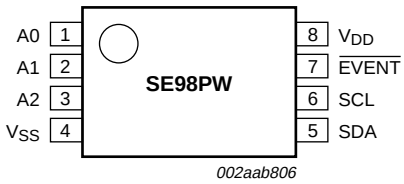


Fig 2. Pin configuration for TSSOP8

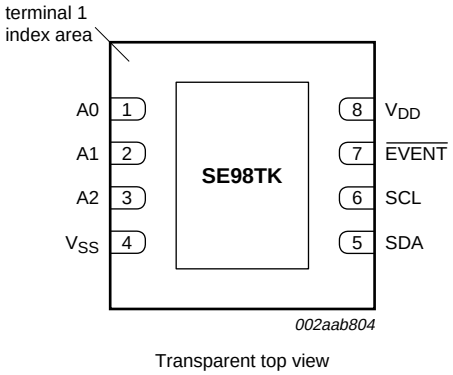


Fig 3. Pin configuration for HVSON8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0[1]	1	I	I²C-bus/SMBus slave address bit 0
A1	2	I	I²C-bus/SMBus slave address bit 1
A2	3	I	I²C-bus/SMBus slave address bit 2
V_{SS}	4	ground	device ground
SDA	5	I/O	SMBus/I²C-bus serial data input/output (open-drain). Must have external pull-up resistor.
SCL	6	I	SMBus/I²C-bus serial clock input/output (open-drain). Must have external pull-up resistor.
$\overline{EVENT}$	7	O	Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor.
V_{DD}	8	power	device power supply (3.0 V to 3.6 V)

[1] In general, application of 10 V on the A0 pin would not damage the pin, but NXP Semiconductors does not guarantee the overvoltage for this pin.

7. Functional description

7.1 Serial bus interface

The SE98 uses the 2-wire serial bus (I2C-bus/SMBus) to communicate with a host controller. The serial bus consists of a clock (SCL) and data (SDA) signals. The device can operate on either the I2C-bus Standard/Fast mode or SMBus. The I2C-bus Standard mode is defined to have bus speeds from 0 Hz to 100 kHz, I2C-bus Fast mode from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE98 uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one bit at a time with the Most Significant Bit (MSB) transferred first, and a complete I2C-bus data is 1 byte. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

7.2 Slave address

The SE98 uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to co-exist on the same bus. The input of each pin is sampled at the start of each I2C-bus/SMBus access. The temperature sensor's fixed address is 0011.

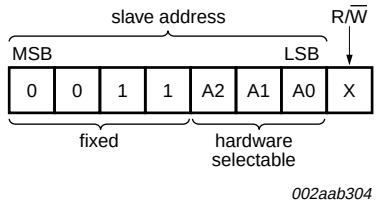
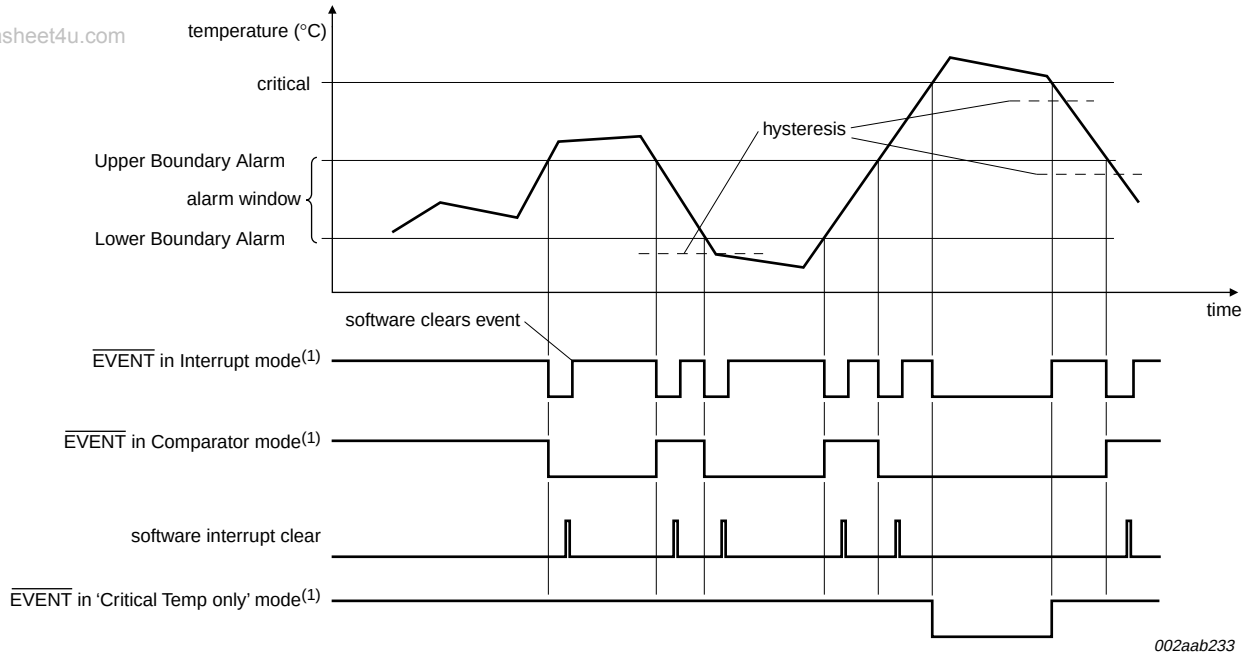


Fig 4. Slave address

7.3 $\overline{\text{EVENT}}$ output

The $\overline{\text{EVENT}}$ pin is an open-drain output whose function can be programmed as an interrupt, comparator, or critical alarm mode. When the device operates in Interrupt mode, and the temperature reaches a critical temperature, the device switches to the comparator mode automatically and asserts the $\overline{\text{EVENT}}$ pin. When the temperature drops below critical temperature, the device reverts back to either interrupt or comparator mode, as programmed in the Configuration register. The interrupt latch can be cleared by writing a '1' to the 'clear $\overline{\text{EVENT}}$' bit in the Configuration register or by performing the SMBus Alert Response Address (ARA).

In comparator mode, the $\overline{\text{EVENT}}$ pin remains asserted until the temperature falls below the value programmed in the Upper Boundary Alarm Trip register or rises above the value programmed in the Lower Boundary Alarm Trip register, or until the range of these alarm registers are reprogrammed and the temperature falls inside the alarm limits. Figure 5 depicts the $\overline{\text{EVENT}}$ output for all the three modes. All event thresholds use hysteresis as programmed in the Configuration register.



(1) $\overline{\text{EVENT}}$ pin shown here is active LOW. It can be programmed to be active HIGH.

Fig 5. $\overline{\text{EVENT}}$ output for 'Interrupt', 'Comparator', and 'Critical Temp only' modes

7.3.1 Alarm window

The alarm window consists of two registers: an Upper Boundary Alarm Trip register (02h), and a Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point. When the $\overline{\text{EVENT}}$ control is enabled, the $\overline{\text{EVENT}}$ output will be triggered whenever entering or exiting the alarm window.

7.3.2 Critical trip

The device can be programmed in such a way that the $\overline{\text{EVENT}}$ output is triggered when the temperature exceeds the critical trip point set by the Critical Alarm Trip register (04h).

When the temperature sensor reaches the critical temperature value, the device is automatically placed in comparator mode; the $\overline{\text{EVENT}}$ output is only cleared when the temperature falls below the critical temperature value and cannot be cleared through the clear $\overline{\text{EVENT}}$ bit or SMBus Alert.

7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE98's conversion rate is at least 8 Hz or 125 ms.

7.5 Power-up default condition

After power-on, the SE98 is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared—$\overline{\text{EVENT}}$ output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0 °C
- Command pointer is defaulted to ‘00h’
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Capability register is defaulted to ‘0015h’
- Operational mode: comparator
- SMBus register is defaulted to ‘00h’

7.6 Device initialization

SE98 temperature sensors have programmable registers, which, upon power-up, default to zero. The open-drain $\overline{\text{EVENT}}$ output is default to being disabled, comparator mode and active LOW. The alarm trigger registers default to being unprotected. The configuration registers, upper and lower alarm boundary registers and critical temperature window are defaulted to zero and need to be programmed to the desired values. SMBus TIMEOUT feature defaults to being enabled and can be programmed to disable. These registers are required to be initialized before the device can properly function. Except for the SPD, which does not have any programmable registers, and does not need to be initialized.

Table 3 shows the default values and the example value to be programmed to these registers.

Table 3. Registers to be initialized

Register	Default value	Example value	Description
01h	0000h	0209h	Configuration register • hysteresis = 1.5 °C • $\overline{\text{EVENT}}$ output = Interrupt mode • $\overline{\text{EVENT}}$ output is enabled
02h	0000h	0550h	Upper Boundary Alarm Trip register = 85 °C
03h	0000h	1F40h	Lower Boundary Alarm Trip register = –20 °C
04h	0000h	05F0h	Critical Alarm Trip register = 95 °C
22h	0000h	0000h	SMBus register = no change

7.7 SMBus Time-out

The SE98 supports the SMBus time-out feature. If the host holds SCL LOW between 25 ms and 35 ms, the SE98 would reset its internal state machine to the bus idle state to prevent the system bus hang-up. This feature is turned on by default. The SMBus time-out is disabled by writing a logic 1 to bit 7 of register 22h.

Remark: When SMBus time-out is enabled, the I²C-bus minimum bus speed is limited by the SMBus time-out timer, and goes down to only 10 kHz.

7.8 SMBus Alert

The SE98 supports SMBus Alert when it is programmed for the Interrupt mode and when the $\overline{\text{EVENT}}$ polarity bit is set to logic 0. The $\overline{\text{EVENT}}$ pin can be ANDed with other $\overline{\text{EVENT}}$ or $\overline{\text{ALERT}}$ signals from other slave devices to signal their intention to communicate with the host controller. When the host detects $\overline{\text{EVENT}}$ or $\overline{\text{ALERT}}$ signal LOW, it issues an Alert Response Address (ARA) to which a slave device would respond with its address. When there are multiple slave devices generating an Alert the SE98 performs bus arbitration. If it wins the bus, it responds to the ARA and then clears the $\overline{\text{EVENT}}$ pin.

Remark: Either in comparator mode or when the SE98 crosses the critical temperature, the host must also read the $\overline{\text{EVENT}}$ status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the $\overline{\text{EVENT}}$ pin will not get de-asserted.

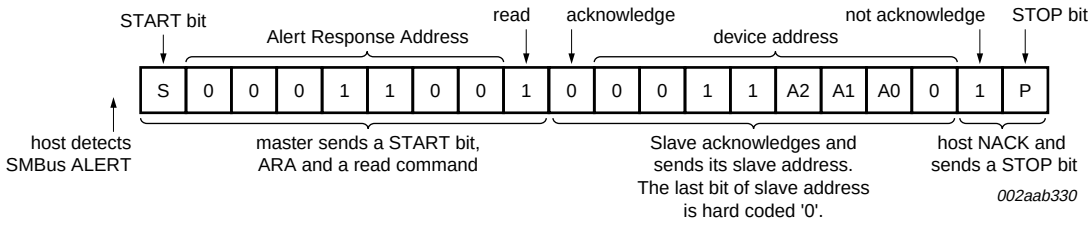


Fig 6. How SE98 responds to SMBus Alert

7.9 SMBus/I²C-bus interface

The data registers in this device are selected by the Pointer register. At power-up, the Pointer register is set to ‘00’, the location for the Capability register. The Pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

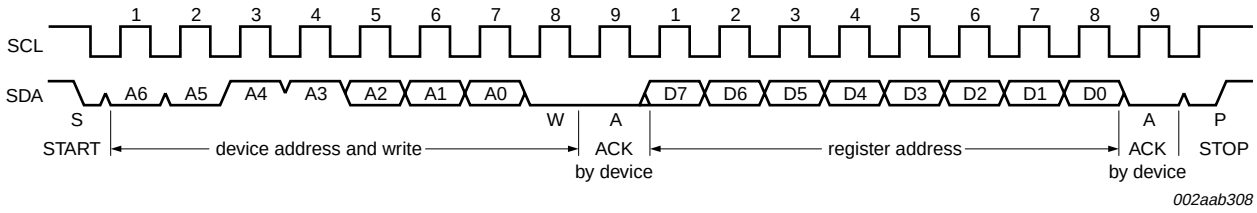
- Read only
- Write only
- Write/Read same address.

A ‘write’ to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Reading this device can take place either of two ways:

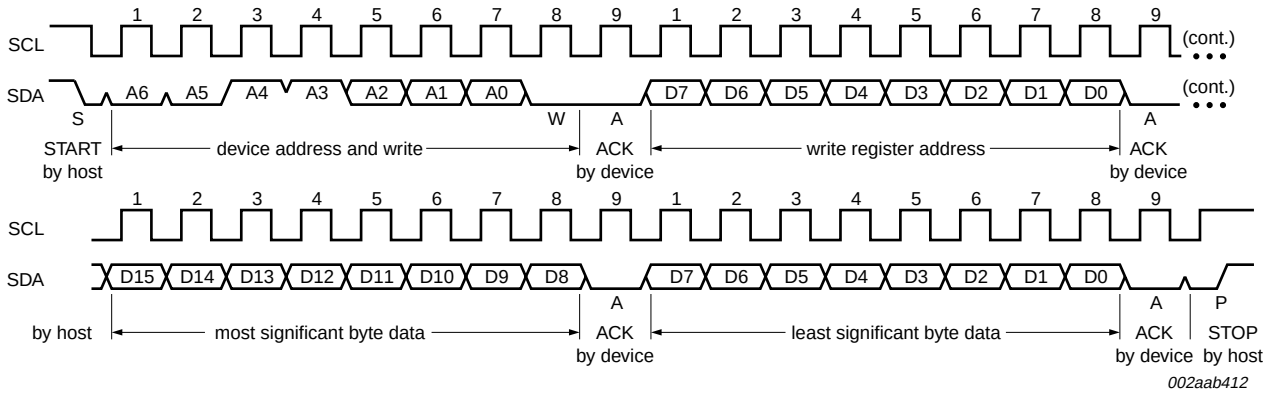
- If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Temperature register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to the timing diagrams in Figure 7, Figure 8, Figure 9 and Figure 10 on how to program the device.



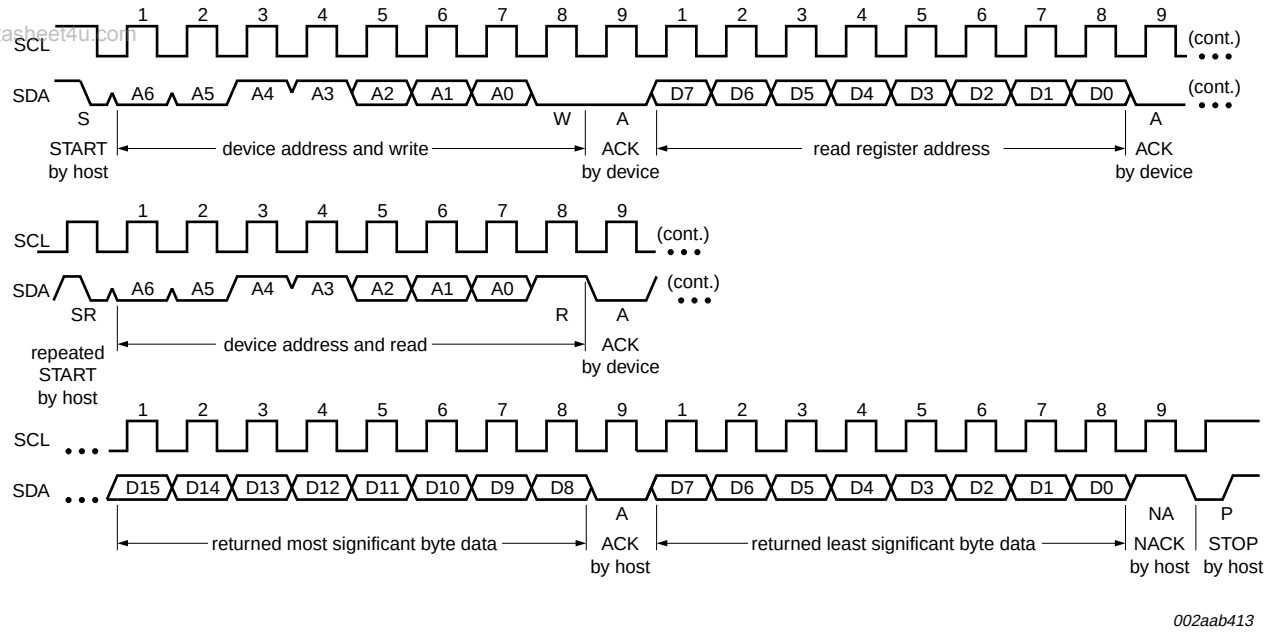
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 7. SMBus/I²C-bus write to the Pointer register



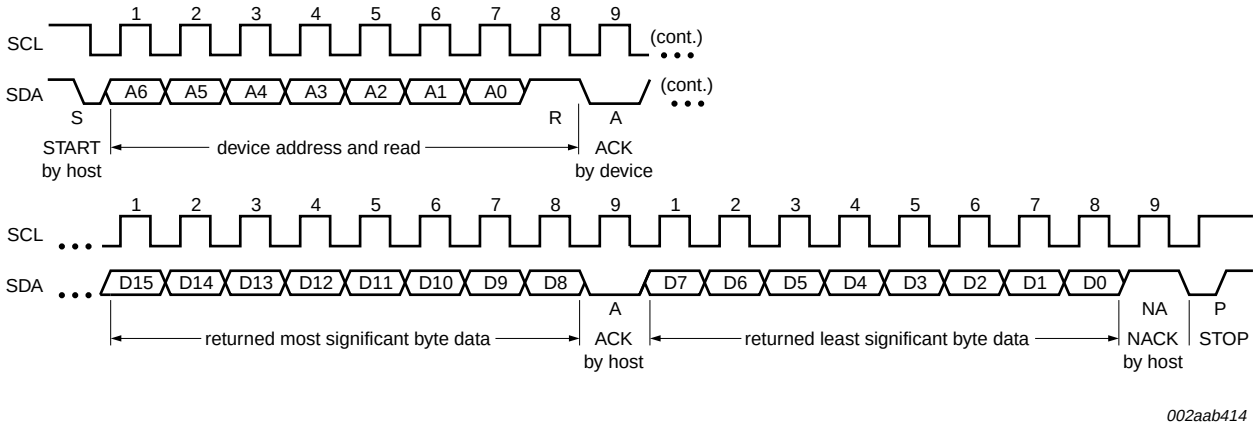
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 8. SMBus/I²C-bus write to the Pointer register followed by a write data word



A = ACK = Acknowledge bit. NA = Not Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 9. SMBus/I²C-bus write to Pointer register followed by a repeat START and an immediate data word read



A = ACK = Acknowledge bit. NA = Not Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 10. SMBus/I²C-bus word read from register with a pre-set pointer

8. Register descriptions

8.1 Register overview

This section describes all the registers used in the SE98. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the Pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading zeroes. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

Table 4. Register summary

Address	POR state	Register name
n/a	n/a	Pointer register
00h	0015h/0017h	Capability register (B-grade = 0017h, C-grade = 0015h)
01h	0000h	Configuration register
02h	0000h	Upper Boundary Alarm Trip register
03h	0000h	Lower Boundary Alarm Trip register
04h	0000h	Critical Alarm Trip register
05h	n/a	Temperature register
06h	1131h	Manufacturer ID register
07h	A101h	Device ID/Revision register
08h to 21h	0000h	reserved registers
22h	0000h	SMBus register
23h to FFh	0000h	reserved registers

A write to reserved registers my cause unexpected results which may result in requiring a reset by removing and re-applying its power.

8.2 Capability register (00h, 16-bit read-only)

Table 5. Capability register (address 00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU[10:3]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RFU[2:0]			TRES[1:0]		WRNG	HACC	BCAP
Reset	0	0	0	1	0	1	0	1
Access	R	R	R	R	R	R	R	R

Table 6. Capability register (address 00h) bit description

Bit	Symbol	Description
15:5	RFU	Reserved for future use. Must be zero.
4:3	TRES	Temperature resolution. 10 — 0.125 °C LSB
2	WRNG	Wider range. 1 — can read temperatures below 0 °C and set sign bit accordingly
1	HACC	Higher accuracy bit set during manufacture. 0 — Accuracy ±2 °C over the active range and ±3 °C over the monitor range (C-grade) 1 — High accuracy ±1 °C over the active range and ±2 °C over the monitor range (B-grade)
0	BCAP	Basic capability. 1 — Has Alarm and Critical Trips capability.

8.3 Configuration register (01h, 16-bit read/write)

Table 7. Configuration register (address 01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU					HEN[1:0]		SHMD
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CTLB	AWLB	CEVNT	ESTAT	EOCTL	CVO	EP	EMD
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8. Configuration register (address 01h) bit description

Bit	Symbol	Description
15:11	RFU	reserved for future use; must be ‘0’.
10:9	HEN	Hysteresis Enable 00 — Disable hysteresis (default) 01 — Enable hysteresis at 1.5 °C 10 — Enable hysteresis at 3 °C 11 — Enable hysteresis at 6 °C When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the ‘Above Alarm Window’ bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to 1 (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to Figure 5 and Table 9). Similarly, the ‘Below Alarm Window’ bit (bit 13 of the Temperature register) will be set to 0 (temperature is equal to or above the Alarm Window Lower Boundary Trip register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary register. As the temperature decreases, bit 13 will be set to 1 when the value in the Temperature register is equal to or less than the value in the Alarm Temperature Lower Boundary register minus 3 °C. Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set, these bits cannot be altered.
8	SHMD	Shutdown Mode. 0 — Enabled Temperature Sensor (default) 1 — Disabled Temperature Sensor When shut down, the thermal sensor diode and Analog-to-Digital Converter (ADC) are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time.

Table 8. Configuration register (address 01h) bit description *…continued*

Bit	Symbol	Description
7	CTLB	Critical Trip Lock bit. 0 — Critical Alarm Trip register is not locked and can be altered (default). 1 — Critical Alarm Trip register settings cannot be altered. This bit is initially cleared. When set, this bit will return a 1, and remains locked until cleared by internal Power-on reset. This bit can be written with a single write and do not require double writes.
6	AWLB	Alarm Window Lock bit. 0 — Upper and Lower Alarm Trip registers are not locked and can be altered (default). 1 — Upper and Lower Alarm Trip registers setting cannot be altered. This bit is initially cleared. When set, this bit will return a 1 and remains locked until cleared by internal power-on reset. This bit can be written with a single write and does not require double writes.
5	CEVNT	Clear $\overline{\text{EVENT}}$ (write only). 0 — No effect (default). 1 — Clears active $\overline{\text{EVENT}}$ in Interrupt mode. Writing to this register has no effect in Comparator mode. When read, this register always returns zero.
4	ESTAT	$\overline{\text{EVENT}}$ Status (read only). 0 — $\overline{\text{EVENT}}$ output condition is not being asserted by this device (default). 1 — $\overline{\text{EVENT}}$ output pin is being asserted by this device due to Alarm Window or Critical Trip condition. The actual event causing the event can be determined from the Read Temperature register. Interrupt Events can be cleared by writing to the 'clear $\overline{\text{EVENT}}$' bit. Writing to this bit will have no effect.
3	EOCTL	$\overline{\text{EVENT}}$ Output Control. 0 — $\overline{\text{EVENT}}$ output disabled (default). 1 — $\overline{\text{EVENT}}$ output enabled. When either of the lock bits is set, this bit cannot be altered until unlocked.
2	CVO	Critical Event Only. 0 — $\overline{\text{EVENT}}$ output on Alarm or Critical temperature event (default) 1 — $\overline{\text{EVENT}}$ only if temperature is above the value in the critical temperature register When the alarm window lock bit is set, this bit cannot be altered until unlocked.
1	EP	$\overline{\text{EVENT}}$ Polarity. 0 — active LOW (default). 1 — active HIGH. When either of the alarm or critical lock bits is set, this bit cannot be altered until unlocked.
0	EMD	$\overline{\text{EVENT}}$ Mode. 0 — comparator output mode (default) 1 — interrupt mode When either of the alarm or critical lock bits is set, this bit cannot be altered until unlocked.

Table 9. Hysteresis Enable

Action	Below Alarm Window Bit (bit 13)		Above Alarm Window Bit (bit 14)	
	Temperature slope	Threshold temperature	Temperature slope	Temperature
sets	falling	$T_{th(low)}$ – Hysteresis	rising	$T_{th(high)}$
clears	rising	$T_{th(low)}$	falling	$T_{th(high)}$ – Hysteresis

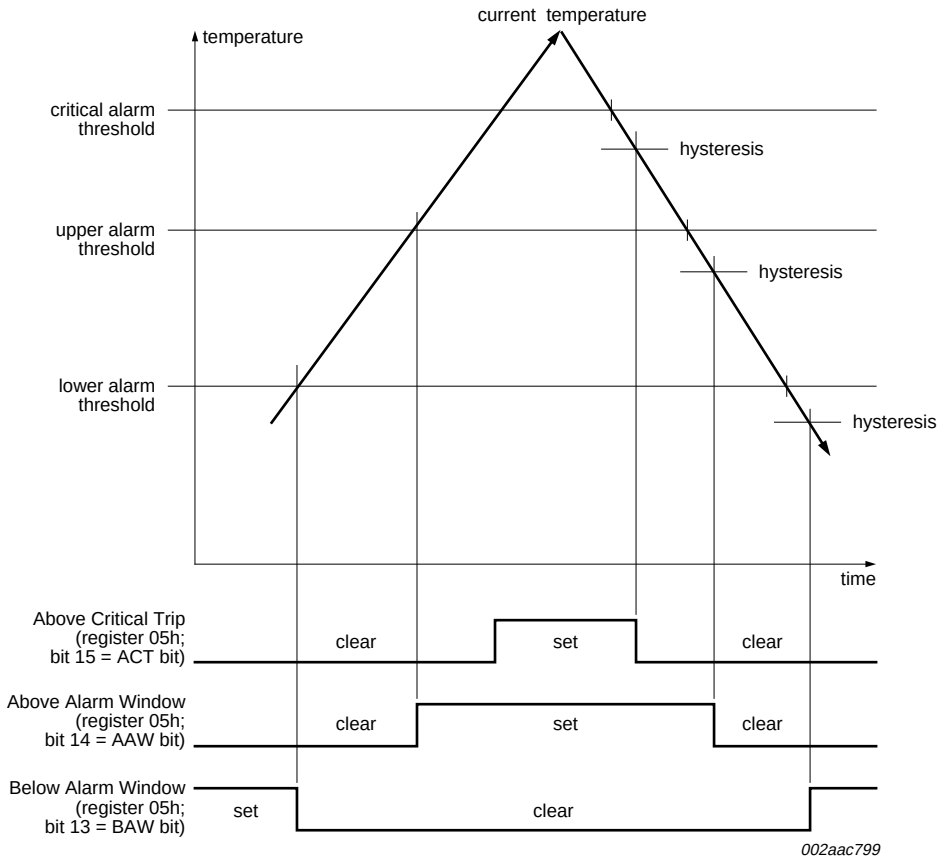


Fig 11. Hysteresis: how it works

8.4 Temperature format

The 16-bit value used in the following Trip Point Set and Temperature Read-Back registers is 2's complement with the Least Significant Bit (LSB) equal to 0.0625 °C. For example:

- A value of 019Ch will represent 25.75 °C
- A value of 07C0h will represent 124 °C
- A value of 1E64h will represent –25.75 °C.

The resolution is 0.125 °C. The unused LSB (bit 0) is set to '0'. Bit 11 will have a resolution of 128 °C.

The upper 3 bits of the temperature register indicate Trip Status based on the current temperature, and are not affected by the status of the Event Output.

8.5 Temperature Trip Point registers

8.5.1 Upper Boundary Alarm Trip register (16-bit read/write)

The value is the upper threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. 'RFU' bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 10. Upper Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	UBT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	UBT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 11. Upper Boundary Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	UBT	Upper Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

8.5.2 Lower Boundary Alarm Trip register (16-bit read/write)

The value is the lower threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 12. Lower Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	LBT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LBT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 13. Lower Boundary Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	LBT	Lower Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

8.5.3 Critical Alarm Trip register (16-bit read/write)

The value is the critical temperature. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero.

Table 14. Lower Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	CT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 15. Critical Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	CT	Critical Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

8.6 Temperature register (16-bit read-only)

Table 16. Temperature register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ACT	AAW	BAW	SIGN	TEMP[10:7]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TEMP[6:0]							RFU
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 17. Temperature register bit description

Bit	Symbol	Description
15	ACT	Above Critical Trip. 0 — temperature is below the Critical Alarm Trip register setting 1 — temperature is equal to or above the Critical Alarm Trip register setting
14	AAW	Above Alarm Window. 0 — temperature is equal to or below the Upper Boundary Alarm Trip register 1 — temperature is above the Alarm window
13	BAW	Below Alarm Window. 0 — temperature is equal to or above the Lower Boundary Alarm Trip register 1 — temperature is below the Alarm window
12	SIGN	Sign bit. 0 — positive temperature value 1 — negative temperature value
11:1	TEMP	Temperature Value (2's complement). (LSB = 0.125 °C)
0	RFU	reserved; always 0

8.7 Manufacturer's ID register (16-bit read-only)

The manufacture's ID matches that assigned to NXP Semiconductors PCI SIG (1131h), and is intended for use to identify the manufacturer of the device.

Table 18. Manufacturer's ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Manufacturer ID							
Reset	0	0	0	1	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	(continued)							
Reset	0	0	1	1	0	0	0	1
Access	R	R	R	R	R	R	R	R

8.8 Device ID register

The device ID and device revision are A1h and 00h, respectively.

Table 19. Device ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Device ID							
Reset	1	0	1	0	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Device revision							
Reset	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R

8.9 SMBus register

Table 20. SMBus Time-out register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	STMOUT	RFU						SALRT
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R/W

Table 21. SMBus Time-out register bit description

Bit	Symbol	Description
15:8	RFU	reserved; always 0
7	STMOUT	SMBus time-out. 0 — SMBus time-out is enabled (default) 1 — disable SMBus time-out When either of the lock bits is set, this bit cannot be altered until unlocked.
6:1	RFU	reserved; always 0
0	SALRT	SMBus Alert. 0 — SMBus Alert is enabled (default) 1 — disable SMBus Alert When either of the lock bits is set, this bit cannot be altered until unlocked.

9. Application design-in information

In a typical application, the SE98 behaves as a slave device and interfaces to the master (or host) via the SCL and SDA lines. The host monitors the $\overline{\text{EVENT}}$ output pin, which is asserted when the temperature reading exceeds the programmed values in the alarm registers. The A0, A1 and A2 pins are directly connected to the shared SPD's A0, A1 and A2 pins, otherwise they must be pulled HIGH or LOW. The SDA and SCL serial interface pins are open-drain and require pull-up resistors, and are able to sink a maximum current of 3 mA with a voltage drop less than 0.4 V. Typical pull-up values for SCL and SDA are 10 kΩ, but the resistor values can be changed in order to meet the rise time requirement if the capacitance load is too large due to routing, connectors, or multiple components sharing the same bus.

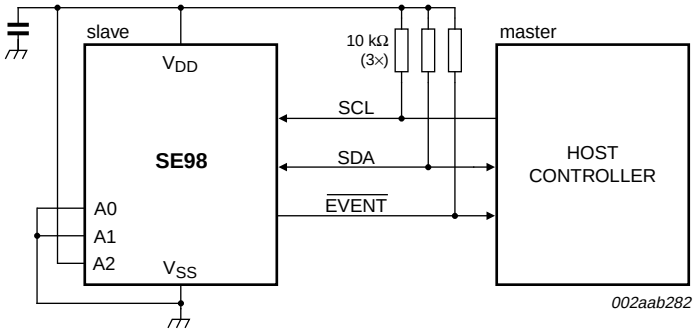


Fig 12. Typical application

9.1 SE98 in memory module application

Figure 13 shows the SE98 being placed in the memory module application. The SE98 is centered in the memory module to provide the function to monitor the temperature of the DRAM. In the event of overheat, the SE98 triggers the $\overline{\text{EVENT}}$ output and the memory controller can throttle the memory bus to slow the DRAM, or the CPU can increase the refresh rate for the DRAM. The memory controller can also read the SE98 and watch the DRAM thermal behavior.

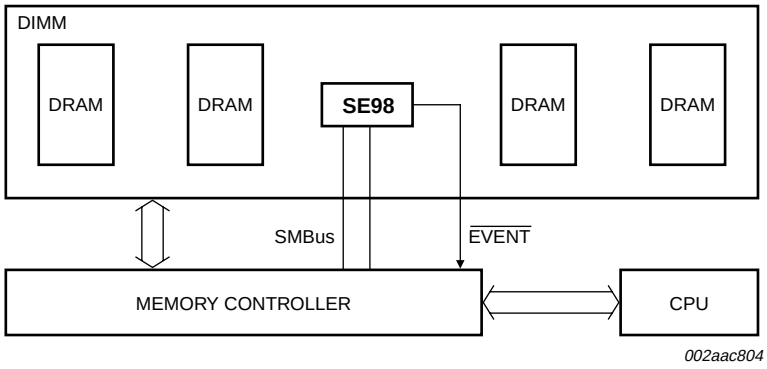


Fig 13. System application

9.2 Layout consideration

The SE98 does not require any additional components other than the host controller to measure temperature. A 0.1 µF bypass capacitor between the V_{DD} and V_{SS} pins is located as close as possible to the power and ground pins for noise protection.

9.3 Thermal considerations

In general, self-heating is the result of power consumption and not a concern, especially with the SE98, which consumes very low power. In the event the SDA and $\overline{\text{EVENT}}$ pins are heavily loaded with small pull-up resistor values, self-heating affects temperature accuracy by approximately 0.5 °C.

Equation 1 is the formula to calculate the effect of self-heating:

$$T\Delta = R_{th(j\text{-}a)} \times [(V_{DD} \times I_{DD}) + (V_{OL1} \times I_{OL1}) + (V_{OL2} \times I_{OL2})] \quad (1)$$

where:

$T\Delta = T_j - T_{amb}$

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = package thermal resistance

V_{OL1} = SDA output low voltage

V_{OL2} = $\overline{\text{EVENT}}$ output low voltage

I_{OL1} = SDA output current LOW

I_{OL2} = $\overline{\text{EVENT}}$ output current LOW.

10. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.2	V
V_n	voltage on any other pin	SDA, SCL, $\overline{\text{EVENT}}$ pins	–0.3	+4.2	V
V_{A0}	voltage on pin A0	overvoltage input; A0 pin	–0.3	+10	V
I_{sink}	sink current	at SDA, SCL, $\overline{\text{EVENT}}$ pins	–1	+50.0	mA
V_{esd}	electrostatic discharge voltage	HBM	-	2500	V
		MM	-	250	V
		CDM	-	1000	V
$T_{j(max)}$	maximum junction temperature		-	150	°C
T_{stg}	storage temperature		–65	+165	°C

[1] In general, application of 10 V on the A0 pin would not damage the pin, but NXP Semiconductors does not guarantee the overvoltage for this pin.

11. Characteristics

Table 23. Characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −20 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{lim(acc)}$	temperature limit accuracy	B-grade temperature accuracy; V_{DD} = 3.3 V ± 10 %				
		T_{amb} = 75 °C to 95 °C	−1.0	< ±0.5	+1.0	°C
		T_{amb} = 40 °C to 125 °C	−2.0	< ±1	+2.0	°C
		T_{amb} = −20 °C to +125 °C	−3.0	< ±2	+3.0	°C
		C-grade temperature accuracy; V_{DD} = 3.3 V ± 10 %				
		T_{amb} = 75 °C to 95 °C	−2.0	< ±1	+2.0	°C
		T_{amb} = 40 °C to 125 °C	−3.0	< ±2	+3.0	°C
		T_{amb} = −20 °C to +125 °C	−4.0	< ±3	+4.0	°C
T_{res}	temperature resolution		-	0.25	-	°C
$I_{DD(AV)}$	average supply current		-	-	250	µA
$I_{DD(stb)}$	standby supply current	SMBus inactive	-	8	15	µA
T_{conv}	conversion period		-	100	-	ms
$E_{f(conv)}$	conversion rate error	percentage error in programmed data	−30	-	+30	%
I_L	leakage current	on A0, A1, A2 pins	-	1	-	µA
V_{DD}	supply voltage		3.0	3.3	3.6	V

Table 24. SMBus DC characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −20 °C to +120 °C; unless otherwise specified. These specifications are guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	SCL, SDA; V_{DD} = 3.0 V to 3.6 V	2.2	-	-	V
V_{IL}	LOW-level input voltage	SCL, SDA; V_{DD} = 3.0 V to 3.6 V	-	-	0.8	V
$I_{OL(sink)EVENT\_N}$	LOW-level output sink current on pin $\overline{EVENT}$	V_{OL} = 0.4 V	1	-	-	mA
$I_{OL(sink)(SDA)}$	LOW-level output sink current on pin SDA	V_{OL} = 0.6 V	6	-	-	mA
I_{LOH}	HIGH-level output leakage current	$V_{OH} = V_{DD}$	-	-	1.0	µA
I_{LIH}	HIGH-level input leakage current	$V_I = V_{DD}$ or V_{SS}	−1.0	-	+1.0	µA
I_{LIL}	LOW-level input leakage current	$V_I = V_{DD}$ or V_{SS}	−1.0	-	+1.0	µA
C_i	input capacitance	SCL, SDA pins	-	5	10	pF

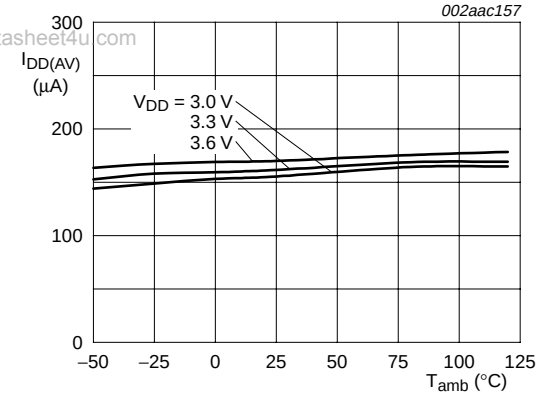


Fig 14. Supply current versus temperature

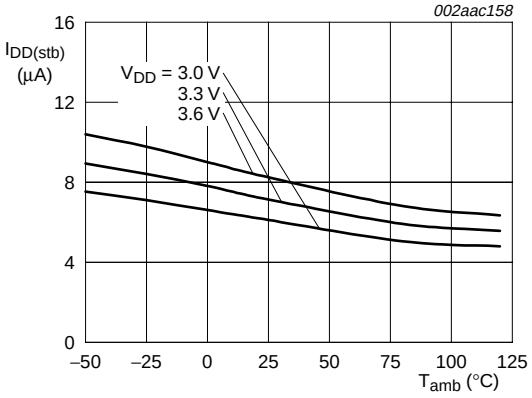


Fig 15. Standby supply current versus temperature

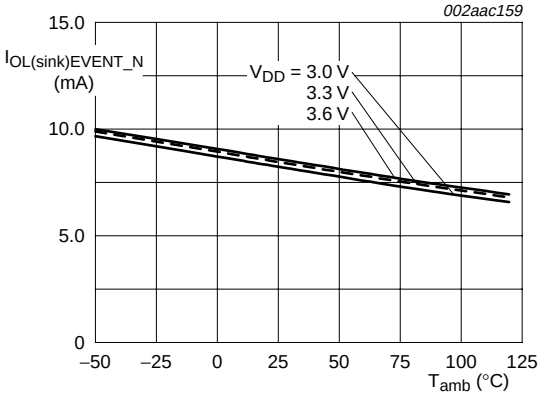


Fig 16. $\overline{\text{EVENT}}$ sink current at 0.4 V versus temperature

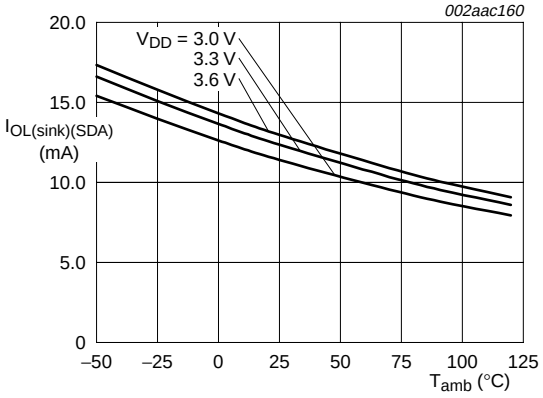
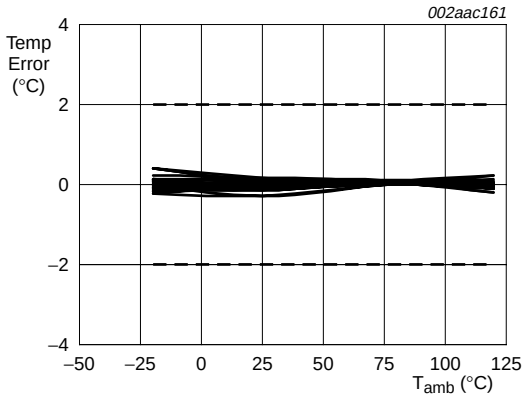


Fig 17. $\overline{\text{EVENT}}$ sink current at 0.6 V versus temperature



Sample of 25 devices at V_{DD} = 3.3 V

Fig 18. Temperature Error versus temperature

Table 25. SMBus AC characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −20 °C to +120 °C; unless otherwise specified. These specifications are guaranteed by design. The AC specifications fully meet or exceed SMBus 2.0 specifications, but allow the bus to interface with the I²C-bus from DC to 400 kHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			0	-	400	kHz
t_{LOW}	LOW period of the SCL clock	10 % to 10 %		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock	90 % to 90 %		0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	10 % of SDA to 90 % of SCL	[1]	4.7	-	-	µs
$t_{HD;DAT}$	data hold time		[2]	300	-	-	ns
$t_{SU;DAT}$	data set-up time			250	-	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		[3]	250	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	300	ns
t_f	fall time of both SDA and SCL signals			-	-	300	ns
$t_{f(o)}$	output fall time			-	-	250	ns
$t_{to(SMBus)}$	SMBus time-out time		[4]	25	-	35	ms

[1] Delay from SDA START to first SCL HIGH-to-LOW transition.

[2] Delay from SCL HIGH-to-LOW transition to SDA edges.

[3] Delay from SCL LOW-to-HIGH transition to restart SDA.

[4] LOW period to reset SMBus.

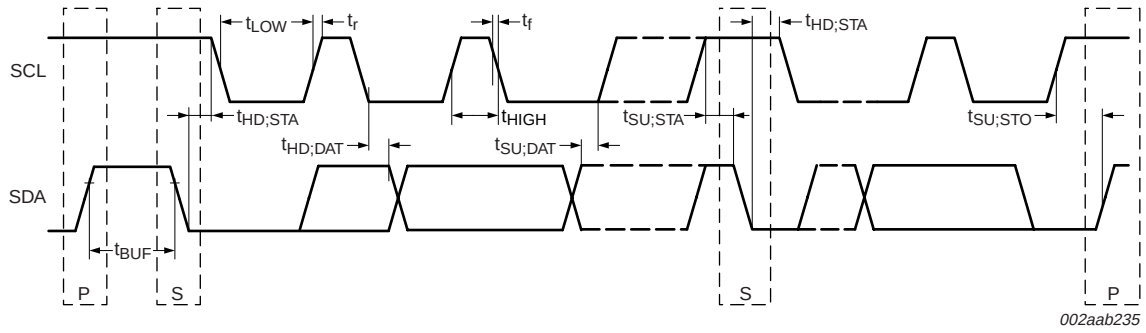
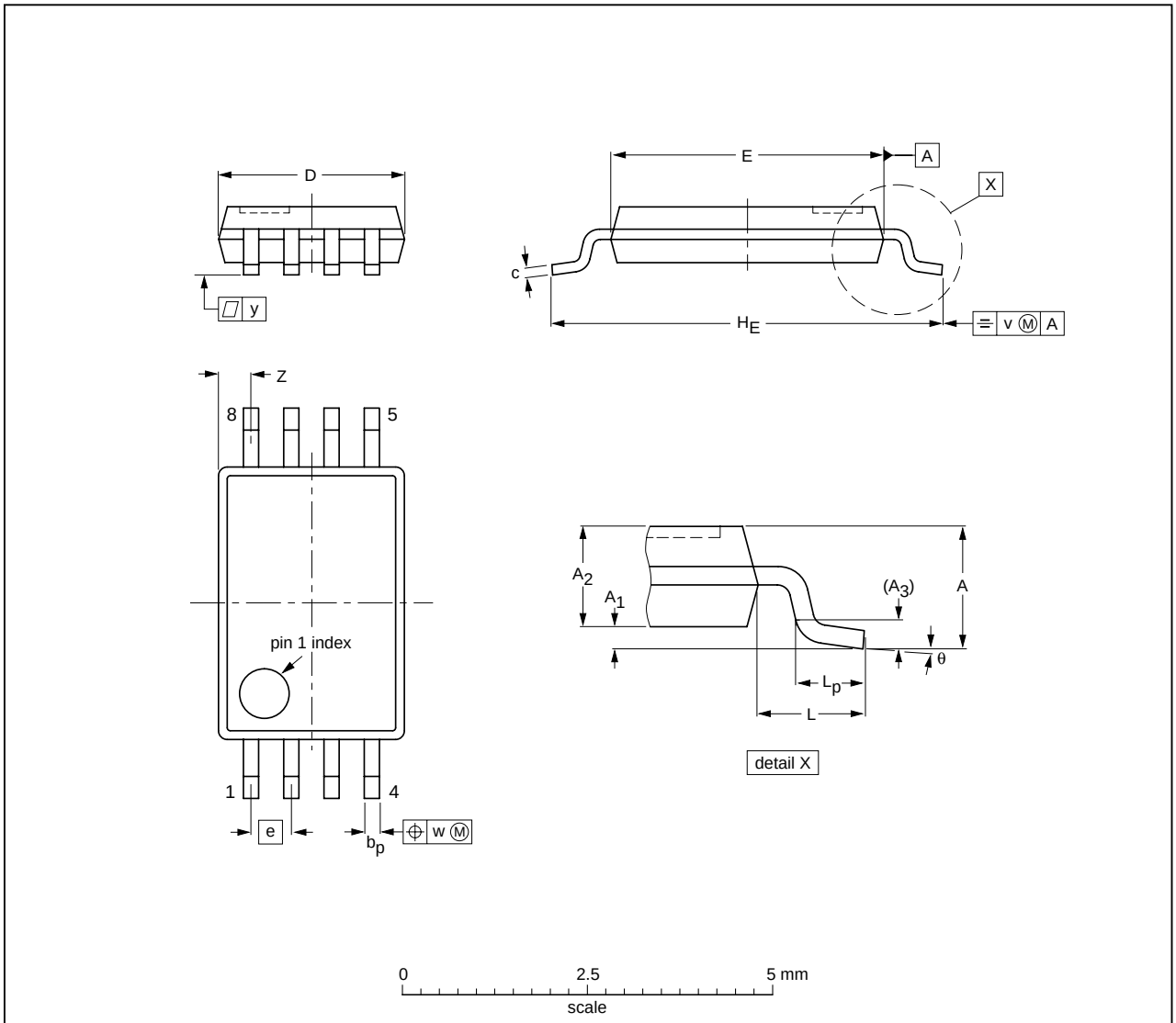


Fig 19. AC timing diagram

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

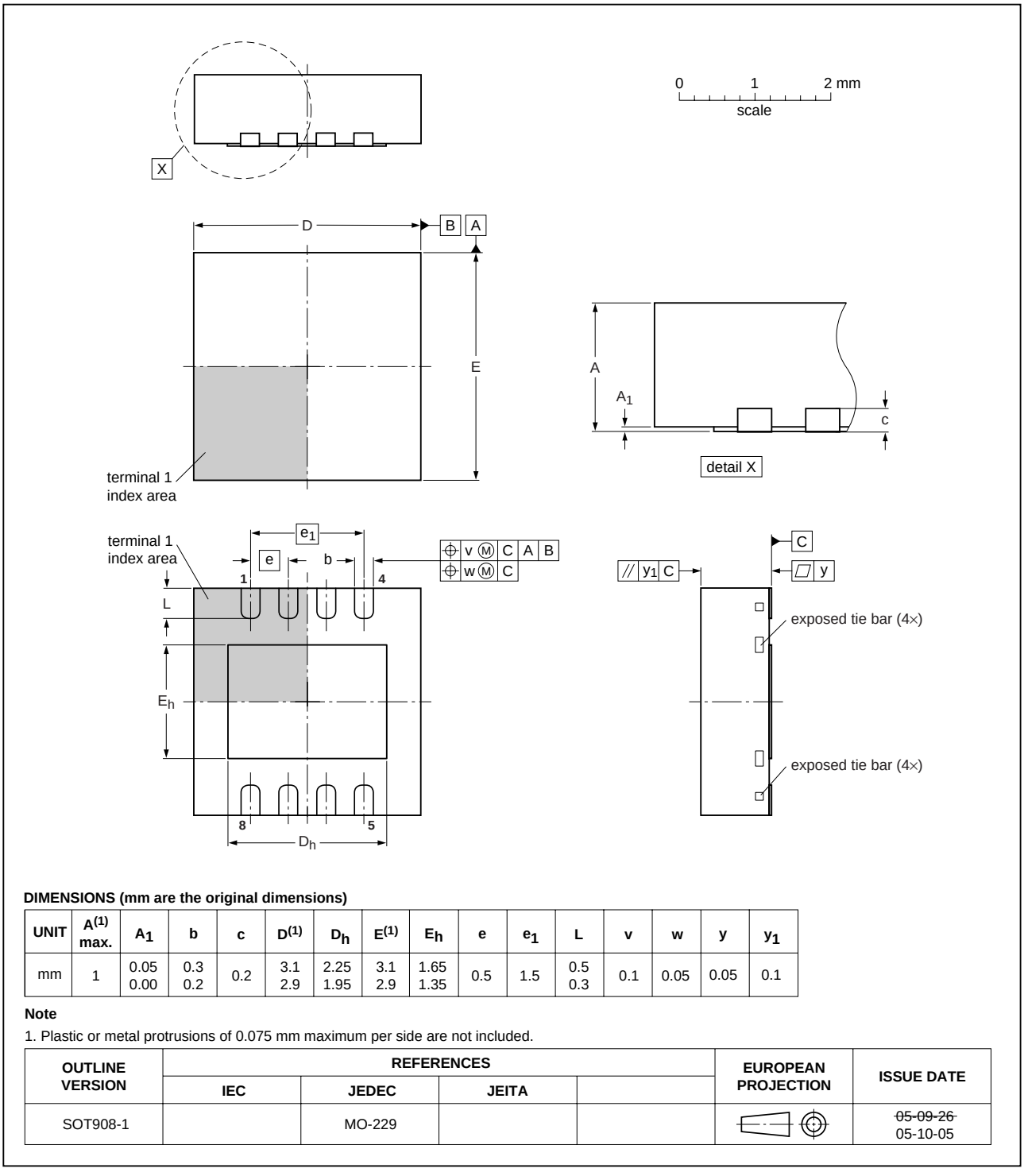
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 20. Package outline SOT530-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT908-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				~~05-09-26~~ 05-10-05

Fig 21. Package outline SOT908-1 (HVSON8)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 26 and 27

Table 26. SnPb eutectic process (from J-STD-020C)

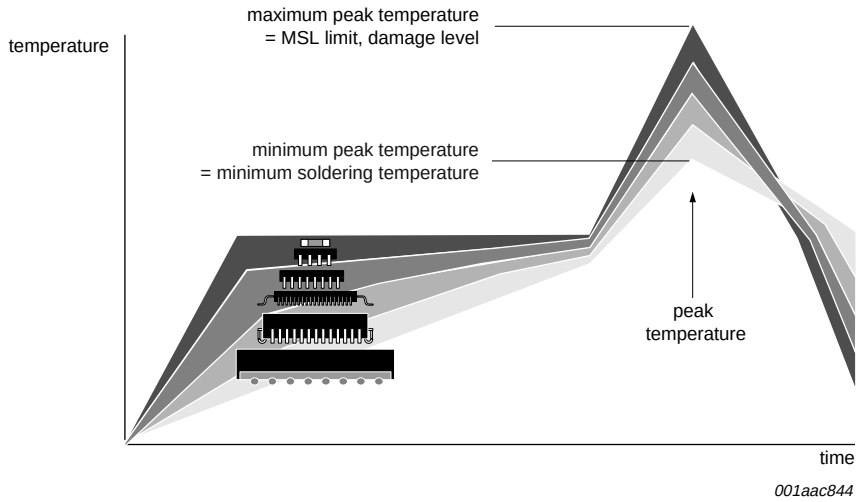
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 27. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 28. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ARA	Alert Response Address
CDM	Charged Device Model
DIMM	Dual In-line Memory Module
HBM	Human Body Model
I²C-bus	Inter IC bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
SO-DIMM	Small Outline Dual In-line Memory Module
POR	Power-On Reset
SMBus	System Management Bus
SPD	Serial Presence Detect

15. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SE98_2	20080107	Product data sheet	-	SE98_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 “General description” re-written • Section 2 “Features” re-written • Table 1 “Ordering information”: removed type numbers SE98PW/1 and SE98TK/1 • Section 6 “Pinning information”: – changed pin name “V_{CC}” to “V_{DD}”; changed pin name “GND” to “V_{SS}” – deleted SE98PW/1 from Figure 2 “Pin configuration for TSSOP8” – deleted SE98TK/1 from Figure 3 “Pin configuration for HVSON8” • Table 2 “Pin description”: added Table note 1 and its reference at pin A0 • Figure 5 “EVENT output for ‘Interrupt’, ‘Comparator’, and ‘Critical Temp only’ modes” modified • Section 7.5 “Power-up default condition” re-written • Added (new) Section 7.6 “Device initialization” • Table 5 “Capability register (address 00h) bit allocation”: – deleted Table note 1 and its reference – changed Reset value for bit 1 from (reference to Table note 1) to “0” • Table 6 “Capability register (address 00h) bit description”: description of bit HACC modified • Figure 11 “Hysteresis: how it works” modified • Section 9 “Application design-in information” re-written • Table 22 “Limiting values” re-written • Table 23 “Characteristics”: added descriptive text below table’s title • Titles of Figure 14, Figure 15, Figure 16 and Figure 17 re-written			
SE98_1 (9397 750 14649)	20060510	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

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18. Contents

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