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SSI 34P553/5531
Pulse Detector & Data Synchronizer

December 1993

DESCRIPTION

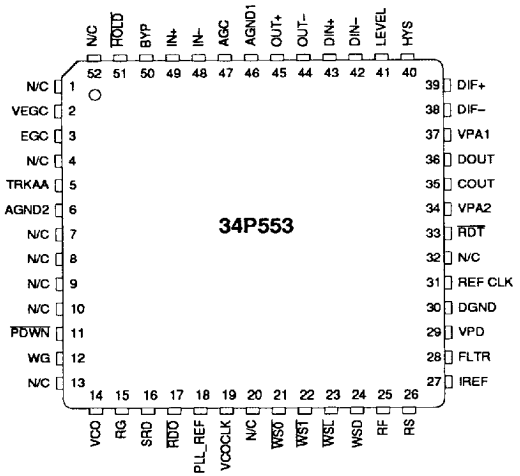
The SSI 34P553/5531 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier. The data synchronization portion is an MFM and 1, 7 data synchronizer with window shift capability. The SSI 34P553/5531 achieves low system operating power two ways, with a low operating power (+5V only design) and with a power down mode. The power down mode is a complete shutdown or sleep mode. The SSI 34P553/5531 is available in a 52-lead fine pitch QFP package.

The 34P5531 is the same device, but with separate CIN+, CIN- inputs, for use with active filters such as the SSI 32F8030 (a 2 kΩ resistor would be placed across DIF+/DIF- in this case).

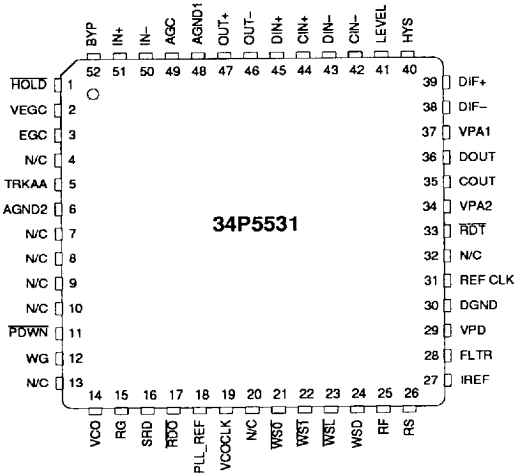
FEATURES

- **Highly Integrated Pulse Detector and Data Synchronizer**
- **+5V only Power Supplies**
- **790 mW max. power**
- **Low Pulse Pairing**
- **0.6-1.6 Mbit/s operation**

PIN DIAGRAMS



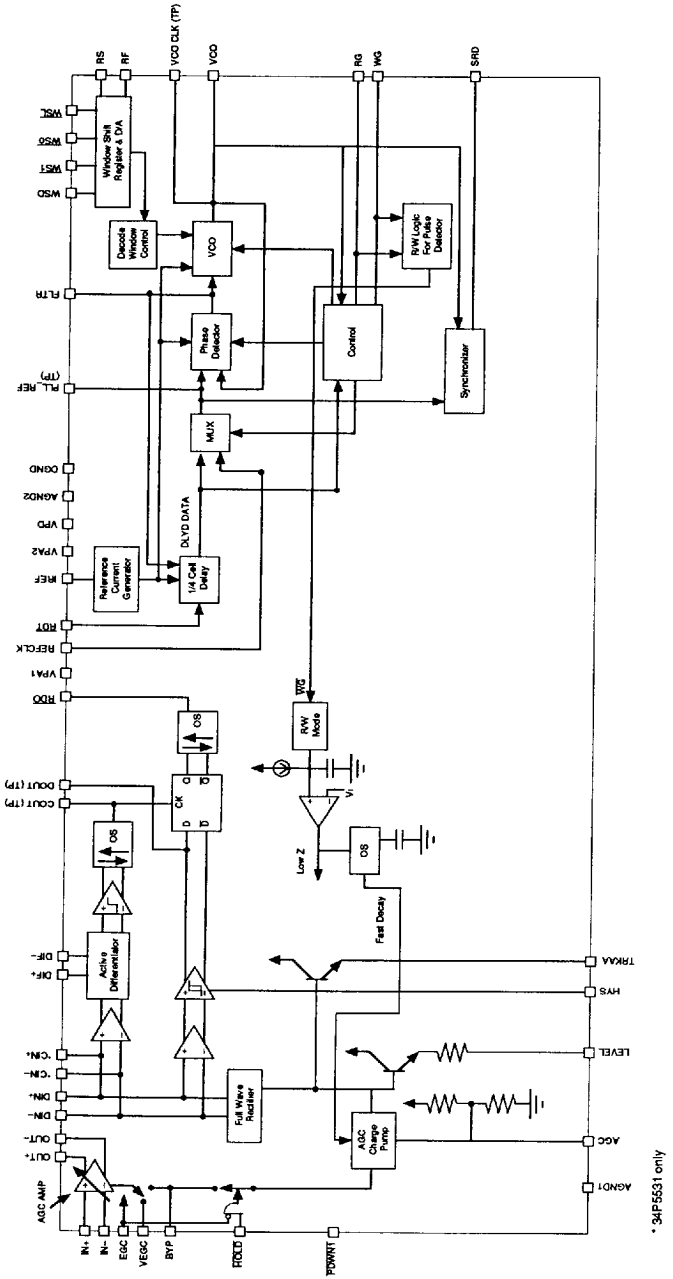
52-Lead QFP



52-Lead QFP

CAUTION Use handling procedures necessary for a static sensitive component

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

PULSE DETECTOR SECTION

READ MODE

The SSI 34P553/5531 enters into the Read mode when the WG pin is pulled low. In the Read mode, the SSI 34P553/5531 provides amplification and pulse level qualification of the signal applied to the input pins of the AGC amplifier.

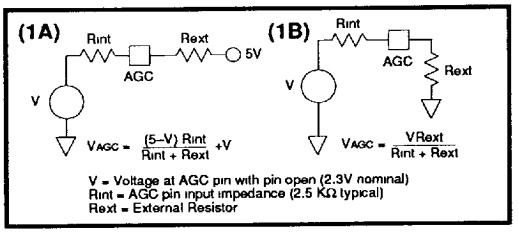
AGC AMPLIFIER

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. To control the gain of the AGC amplifier, the signal at the DIN± pins is full-wave rectified and amplified. The resulting voltage is compared to the voltage level present at the AGC pin. If the voltage level is higher than the AGC pin reference level, the SSI 34P553/5531 will enter into an Attack mode. If it is lower than the AGC pin voltage the device will enter into a Decay mode.

Attack Mode. The SSI 34P553/5531 contains a dual rate attack charge pump that is controlled by the instantaneous level at DIN±. When the voltage from the full wave rectifier exceeds the AGC pin voltage by greater than 125%, a Fast Attack mode is entered. During fast attack, 1.4 mA of current is supplied to the network on the BYP pin. When the full wave rectifier voltage exceeds the AGC pin voltage by 100 to 125%, the Slow Attack mode is entered. During slow attack the charge current supplied to the BYP pin is 0.18 mA. This dual rate charge pump allows the AGC to recover rapidly during write to read transitions while minimizing distortion once the AGC amplitude is within range.

Decay Mode. Two internally controlled Decay modes are provided by the SSI 34P553/5531. Upon a switch to Write mode, the device holds the gain at its last value and the AGC inputs are switched to low impedance. When the device is switched back from write to read, the gain remains held and the AGC inputs remain in a low impedance state for 0.9 µs. At this time, if the new gain required is more than the held value the device enters into the Decay mode. A fast decay current of 0.12 mA is automatically switched on for a period of 0.9 µs. After 0.9 µs the device will sink a steady state slow decay current of 4.5 µA (reference Figure 7.)

AGC Level Control. The AGC level is controlled by the voltage presented on the AGC pin. The AGC pin is internally biased at approximately 2.3V which sets the signal at the DIN± pins to 1.0 Vpp under nominal conditions. The voltage at the AGC pin can be externally controlled by connecting a resistor between the AGC pin and either VPA1 or AGND1. When a resistor is connected from AGC to VPA1 the voltage on the AGC pin can be increased (Figure 1a). When a resistor is connected from AGC to AGND1 the voltage on the AGC pin can be decreased (Figure 1b). The new DIN± input target level is nominally (VAGC -0.75)•0.64 Vpp. The output of the AGC amplifier has a maximum swing of 3.0 Vpp that can be controlled using the AGC pin. The 3.0 Vpp swing supports the use of external filters that have up to 6 dB of loss. A multi-pole Bessel or an equiripple linear phase filter is typically used for its linear phase or constant group delay characteristics.



FIGURES 1A & 1B: AGC Voltage

The gain of the AGC amplifier is directly controlled by the voltage at the BYP pin (VBYP) or the VEGC pin as shown in Figure 2. The AGC amplifier has open collector outputs that can sink up to 4.0 mA of current. For correct operation over the gain range each output should be pulled up to VPA1 through a 340 Ω resistor as shown in Figure 3.

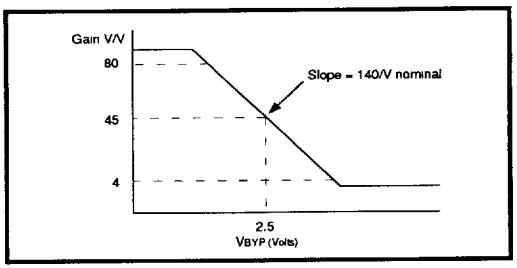


FIGURE 2: AGC Gain

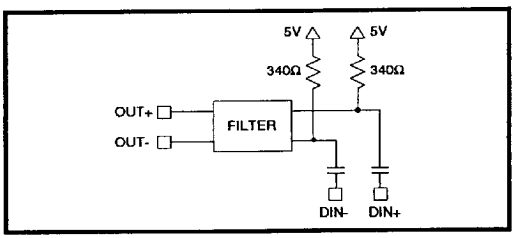


FIGURE 3: AGC Filter

PULSE QUALIFICATION

The SSI 34P553/5531 uses both amplitude and time qualification to digitize the incoming data pulses. In the amplitude channel the signal is sent to a hysteresis comparator. A hysteresis trip level is externally set such that only pulses that exceed the required signal level will trip the comparator. This prevents false qualification of baseband noise. The hysteresis trip level can be either a fixed level or a fraction of the DIN± voltage level.

Hysteresis Level. A fixed hysteresis level can be set by applying a DC voltage to the HYS pin. This is a simple method for hysteresis control but it does not compensate well for internal variances from device to device. A more effective approach is to feed forward a percentage of the voltage level at the DIN± pins. This approach is accomplished by using a filter/divider network between the LEVEL and HYS pins. The LEVEL pin output voltage is a rectified and amplified version of the voltage level applied to the DIN± pins. The gain in this circuit is set so that a 1 Vpp signal applied to DIN± will result in a 1 Vpk (typical) output signal at the LEVEL pin. An external capacitor to AGND1 should be used on the LEVEL pin to maintain a DC level. An external voltage divider can be connected between the LEVEL pin and AGND1 to provide the hysteresis programming voltage to the HYS pin. The HYS pin voltage determines the percentage of the DIN± input signal that will trip the hysteresis comparator of the SSI 34P553/5531. The transfer function of the HYS pin for setting the threshold percentage is:

$$\text{Hysteresis Threshold} = 0.41 \times \text{VHYS}$$

where VHYS is the voltage applied to the HYS pin. For example, with a 1.0 Vpp signal at DIN± the LEVEL pin output will be 1.0 Vpk. Using a 50% resistor divider between LEVEL and AGND1 would result in a HYS pin voltage of 0.5V and that would produce a hysteresis threshold of 0.20V in both the positive and negative direction. This translates to a hysteresis threshold percentage of 40% of DIN±.

Because the SSI 34P553/5531 circuits are internally biased to the same levels, the technique of feeding forward the LEVEL pin voltage helps to offset process related internal tolerance variations. In addition, the feed forward technique speeds up transient recovery by allowing qualification of input pulses while the AGC is still settling, such as during write to read recovery or head change recovery. Care should be taken in selecting the hysteresis level time constant so that pattern induced low amplitude signals are not missed. The SSI 34P553/5531 has a built in minimum of ±50 mV threshold for level qualification even when the HYS pin is grounded. This prevents false triggering due to baseband noise during a DC erase gap.

The outputs of the hysteresis comparator are the "D" inputs of the D-type flip-flop. One side of the hysteresis comparator outputs is provided as the DOUT pin test point. The DOUT pin can be monitored by connecting a 3 to 6 kΩ resistor to AGND2. When the DOUT pin is not used, it can be pulled up to VPA1 to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3 to 6 KΩ pull-down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from DIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
20 pF < C < 500 pF
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the DIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{RDO}$ output pulse width.

WRITE MODE

In Write Mode the SSI 34P553/5531 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, ($\overline{RDO}$ pin held high), the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P553/5531 and a head preamplifier such as the SSI 34R1203R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

DATA SYNCHRONIZER SECTION

The SSI 34P553/5531 is designed to perform data synchronization in rotating memory systems which utilize a 1, 7 RLL and MFM encoding format. In the Read Mode the SSI 34P553/5531 performs Data Synchronization. The interface electronics and architecture of the SSI 34P553/5531 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 34P553/5531 can operate with data rates ranging from .6 to 1.6 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{5.97}{DR} - 1.78\,(k\Omega)\,MFM$$

$$RR = \frac{7.96}{DR} - 1.78\,(k\Omega)\,1,7$$

Where: DR = Data Rate in Mbit/s

An external TTL compatible reference may be applied to REFCLK

The SSI 34P553/5531 employs a Dual Mode Phase Detector: Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchrouous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develp the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 5, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. VCO is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at the code rate, VCO is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of VCO.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port ($\overline{WSL}$, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In application not utilizing this feature, $\overline{WSL}$ should be left open or connected to VPA2, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±5% to ±20% of TVCO are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.25\,TVCO\left(1 - \frac{3260+R}{5950+R}\right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to ±3% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to REFCLK. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner, the acquisition time is substantially reduced.

POWER DOWN MODE

A Power Down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN}$ low causes the device to go into complete shutdown.

MODE CONTROL

The SSI 34P553/5531 Circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, RG, and WG pins as shown in Table 1.

TABLE 1: Mode Control

WG	RG	$\overline{HOLD}$	$\overline{PDWN1}$	
0	0	1	1	Read Mode VCO Locked to XTAL
0	1	1	1	Read Mode VCO Locked to Read Data
0	X	0	1	Read Mode AGC gain held constant*
1	0	X	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	X	0	Power shutdown mode

* AGC gain will drift at a rate determined by BYP capacitor and Hold mode leakage current.

TABLE 2: Decode Window Symmetry Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

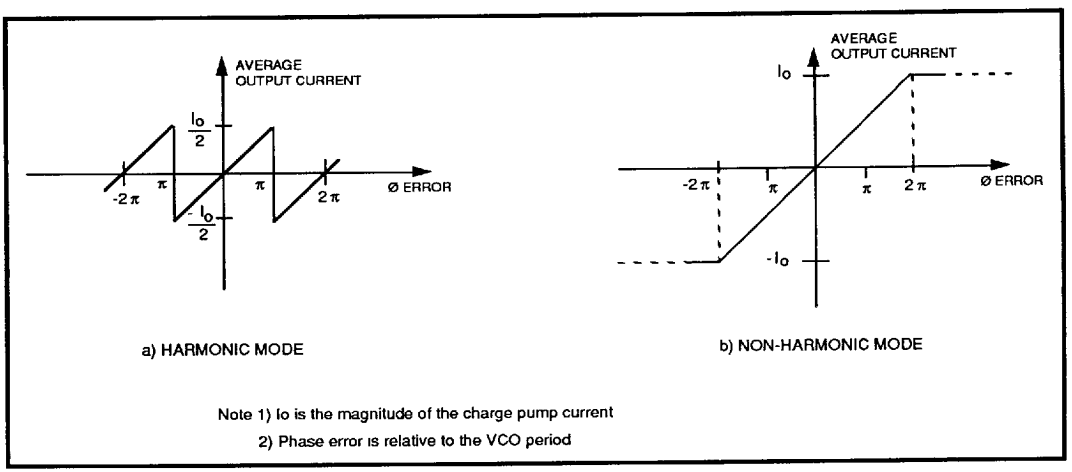


FIGURE 4: Phase Detector Transfer Function

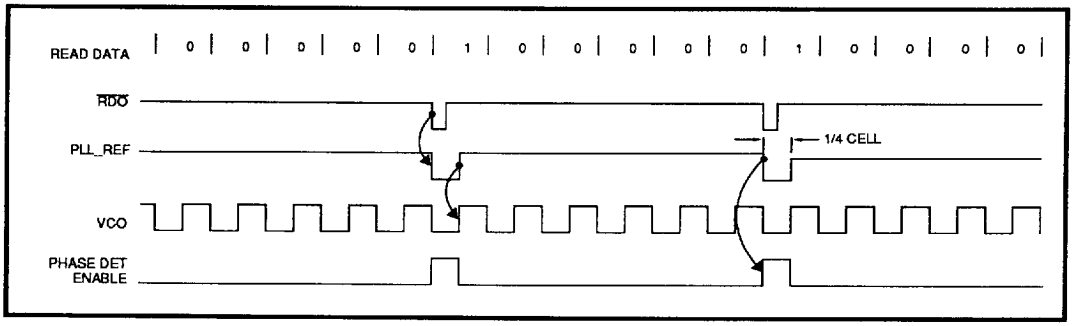


FIGURE 5: Data Synchronization Waveform Diagram

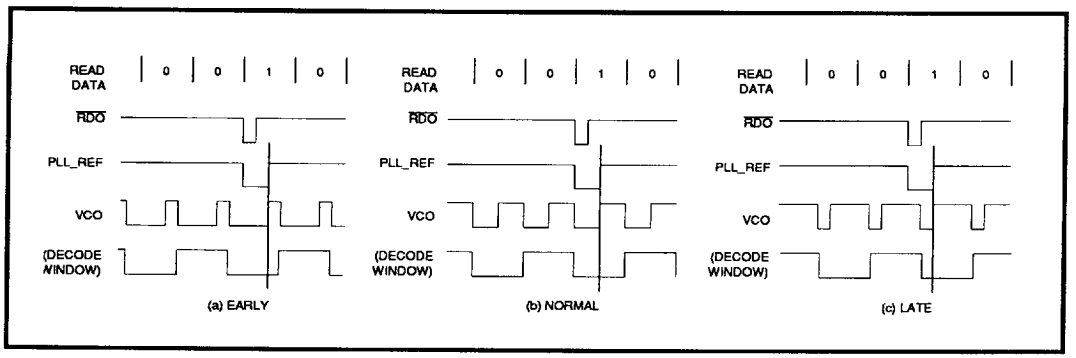


FIGURE 6: Decode Window

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1	I	Analog (+5V) power supply for pulse detector.
AGND1	I	Analog ground pin for pulse detector block.
VPA2	I	Analog (+5V) supply pin for data synchronizer block.
AGND2	I	Analog ground pin for data synchronizer block.
VPD	I	Digital (+5V) power supply pin.
DGND	I	Digital ground pin.
IN+, IN–	I	Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins.
DIN+, DIN–	I	Analog input to the hysteresis comparator, and differentiator.
CIN+, CIN–	I	Analog input to the clock comparator, differentiator. (34P5531 only)
DIF+, DIF–	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input. A 5 kΩ pull down resistor is required. When not in use, leave open or pull up to VPA1 to save power.
DOUT	O	Test point for monitoring the flip-flop D-input. A 5 kΩ pull down resistor is required. When not in use, leave open or pull up to VPA1 to save power.
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1.
AGC	I	Reference input voltage for the read data AGC loop.
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
TRKAA	O	Full wave rectifier output. This output has the same DC level as the LEVEL pin, i.e., ≤ 0.3V with no AC signal and ≈ $1V_{OP}$ with a $1V_{PP}$ AC signal at DIN+/ DIN-.
$\overline{\text{HOLD}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
EGC	I	External Gain Control. This is a TTL input pin that allows the AGC gain to be controlled by either BYP or the VEGC pin voltage. When EGC is high, the AGC gain is controlled by VEGC and the internal charge pump to BYP is disabled.
VEGC	I	The voltage at this pin is used to control the AGC gain when the EGC pin is held high.
$\overline{\text{RDO}}$	O	Read Data Output. This is the TTL output from the pulse detector. This signal may be fed directly into the $\overline{\text{RDT}}$ input.
IREF	I	Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2.
FLTR	I/O	Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SRD	O	Synchronized Read Data: read data that has been re-synchronized to VCO clock.
WSD	I	Window Symmetry Direction: controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	Window symmetry control bit: a low level introduces a window shift of 5% TORC (read reference clock period) in the direction established by WSD pin. $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	Window Symmetry Control bit: a low level introduces a window shift of 15% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
$\overline{WSL}$	I	Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{WS0}$, $\overline{WS1}$ into the internal DAC. An active low level latches the input bits.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.
RG	I	Read gate: selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pullup.
WG	I	Write Gate: enables the Write mode. Pin WG has an internal resistor pullup.
VCO CLK	O	VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{RDT}$	I	Read Data input. This TTL input comes from the $\overline{RDO}$ output of the pulse detector. This signal is active low.
$\overline{PDWN}$	I	Power Down input. When this input is low, the chip enters Low Power mode. This pin has an internal pullup resistor, and may be left open or tied high if not used.
REF CLK	I	Reference Clock. This is a TTL input at the code rate that is used as the reference for the VCO in Idle mode.
VCO	O	VCO output. This is the VCO signal converted to a TTL level.
PLL_REF	O	PLL Reference Test Point. In Write and Idle modes, this is the reference oscillator signal. In Read mode, it is the delayed read data (DRD) signal. This is an ECL level output. PLL_REF can be compared to VCOCLK to see the window centering accuracy.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V ≤ VPA 2 ≤ 5.5V, 25°C ≤ Tj ≤ 135°C, 1.2 MHz ≤ 1/TVCO ≤ 2.4 MHz.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
5V Supply Voltage, VPA1, VPA2, VPD	6.0 V
Pin Voltage (Analog pins)	-0.3 to VPA1, 2 + 0.3 V
Pin Voltage (All others)	-0.3 to VPD + 0.3 V or +12 mA
Storage Temperature	-65 to 150 °C
Lead Temperature (Soldering 10 sec.)	260 °C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA1, 2 & VPD)		4.5	5.0	5.5	V
Tj Junction Temperature		25		135	°C

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IVPA1, 2 Supply Current IVPD	Outputs unloaded $\overline{PDWN}$= high or open		110	143	mA
	$\overline{PDWN}$ = low Outputs unloaded		44	57	mA
Pd Power dissipation	Ta = 25°C, outputs unloaded $\overline{PDWN}$= high or open		550	790	mW
	$\overline{PDWN}$ = low Outputs unloaded		220	315	mW

ELECTRICAL SPECIFICATIONS (continued)

LOGIC SIGNALS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VIL Input Low Voltage		-0.3		0.8	V
VIH Input High Voltage		2.0		VCC+0.3	V
IIL Input Low Current	VIL = 0.4V	-0.4			mA
IIL WG Input Low Current	VIL = 0.4V	-0.8			mA
IIH Input High Current	VIH = 2.4V			100	µA
VOL Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA	2.4			V
VOHT Test Point Output High Level PLL_ REF, VCOCLK	262Ω to VPD 402Ω to GND VPD = 5.0V VOHT - VPD		-0.85		V
VOLT Test Point Output Low Level PLL_REF, VCOCLK	262Ω to VPD 402Ω to GND VPD = 5.0V, VOHT - VPD		-1.75		V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

MODE CONTROL

Enable to/from $\overline{\text{PDWN}}$ Transition Time	Settling time of external capacitors not included, $\overline{\text{PDWN}}$ pin high to/from low			20	µs
Read to Write Transition Time	WG pin low to high			1.0	µs
Write to Read Transition Time	WG pin high to low AGC setting not included	0.4	0.9	1.6	µs
$\overline{\text{HOLD}}$ On to/from $\overline{\text{HOLD}}$ Off Transition Time	$\overline{\text{HOLD}}$ pin high to/from low			1.0	µs
RG Time Delay				100	ns

READ MODE (WG is low)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 340Ω x 2 to VPA1, and each side is loaded with < 10 pF to AGND1, and AC coupled to DIN±. A 0.1 µF capacitor is connected between BYP and AGND1. AGC pin is open.

Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp	4		80	V/V
AGC Input Range	AGC output = 1Vpp differential	25		250	mVpp
Output Offset Voltage Variation	Over entire gain range	-500		+500	mV
Maximum Output Voltage Swing	Set by BYP or VEGC pin	3.0			Vpp

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz	4	5.4	7.5	kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		5	10	pF
Single Ended Input Impedance	WG = low, IN+ or IN-	2	2.7	4	kΩ
	WG = high, IN+ or IN-		160	250	Ω
Input Noise Voltage	Gain set to maximum, Rs = 0 BW = 15 MHz		5	15	nV/√Hz
Bandwidth	-3 dB bandwidth at maximum gain	12			MHz
OUT+ & OUT- Pin Current	No DC path to AGND1	2.5	4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mVpp @ 5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC Input (DIN+) - (DIN-) = (V_{AGC} - K1) • K2	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp				
	K1	0.5	0.8	0.95	V
	K2	0.54	0.64	0.74	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			5.0	%
AGC Voltage	AGC open	2.0	2.3	2.6	V
AGC Pin Input Impedance		1.8	2.5	3.8	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V, AGC pin open	2.8	4.5	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after WG goes low, stops at 1.8 µs after WG goes low		0.12		mA
BYP Leakage Current	$\overline{HOLD}$ = low	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.563 VDC, AGC pin open	-0.11	-0.18	-0.25	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, AGC pin open	-0.9	-1.4	-1.9	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%

ELECTRICAL SPECIFICATIONS (continued)

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 90% final value		100	180	µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp at 0.6 MHz (OUT+) - (OUT-) to 90% final value	190	300	550	µs
Gain Attack Time	WG = high to low (IN+) - (IN-) = 250 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 110% final value		8	15	µs

WRITE MODE (WG is high)

Single Ended Input Impedance (Each Side)	IN+ or IN-		160	250	Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz	3	5.5	8	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz		4	8	pF
Single Ended Input Impedance (Each Side)	DIN+ or DIN-	1.5	2.75	4	kΩ
Level Gain	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND	0.80	1.00	1.25	V/Vpp
Slope of Level Gain	Calculated from 0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp	0.75	0.87	1.00	V/Vpp
Intercept of Level Gain	DIN± = 0 Vpp	-0.6	-0.4	-0.2	V
Level Gain		Slope + (Intercept/DIN)			
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA	100	200	300	Ω
Level pin Maximum Output Current		1.5			mA

HYSTERESIS COMPARATOR (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Hysteresis Gain	0.3V < HYS < 1.0V	0.30	0.41	0.50	V/V
Slope of Hysteresis Gain	Calculated from 0.3V < HYS < 1.0V	0.34	0.42	0.46	V/Vpp
Intercept of Hysteresis Gain	HYS = 0V	-0.05	0.00	0.05	V
Hysteresis Gain		Slope + (Intercept/HYS V)			
HYS Pin Current	0.3 V < HYS < 1.0V	0.0		-5	µA
DOUT Pin Output Low Voltage	5 kΩ from DOUT to AGND2	VPA2 -2.5	VPA2 -2	VPA2 -1.35	V
DOUT Pin Output High Voltage	5 kΩ from DOUT to AGND2	VPA2 -2.0	VPA2 -1.6	VPA2 -1.1	V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC-coupled, 1.0 Vpp, 0.6 MHz sine wave. 100 Ω in series with 265 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	2.0	2.5	3.5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	-0.7		+0.7	mA
COUT Pin Output Low Voltage	5 kΩ from COUT to GND	VPA2 -2.5	VPA2 -2	VPA2 -1.35	V
COUT Pin Output High Voltage	5 kΩ from COUT to GND	VPA2 -2	VPA2 -1.6	VPA2 -1.1	V
COUT Pin Output Pulse Width			36		ns

ELECTRICAL SPECIFICATIONS (continued)

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (DIN+) - (DIN-) are an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 100Ω in series with 265 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT have a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low. $\overline{RDO}$ is loaded with a 4 kΩ resistor to VPD and a 10 pF capacitor to DGND.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak of DP/DN to $\overline{RDO}$ output pulse		60	110	ns
Td4	Propagation Delay	From negative peak of DP/DN to $\overline{RDO}$ output pulse		60	110	ns
|Td3-Td4|	Pulse Pairing				6	ns
Td5	Output Pulse Width		25	36	55	ns

SYNCHRONIZER SECTION

READ MODE

TRVCO, VCO Output Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFVCO, VCO Output Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TSRD, SRD Output Pulse Width		(TVCO) -12		(TVCO) +12	ns
TRSRD, Read Data Rise Time	0.8V to 2.0V, CL ≤ 15 pF			10	ns
TFSRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TPSRD, SRD Output Setup/HoldTime	Falling edge of VCO to either edge of SRD	-15		15	ns
TRD, $\overline{RDT}$ Input Pulse Width		20		(TVCO) -20	ns
TFRD, $\overline{RDT}$ Input Fall Time				15	ns
TWVCO, VCO Output		0.26TVCO		0.74TVCO	ns
Pulse Width (Includes Effects of Window Shift)		-10		+10	

WINDOW SYMMETRY CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TWSS $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
TWSH $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 83.8 (RR + 1.78), RR = 3k to 9k VPA2 = 5.0V	0.8TO		1.2TO	ns
	VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VPA2-0.6V VPA2 = 5.0V	±22		±45	%
KVCO	VCO Control Gain	$\omega o = 2\pi / TO$ 1.0V ≤ VCO IN ≤ VPA2-0.6V	0.16 ωo		0.25 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.538 / (RR+500) VPA2 = 5.0V	0.83 KD		1.17 KD	A/rad
*	KVCO x KD Product Accuracy		-28		+28	%
*	VCO Phase Restart Error			12		ns
	Decode Window Centering Accuracy		-.02 TVCO		.02 TVCO	ns
	Decode Window		0.9 TVCO			ns
TS1	Decode Window Time Shift	TWS1 = .05 TVCO $\overline{WSO}$ = 0; $\overline{WSI}$ = 1		TWS1		ns
TS2	Decode Window Time Shift	TWS2 = .15 TVCO $\overline{WSO}$ = 1; $\overline{WSI}$ = 0		TWS2		ns
TS3	Decode Window Time Shift	TWS3 = .2 TVCO $\overline{WSO}$ = 0; $\overline{WSI}$ = 0		TWS3		ns
TSA	Decode Window Time Shift	$TWSA = 0.29\,TVCO\left(1-\frac{3260+R}{5950+R}\right)$ $\overline{WSO}$ = 1; $\overline{WSI}$ = 1		TWSA		ns
*	Not directly testable; design characteristics					

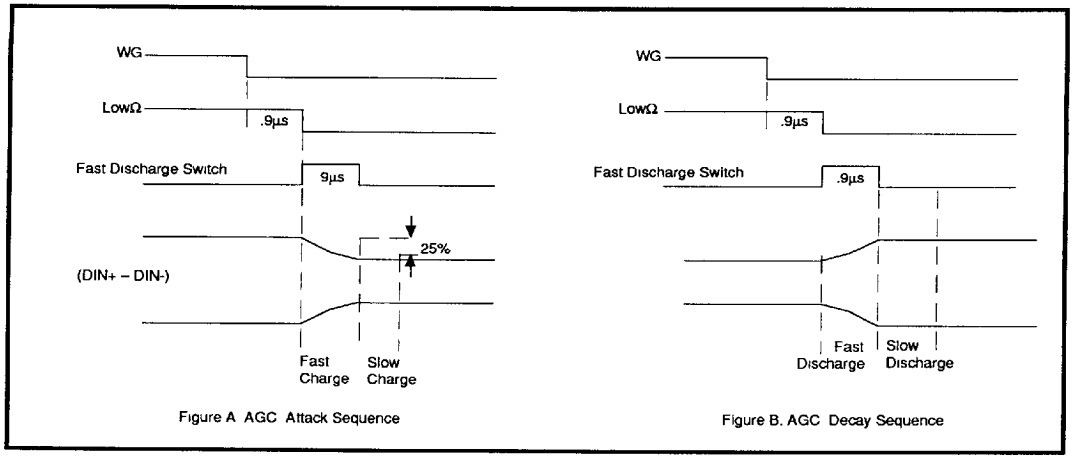


FIGURE 7: AGC Timing Diagram

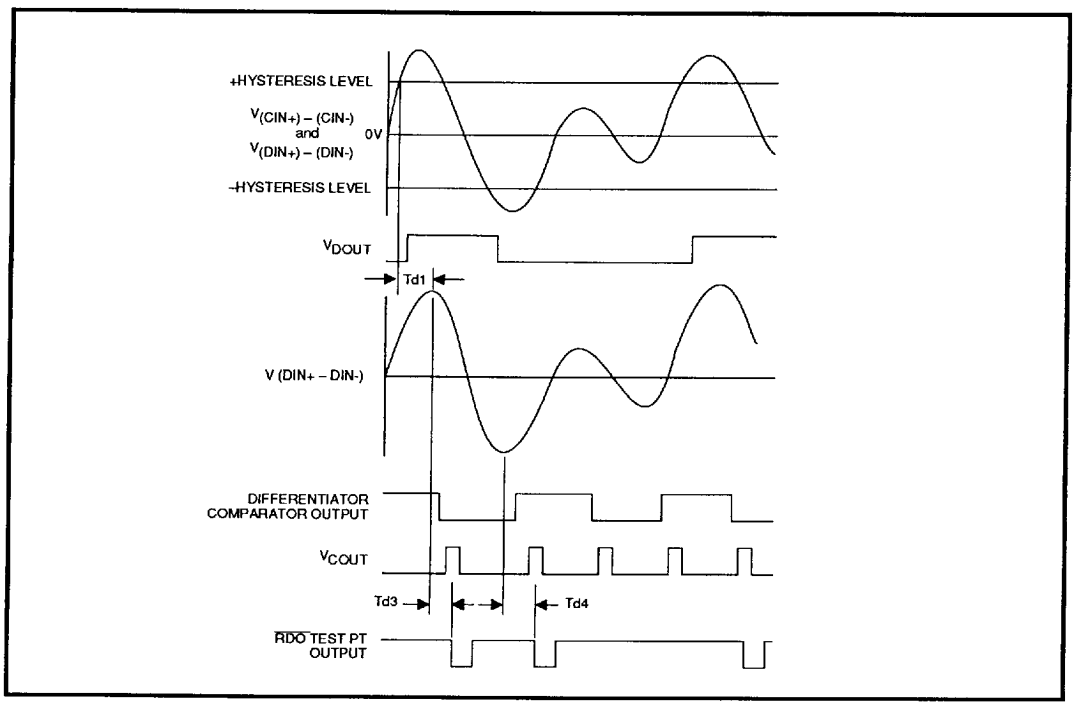


FIGURE 8: Read Mode Digital Section Timing Diagram

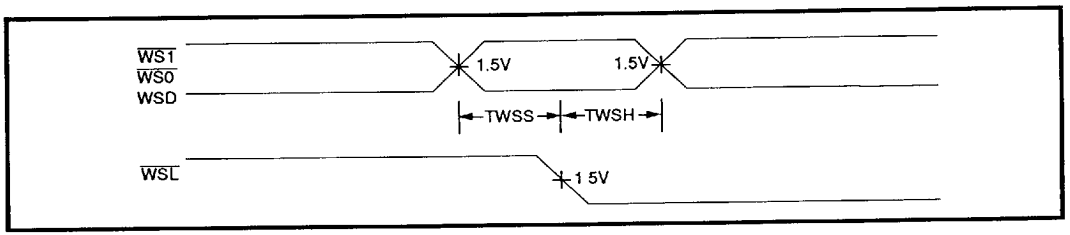


FIGURE 9: Window Symmetry Control Timing

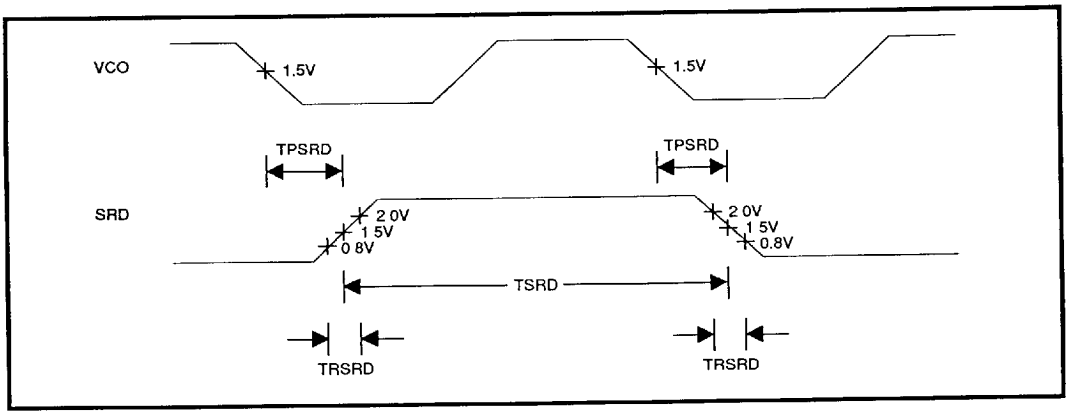


FIGURE 10: Read Mode Timing

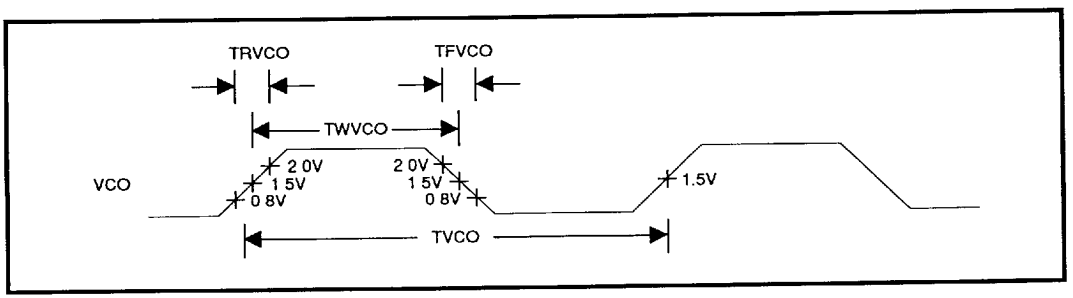


FIGURE 11: VCO Timing

APPLICATIONS INFORMATION

The SSI 34P553/5531 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure14A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of an encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 15.

The SSI 34P553/5531 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the SSI 34P553/5531 data synchronizer is shown in Figure 16B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO: $K_o = \frac{d\omega_o}{dV}$ (1a)

$$\frac{dT_o}{dV} \quad \frac{d}{dV}\left(\frac{1}{f_o}\right) = -\frac{1}{f_o{}^2}\frac{df_o}{dV} = -T_o{}^2\frac{df_o}{dV} = -\frac{T_o{}^2}{2\pi}\frac{dw_o}{dV} \quad (1b)$$

where:

K_o = VCO gain
ω_o = VCO center frequency (rad/s)
f_o = VCO center frequency (Hz)
T_o = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o}a\frac{dT_o}{dV} = -\alpha T_o\frac{dw_o}{dV} = -\alpha T_o K_o$$

where:

θ_o = Phase due to quarter cell delay circuit
T_o = VCO center frequency period
T_Q = Quarter cell delay time
$\alpha = T_Q/T_o = 0.5$ for the 32P548

The gain of the quarter cell delay block is constant in the SSI 34P553/5531, regardless of the values of other components.

For the SSI 34P553/5531, the nominal value of K_T is 0.17π.

PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In Write and Idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In Read, mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in Idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for Read and Idle modes are given in (3) and (4), respectively.

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+nK_TK_dF(s)+\frac{nK_oK_dF(s)}{S}} \quad (3)$$

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+\frac{nK_oK_dF(s)}{S}} \quad (4)$$

where:

K_T = Quarter cell delay one-shot gain
K_O = VCO gain
K_d = Phase detector gain
F(s) = Loop filter transfer function
n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_O T_O$ into (3),

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+(1-s\alpha T_O)\frac{nK_OK_dF(s)}{S}}$$

The additional $-s\alpha T_O$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 12, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, V_o/I_i (s), where V_o (s) is the output voltage, and I_i (s) is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1+1}{s(C_1+C_2)\left(sR_1\frac{C_1C_2}{C_1+C_2}+1\right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1+C_2)+1}{sC\left(sR_1C_2+1\right)} \quad (7)$$

For loop filter (a), C_2 is normally chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and $sR_1C_1 \ll 1$ at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1+1}{sC_1} \quad (8)$$

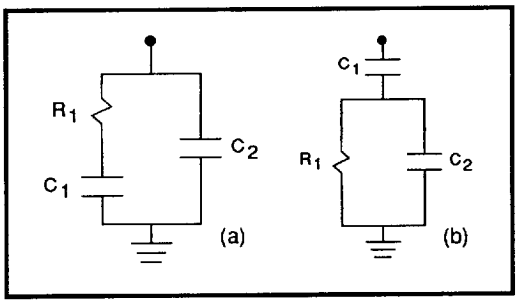


FIGURE 12: Loop Filter

For loop filter (b), C_2 is normallly chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and that $sR_1C_2 \ll 1$ at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1+1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

(10)

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_d}{C_1(1-\alpha T_OnK_OK_dR_1)}(sR_1C_1+1)}{s^2+s\frac{nK_OK_d}{1-\alpha T_OnK_OK_dR_1}\left(R_1-\frac{\alpha T_O}{C_1}\right)+\frac{nK_OK_d}{C_1(1-\alpha T_OnK_OK_dR_1)}}$$

This is in the form of a standard second order transfer fucntion. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: ζ = damping factor
ω_n = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_OK_d}{C_1(1-\alpha T_OnK_OK_dR_1)}} \quad (12)$$

$$\zeta = \frac{R_1-\frac{\alpha T_O}{C_1}}{2}\sqrt{\frac{nK_OK_dC_1}{1-\alpha T_OnK_OK_dR_1}} \quad (13)$$

Substituting (8) into (4) gives the transfer function for Idle mode:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1}(sR_1C_1+1)}{s^2+s(nK_oK_dR_1)+\frac{nK_oK_d}{C_1}} \quad (14)$$

Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2}\sqrt{nK_oK_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find ζ/ω_n, then solve for R_1C_1.

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_o \quad (17)$$

Substitute this value for R_1C_1 into the equation for ω_n and solve for C_1.

$$C_1 = \frac{nK_oK_d}{\omega_n^2} + \alpha T_o nK_oK_d\left(\frac{2\zeta}{\omega_n} + \alpha T_o\right) \quad (18)$$

Now that C_1 is known, R_1 can be found by dividing (17) through by C_1.

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_o\right)\frac{1}{C_1} \quad (19)$$

EXAMPLE 1

Assume that the data rate is 0.6 Mbit/s, $\zeta = 0.7$, a length of 20 2T patterns for the loop to lock is used, and $\omega_n t = 5.7$ for error < 1%.

n = 0.5 due to the 2T pattern.

$$T_0 = \frac{1}{f_0} = \frac{1}{1.2 \cdot 10^6} = 833\text{ns}$$

$\omega_0 = 2\pi f_0 = 2\pi (1.2 \cdot 10^6) = 7.54 \cdot 10^6$ rad/s

$\alpha_0 = 0.5$

For the SSI 34P553: $RR = \frac{5.97}{DR} - 1.79(k\Omega) = 8.17k\Omega$

where DR = Data Rate in Mbit/s

$$K_0 = 0.17\omega_0 = 1.28 \cdot 10^6 \frac{\text{rad/sec}}{\text{Volt}}$$

$$K_d = \frac{0.62}{RR+500} = 71.51 \cdot 10^{-6}\ \text{A/rad}$$

$K_T = 0.17\pi = 0.534$

Assuming a length of 20 2T patterns, then:
t = (20) (2) (833) ns = 33.3 µs

$$\omega n = \frac{5.7}{33.3\mu s} = 1.71 \cdot 10^5\ \text{rad/s}$$

C_1 = 1565 pF + 165.6 pF = 1.73 nF

R_1 = 5.02 kΩ

The resulting loop filter is shown in Figure 13.

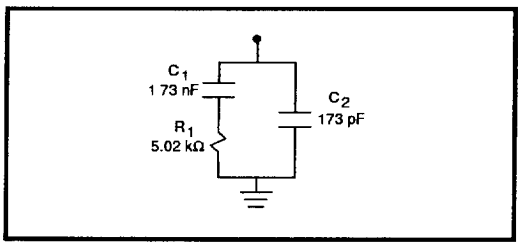


FIGURE 13

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in Idle mode, the loop transfer function is given by (14), and ω_n and ζ are given by (15) and (16). R_1 and C_1 from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in Idle mode.

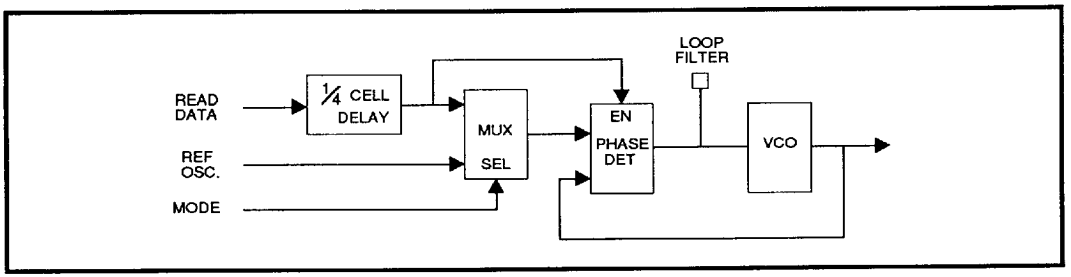


FIGURE 14A: Standard Configuration of a Data Synchronizer Phase-Locked Loop

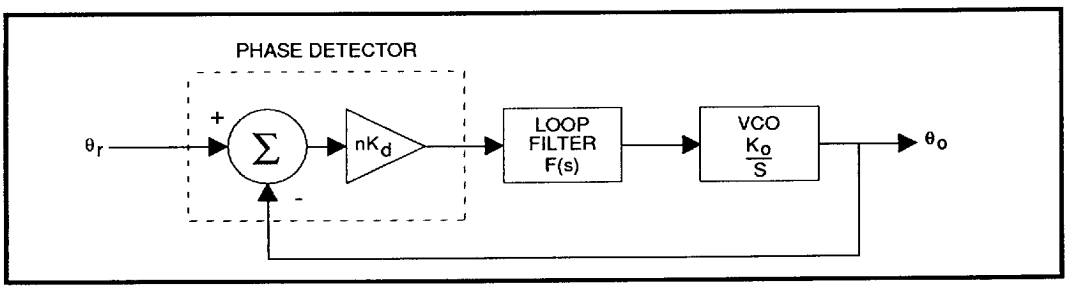


FIGURE 14B: Phase-Lock Loop System Representation

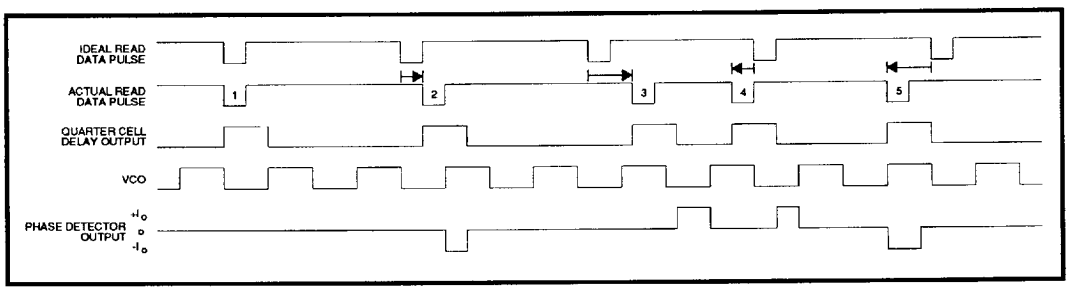


FIGURE 15A: Phase Detector Timing with Ideal Quarter Cell Delay. For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

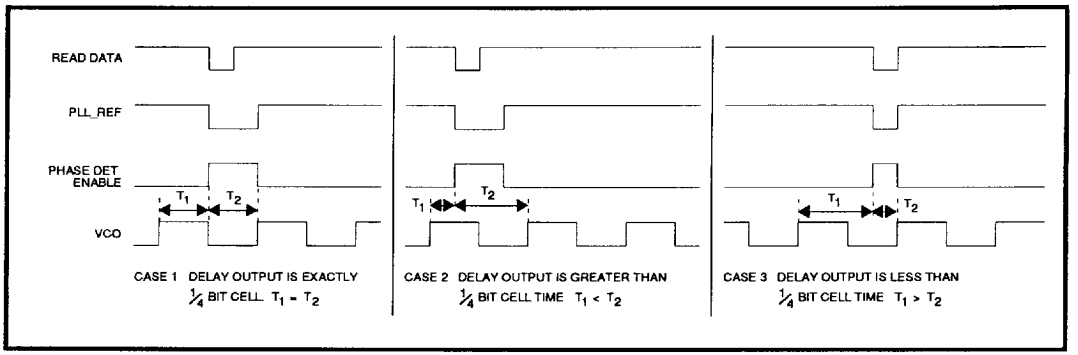


FIGURE 15B: Timing of Phase Detector Enable Logic. The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity, If the quarter cell delay output is not exactly 1/4 bit cell wide, then T1 ≠ T2, as shown in cases 2 and 3.

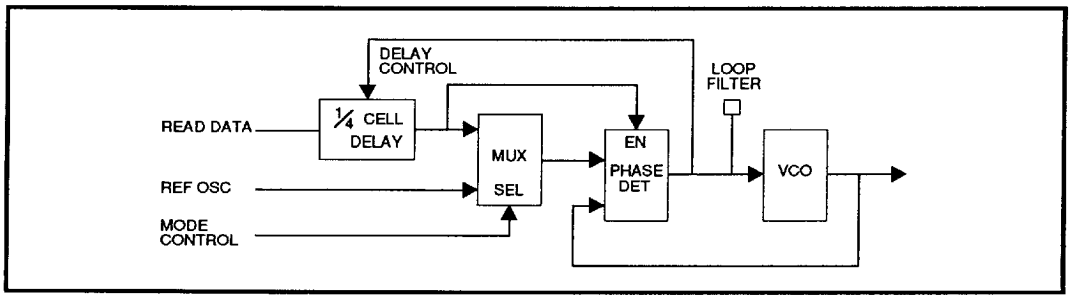


FIGURE 16A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control

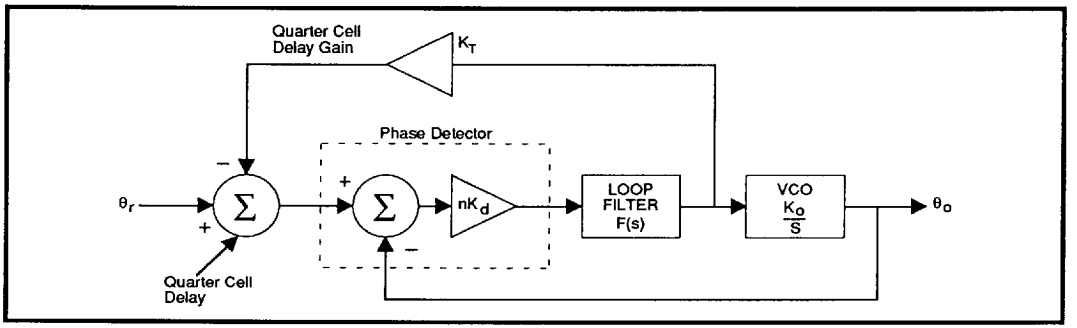


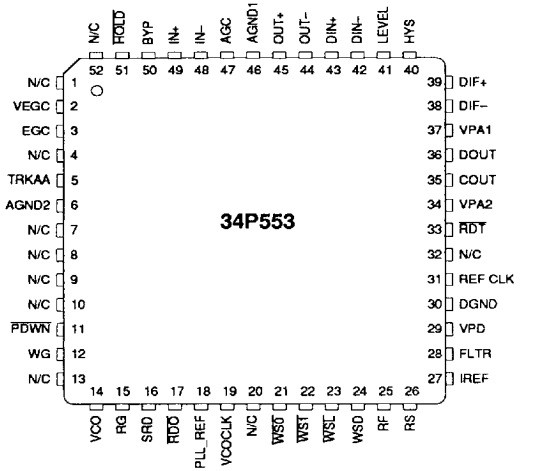
FIGURE 16B: Modified Data Synchronizer System Representation

SSI 34P553/5531
Pulse Detector & Data Synchronizer

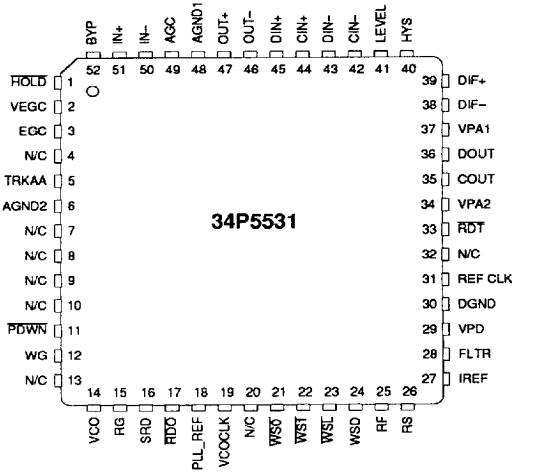
PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

52-Lead QFP	75° C/W



52-Lead QFP



52-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P553 Pulse Detector & Data Synchronizer		
52-Lead QFP	32P553-CG	32P553-CG
SSI 32P5531 Pulse Detector & Data Synchronizer		
52-Lead QFP	32P5531-CG	32P5531-CG

Silicon Systems, Inc , 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

