# PC Clock Generator

## Features

- Generates up to 16 preset frequencies, 4 peripheral clocks, and buffers input reference frequency
- Power down, slow down, stop clock, or output enable feature supporting "Green PC" applications
- Smooth glitch-free frequency transitions
- Requires only three external components: one 14.318 MHz crystal and two 0.1 µF decoupling capacitors
- On-chip loop filters for clock generators
- Supports x86-based designs
- Drop-in replacement for AV9155
- CMOS technology available in 20-pin PDIP and SOIC
- 5V or 3.3V supply

## Description

CH9055 is a dual PLL clock generator designed for personal computer motherboard applications. CH9055 buffers the reference frequency into 2 outputs, generates CPU and 2XCPU clocks, and provides up to 4 separate fixed peripheral clocks. The CPU and 2XCPU frequencies can be selected with the clock select inputs, SCLK[23:20]. These frequencies support the new generation of CPU upgradable motherboards. CPU clocks for x86 and Pentium™ are selected by externally setting select pins to VDD or GND.

CH9055 is available with Output Enable (OE), Power Down (PD*), Slow Down (SD*) or Stop Clock (CLKEN) options, which are ideal for low power "Green PC" applications.

Power down is enabled by setting the PD* pin to ground. While PD* is active, the internal PLLs and crystal are disabled to minimize current consumption (less than 10 µA).

Setting the SD* pin to ground enables slow down, which gradually slows the CPU and 2XCPU outputs to 16 MHz, 8 MHz, or 4 MHz.

The clock enable (CLKEN) option supports x86-based systems with a stop clock feature. When CLKEN is pulled low, CPU and 2XCPU outputs are disabled and held at a low state.



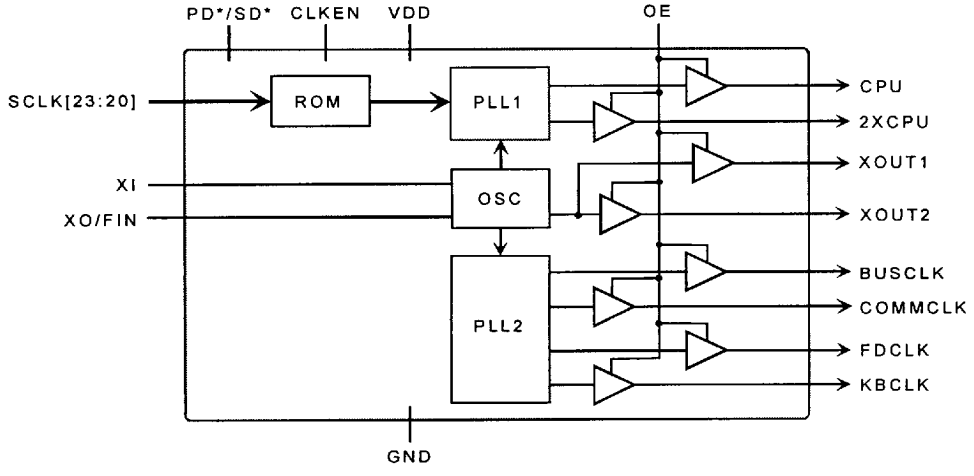


**Figure 1: Block Diagram**

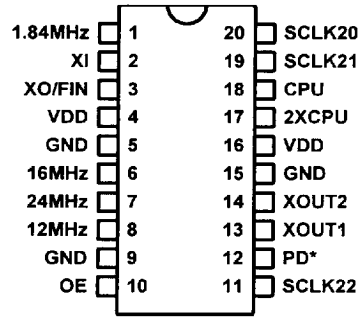


**Figure 2: CH9055A**

**Table 1 • Pin Description CH9055A**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out | 1.84 MHz | 1.84 MHz communications clock output |
| 2 | In | XI | Crystal input |
| 3 | Out / In | XO / FIN | Crystal output or external FREF input |
| 4, 16 | Power | VDD | 5V or 3.3V supply |
| 5, 9, 15 | Power | GND | Ground |
| 6 | Out | 16 MHz | 16 MHz AT bus clock output |
| 7 | Out | 24 MHz | 24 MHz floppy disk clock output |
| 8 | Out | 12 MHz | 12 MHz keyboard clock output |
| 10 | In | OE | Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated. |
| 11, 19, 20 | In | SCLK22, SCLK21, SCLK20 | CPU and 2XCPU clock select inputs (internal pull-up) |
| 12 | In | PD* | Power down input (active low, internal pull-up) |
| 13, 14 | Out | XOUT1, XOUT2 | Buffered reference (14.318 MHz) clock outputs |
| 17 | Out | 2XCPU | 2XCPU clock output |
| 18 | Out | CPU | CPU clock output |

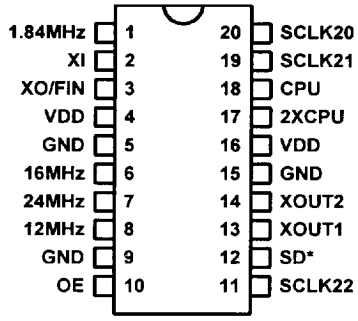


**Figure 3: CH9055B**

**Table 2 • Pin Description CH9055B**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out | 1.84 MHz | 1.84 MHz communications clock output |
| 2 | In | XI | Crystal input |
| 3 | Out / In | XO / FIN | Crystal output or external FREF input |
| 4, 16 | Power | VDD | 5V or 3.3V supply |
| 5, 9, 15 | Power | GND | Ground |
| 6 | Out | 16 MHz | 16 MHz AT bus clock output |
| 7 | Out | 24 MHz | 24 MHz floppy disk clock output |
| 8 | Out | 12 MHz | 12 MHz keyboard clock output |
| 10 | In | OE | Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated. |
| 11, 19, 20 | In | SCLK22, SCLK21, SCLK20 | CPU and 2XCPU clock select inputs (internal pull-up) |
| 12 | In | SD* | Slow down input (active low, internal pull-up) |
| 13, 14 | Out | XOUT1, XOUT2 | Buffered reference (14.318 MHz) clock outputs |
| 17 | Out | 2XCPU | 2XCPU clock output |
| 18 | Out | CPU | CPU clock output |

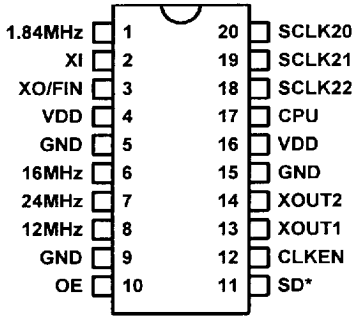


**Figure 4: CH9055C**

**Table 3 • Pin Description CH9055C**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out | 1.84 MHz | 1.84 MHz communications clock output |
| 2 | In | XI | Crystal input |
| 3 | Out / In | XO / FIN | Crystal output or external FREF input |
| 4, 16 | Power | VDD | 5V or 3.3V supply |
| 5, 9, 15 | Power | GND | Ground |
| 6 | Out | 16 MHz | 16 MHz AT bus clock output |
| 7 | Out | 24 MHz | 24 MHz floppy disk clock output |
| 8 | Out | 12 MHz | 12 MHz keyboard clock output |
| 10 | In | OE | Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated. |
| 11 | In | SD* | Slow down input (active low, internal pull-up) |
| 12 | In | CLKEN | CPU clock enable input (active low, internal pull-up). When CLKEN is low, CPU output is disabled and held in a low state. |
| 13, 14 | Out | XOUT1, XOUT2 | Buffered reference (14.318 MHz) clock outputs |
| 17 | Out | CPU | CPU clock output |
| 18, 19, 20 | In | SCLK22, SCLK21, SCLK20 | CPU clock select inputs (internal pull-up) |

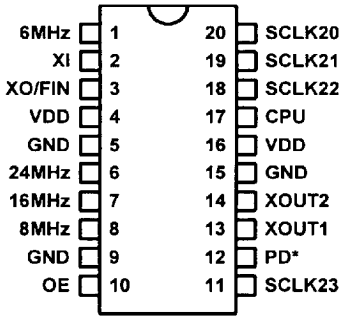


**Figure 5: CH9055D**

**Table 4 • Pin Description CH9055D**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out | 6 MHz | 6MHz communications clock output |
| 2 | In | XI | Crystal input |
| 3 | Out / In | XO / FIN | Crystal output or external FREF input |
| 4, 16 | Power | VDD | 5V or 3.3V supply |
| 5, 9, 15 | Power | GND | Ground |
| 6 | Out | 24 MHz | 24 MHz floppy disk clock output |
| 7 | Out | 16 MHz | 16 MHz AT bus clock output |
| 8 | Out | 8 MHz | 8 MHz keyboard clock output |
| 10 | In | OE | Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated. |
| 11, 18, 19, 20 | In | SCLK23, SCLK22, SCLK21, SCLK20 | CPU clock select inputs (internal pull-up) |
| 12 | In | PD* | Power down input (active low, internal pull-up) |
| 13, 14 | Out | XOUT1, XOUT2 | Buffered reference (14.318 MHz) clock outputs |
| 17 | Out | CPU | CPU clock output |

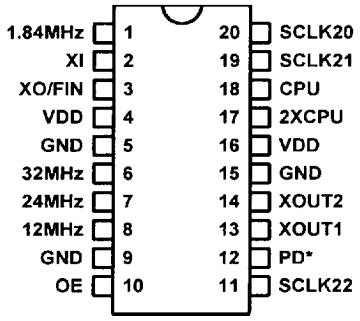


**Figure 6: CH9055E**

**Table 5 • Pin Description CH9055E**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out | 1.84 MHz | 1.84 MHz communications clock output |
| 2 | In | XI | Crystal input |
| 3 | Out / In | XO / FIN | Crystal output or external FREF input |
| 4, 16 | Power | VDD | 5V or 3.3V supply |
| 5, 9, 15 | Power | GND | Ground |
| 6 | Out | 32 MHz | 32 MHz AT bus clock output |
| 7 | Out | 24 MHz | 24 MHz floppy disk clock output |
| 8 | Out | 12 MHz | 12 MHz keyboard clock output |
| 10 | In | OE | Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated. |
| 11, 19, 20 | In | SCLK22, SCLK21, SCLK20 | CPU and 2XCPU clock select inputs (internal pull-up) |
| 12 | In | PD* | Power down input (active low, internal pull-up) |
| 13, 14 | Out | XOUT1, XOUT2 | Buffered reference (14.318 MHz) clock outputs |
| 17 | Out | 2XCPU | 2XCPU clock output |
| 18 | Out | CPU | CPU clock output |

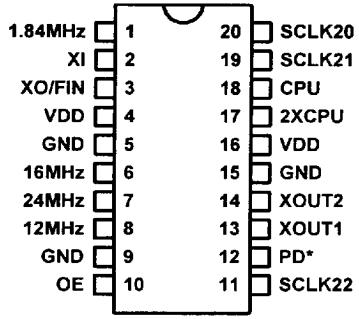


**Figure 7: CH9055F**

**Table 6 • Pin Description CH9055F**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out | 1.84 MHz | 1.84 MHz communications clock output |
| 2 | In | XI | Crystal input |
| 3 | Out / In | XO / FIN | Crystal output or external FREF input |
| 4, 16 | Power | VDD | 5V or 3.3V supply |
| 5, 9, 15 | Power | GND | Ground |
| 6 | Out | 16 MHz | 16 MHz AT bus clock output |
| 7 | Out | 24 MHz | 24 MHz floppy disk clock output |
| 8 | Out | 12 MHz | 12 MHz keyboard clock output |
| 10 | In | OE | Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated. |
| 11, 19, 20 | In | SCLK22, SCLK21, SCLK20 | CPU and 2XCPU clock select inputs (internal pull-up) |
| 12 | In | PD* | Power down input (active low, internal pull-up) |
| 13, 14 | Out | XOUT1, XOUT2 | Buffered reference (14.318 MHz) clock outputs |
| 17 | Out | 2XCPU | 2XCPU clock output |
| 18 | Out | CPU | CPU clock output |

**Table 7 • Frequencies for CH9055A through C (in MHz)**

| SCLK (Clock Select) | | | | Version A | | Version B | | Version C | |
|---|---|---|---|---|---|---|---|---|---|
| 23 | 22 | 21 | 20 | CPU | 2XCPU | CPU | 2XCPU | CPU | Slow Freq |
| 0 | 0 | 0 | 0 | 4.0 | 8.0 | 4.0 | 8.0 | 25.0 | 8.0 |
| 0 | 0 | 0 | 1 | 8.0 | 16.0 | 8.0 | 16.0 | 33.33 | 8.0 |
| 0 | 0 | 1 | 0 | 16.0 | 32.0 | 16.0 | 32.0 | 40.0 | 8.0 |
| 0 | 0 | 1 | 1 | 20.0 | 40.0 | 20.0 | 40.0 | 50.0 | 16.0 |
| 0 | 1 | 0 | 0 | 25.0 | 50.0 | 25.0 | 50.0 | 66.6 | 16.0 |
| 0 | 1 | 0 | 1 | 33.3 | 66.6 | 33.3 | 66.6 | 60.0 | 16.0 |
| 0 | 1 | 1 | 0 | 40.0 | 80.0 | 40.0 | 80.0 | 80.0 | 16.0 |
| 0 | 1 | 1 | 1 | 50.0 | 100.0 | 50.0 | 100.0 | 50.0 | 8.0 |
| 1 | 0 | 0 | 0 | — | — | — | — | — | — |
| 1 | 0 | 0 | 1 | — | — | — | — | — | — |
| 1 | 0 | 1 | 0 | — | — | — | — | — | — |
| 1 | 0 | 1 | 1 | — | — | — | — | — | — |
| 1 | 1 | 0 | 0 | — | — | — | — | — | — |
| 1 | 1 | 0 | 1 | — | — | — | — | — | — |
| 1 | 1 | 1 | 0 | — | — | — | — | — | — |
| 1 | 1 | 1 | 1 | — | — | — | — | — | — |
| COMMCLK (Communications clock output) | | | | 1.84 | | 1.84 | | 1.84 | |
| BUSCLK (AT bus clock output) | | | | 16.0 | | 16.0 | | 16.0 | |
| FDCLK (Floppy disk clock output) | | | | 24.0 | | 24.0 | | 24.0 | |
| KBCLK (Keyboard clock output) | | | | 12.0 | | 12.0 | | 12.0 | |
| XOUT1 and XOUT2 (Reference clock outputs) | | | | 14.318 | | 14.318 | | 14.318 | |
| Power down | | | | Yes | | No | | No | |
| Stop CPU clock | | | | No | | No | | Yes | |
| Glitch-free transitions | | | | Yes | | Yes | | Yes | |
| Slow down | | | | No | | Yes | | Yes | |
| Slow down frequency | | | | N/A | | 4.0 | 8.0 | See above | |

**Note:** Please consult Chrontel for custom frequency patterns

**Table 8 • Frequencies for CH9055D through F (in MHz)**

| SCLK (Clock Select) | | | | Version D | Version E | | Version F | |
|---|---|---|---|---|---|---|---|---|
| 23 | 22 | 21 | 20 | CPU | CPU | 2XCPU | CPU | 2XCPU |
| 0 | 0 | 0 | 0 | 16.0 | 4.0 | 8.0 | 37.5 | 75.0 |
| 0 | 0 | 0 | 1 | 40.0 | 8.0 | 16.0 | 16.0 | 32.0 |
| 0 | 0 | 1 | 0 | 50.0 | 16.0 | 32.0 | 30.0 | 60.0 |
| 0 | 0 | 1 | 1 | 80.0 | 20.0 | 40.0 | 20.0 | 40.0 |
| 0 | 1 | 0 | 0 | 66.6 | 25.0 | 50.0 | 25.0 | 50.0 |
| 0 | 1 | 0 | 1 | 100.0 | 33.3 | 66.6 | 33.3 | 66.6 |
| 0 | 1 | 1 | 0 | 8.0 | 40.0 | 80.0 | 40.0 | 80.0 |
| 0 | 1 | 1 | 1 | 4.0 | 50.0 | 100.0 | 26.0 | 52.0 |
| 1 | 0 | 0 | 0 | 8.0 | — | — | — | — |
| 1 | 0 | 0 | 1 | 20.0 | — | — | — | — |
| 1 | 0 | 1 | 0 | 25.0 | — | — | — | — |
| 1 | 0 | 1 | 1 | 40.0 | — | — | — | — |
| 1 | 1 | 0 | 0 | 33.3 | — | — | — | — |
| 1 | 1 | 0 | 1 | 50.0 | — | — | — | — |
| 1 | 1 | 1 | 0 | 4.0 | — | — | — | — |
| 1 | 1 | 1 | 1 | 2.0 | — | — | — | — |
| COMMCLK (Communications clock output) | | | | 6.0 | 1.84 | | 1.84 | |
| BUSCLK (AT bus clock output) | | | | 16.0 | 32.0 | | 16.0 | |
| FDCLK (Floppy disk clock output) | | | | 24.0 | 24.0 | | 24.0 | |
| KBCLK (Keyboard clock ouput) | | | | 8.0 | 12.0 | | 12.0 | |
| XOUT1 and XOUT2 (Reference clock outputs) | | | | 14.318 | 14.318 | | 14.318 | |
| Power down | | | | Yes | Yes | | Yes | |
| Stop CPU clock | | | | No | No | | No | |
| Glitch-free transitions | | | | Yes | Yes | | Yes | |
| Slow down | | | | No | No | | No | |
| Slow down frequency | | | | N/A | N/A | N/A | N/A | N/A |

**Note:** Please consult Chrontel for custom frequency patterns

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### Table 9 • Absolute Maximum Ratings

| Symbol | Description | Value | Unit |
|---|---|---|---|
| VDD | Power supply voltage with respect to GND | −0.5 to +7.0 | V |
| VIN | Input voltage on any pin with respect to GND | −0.5 to VDD+0.5 | V |
| TSTOR | Storage temperature | −55 to +150 | °C |

**Note:** Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Table 10 • DC Specifications (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 5V ±5%)

| Symbol | Description | Test Condition @TA=25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | Output high voltage | VDD = 4.75V, IOH = 4mA | 2.4 | | | V |
| VOL | Output low voltage | VDD = 4.75V, IOL = 8mA | | | 0.4 | V |
| VIH | Input high voltage | | 2.0 | | | V |
| VIL | Input low voltage | | | | 0.8 | V |
| IPU | Input pull-up current | | | 5 | 20 | µA |
| ILK | Input leakage current | | −10 | | 10 | µA |
| CI | Input capacitance | Except XO / FIN, XI | | | 10 | pF |
| CI | Input capacitance | Pins XO / FIN, XI | | 20 | | pF |
| IPD | Power down supply current | PD* = Low | | 10 | | µA |
| ISD | Slow down supply current | SD* = Low, VDD = 5.0V, No load | | 10 | | mA |
| IDD | Operating current | VDD = 5V CPU = 40 MHz, No load<br>CPU = 80 MHz, No load | | 20<br>25 | | mA |

### Table 11 • AC Specifications (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 5V ±5%)

| Symbol | Description | Test Condition @TA = 25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FXTAL | Crystal frequency | | | 14.318 | | MHz |
| FIN | Input frequency | | 1 | 14.318 | 32 | MHz |
| TIR | Input clock rise time | | | | 20 | ns |
| TIF | Input clock fall time | | | | 20 | ns |
| TR | Output clock rise time | 15 pF load, VOUT = 0.8V to 2.0V | | | 3 | ns |
| TF | Output clock fall time | 15 pF load, VOUT = 0.8V to 2.0V | | | 3 | ns |
| TDC | Duty cycle | 15 pF load | 45 | 48/52 | 55 | % |
| TJCC | Jitter, cycle to cycle | CPU = 50 MHz | | 50 | 150 | ps |
| TFT | Frequency transition time | 8 – 80 MHz | | 10 | | ms |
| TPU | Power up time | From OFF to 100 MHz | | 15 | | ms |

**Table 12 • DC Specifications (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 3.3V ± 0.3V)**

| Symbol | Description | Test Condition @TA=25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | Output high voltage | VDD = 3.0V, IOH = 1mA | VDD – 0.5 | | | V |
| VOL | Output low voltage | VDD = 3.0V, IOL = 2mA | | | 0.5 | V |
| VIH | Input high voltage | | 2.0 | | | V |
| VIL | Input low voltage | | | | 0.8 | V |
| IPU | Input pull-up current | | | 3 | 10 | µA |
| ILK | Input leakage current | | –10 | | 10 | µA |
| CI | Input capacitance | Except XO / FIN, XI | | | 10 | pF |
| CI | Input capacitance | Pins XO / FIN, XI | | 20 | | pF |
| IPD | Power down supply current | PD* = Low | | 3 | | µA |
| ISD | Slow down supply current | SD* = Low, VDD = 3.3V, No load | | 10 | | mA |
| IDD | Operating current | VDD = 3.3V CPU = 40 MHz, No load<br>CPU = 80 MHz, No load | | 15<br>18 | | mA |

**Table 13 • AC Specifications (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 3.3V ± 0.3V)**

| Symbol | Description | Test Condition @TA = 25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FXTAL | Crystal frequency | | | 14.318 | | MHz |
| FIN | Input frequency | | 1 | 14.318 | 20 | MHz |
| TIR | Input clock rise time | | | | 20 | ns |
| TIF | Input clock fall time | | | | 20 | ns |
| TR | Output clock rise time | 15 pF load, VOUT = 0.8V to 2.0V | | | 3 | ns |
| TF | Output clock fall time | 15 pF load, VOUT = 0.8V to 2.0V | | | 3 | ns |
| TDC | Duty cycle | 15 pF load | 45 | 48/52 | 55 | % |
| TJCC | Jitter, cycle to cycle | CPU = 50 MHz | | 50 | 150 | ps |
| TFT | Frequency transition time | 8 – 80 MHz | | 10 | | ms |
| TPU | Power up time | From OFF to 100 MHz | | 15 | | ms |

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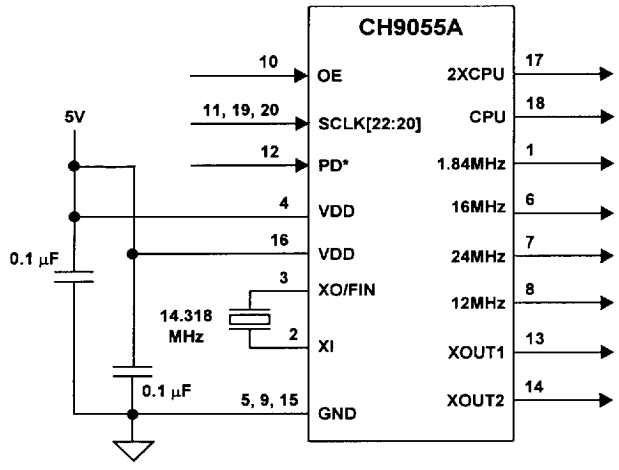


**Figure 8: Application Schematic**

Note: For other versions, please refer to pin descriptions for exact pin numbers and functions

| ORDERING INFORMATION | | | |
|---|---|---|---|
| Part number | Package type | Number of pins | Voltage supply |
| CH9055x-N | 300 mil PDIP | 20 | 5V |
| CH9055x-S | 150 mil SOIC | 20 | 5V |
| CH9055x-N-L | 300 mil PDIP | 20 | 3.3V |
| CH9055x-S-L | 150 mil SOIC | 20 | 3.3V |
| **Note**: x = frequency table version | | | |