



DESCRIPTION

The ES6128 Vibratto™S DVD processor is a super high-performance single-chip MPEG video decoding solution that integrates a state-of-the-art progressive-scan video feature to provide brilliant and sharp, flicker-free output to the video display, built-in CPRM, and S/PDIF input and output support. The ES6128 performs audio/video stream data processing, TV encoding, Macrovision™ copy protection, DVD system navigation, system control, and housekeeping functions.

The Vibratto-S DVD processor is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consisting of 32-bit RISC and 64-bit DSP processors and offers the best DVD feature set. The processing units enable simultaneous parallel execution of system commands and data processing to perform specialized encoding and decoding tasks.

The RISC processor performs bit stream parsing, control audio data output, transfer video and audio data to the vector engine and service system control and housekeeping functions. The vector engine performs audio and video micro-code processing required by A/V standards, such as Dolby® Digital, MPEG and JPEG imaging. These processing tasks include video motion compensation and estimation, loop filtering, Discrete Cosine Transforms (DCT), inverse DCT, quantization, and inverse quantization.

The Vibratto-S DVD processor supports both parallel and serial DVD loader interfaces, industry standard I²S audio data input and output, EPROM and DRAM access, and audio/video data buffering. It also supports both letterbox and pan-and-scan displays, sub-picture overlay, and On-Screen Display (OSD). In addition, the Vibratto-S DVD solution plays Karaoke, CD+G, HDCD, CD-DA, MP3, and WMA.

The ES6128 DVD processor is available in a 208-pin Plastic Quad Flat Pack (PQFP) device package.

FEATURES

- Single-chip DVD processor.
- Integrated NTSC/PAL encoder with pixel-adaptive de-interlacer and five 10-bit 54 MHz video DACs.
- High-quality progressive scan video output for flicker-free video display.
- DVD-Video, DVD-VR, VCD 1.1 and 2.0, and SVCD.
- Media playback with CD-ROM, CD-R/RW, DVD-R/RW, DVD+R/RW, and DVD-RAM.
- Up to 7.1 channel audio outputs.
- Interface for IDE devices, A/V DVD loaders.
- Interface for CF, MS, SD, MMC, and SM memory cards.
- Direct interface of 8-/16-bit DRAM up to 128-Mb capacity.
- Direct interface for up to 4 banks of 8-/16-bit EPROM or Flash EPROM for up to 4-MB for each bank.
- Macrovision 7.1 for NTSC/PAL interlaced video.
- Macrovision NTSC/PAL (480p/576p) progressive scan video.
- Simultaneous composite, S-video, and YUV outputs.
- CCIR 656/601 YUV 4:2:2 input and output.
- On-Screen Display controller supports 256 colors in 8 degrees of transparency.
- Subpicture Unit (SPU) decoder supports karaoke lyric, subtitles, and EIA-608 compliant Line 21 Captioning.
- SmartLogo™ for custom JPEG wallpaper.
- JPEG digital photo support (Kodak Picture CD™ and Fujifilm FujiColor CD™).
- ESS Music Slideshow™.
- Bass management.
- Dolby Digital (AC-3), Dolby Pro Logic™, and Pro Logic II.
- DTS™ surround.
- S/PDIF digital audio input and output.
- MPEG AAC and Multichannel.
- SRS TruSurround® and TruSurround XT™.
- Windows™ Media Audio decoding.
- Professional karaoke with full scoring scheme.
- Lead-free leads using 98%-Sn/2%-Cu or 98%-Sn/2%-Bi available with ES6128FF.



ES6128 PINOUT DIAGRAM

The device pinout for the ES6128 is shown in Figure 1.

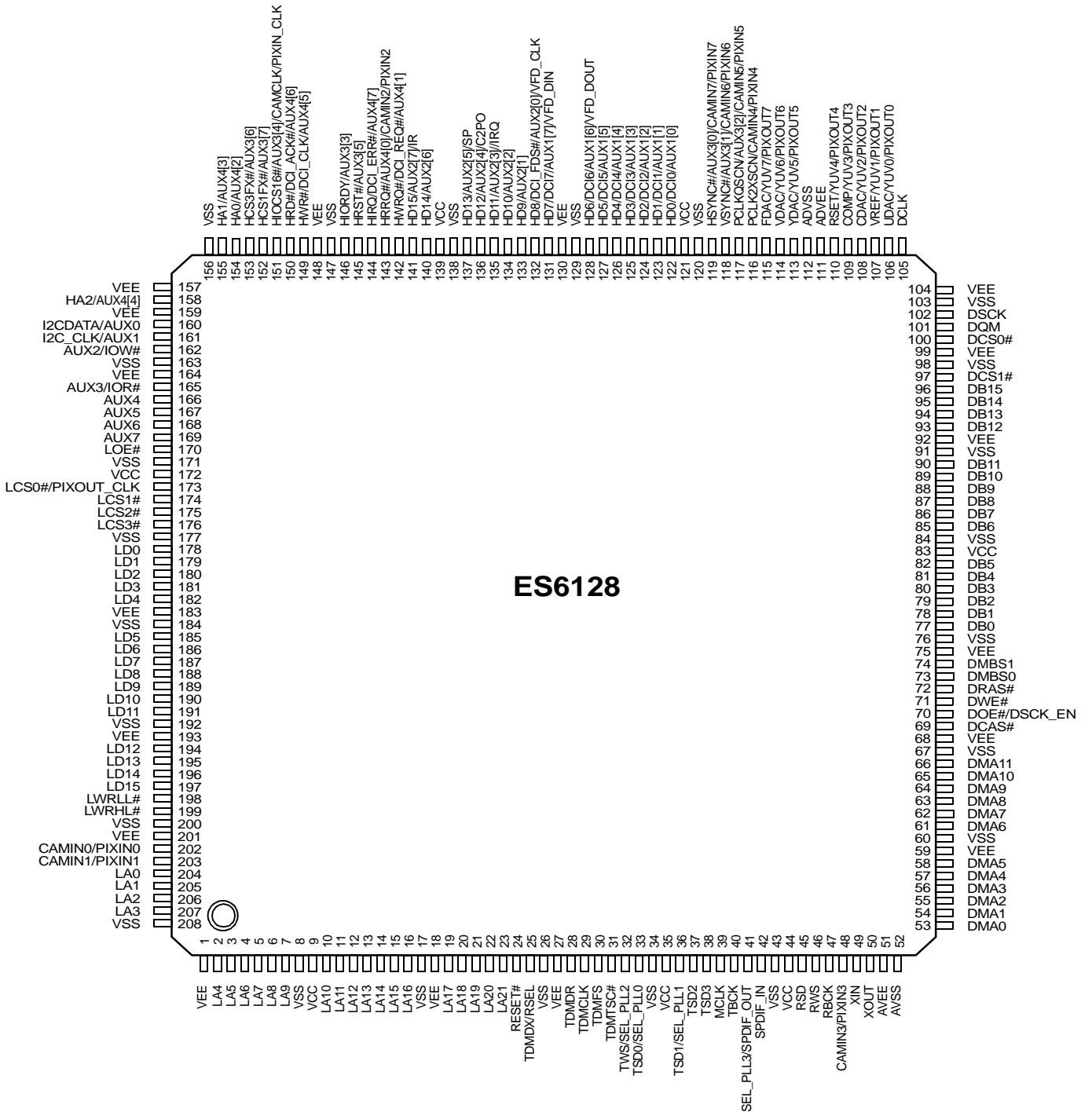


Figure 1 ES6128 Device Pinout



ES6128 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES6128.

Table 1 ES6128 Pin Description

| Name | Pin Numbers | I/O | Definition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|--|----------|---|----------|-----------|----------|--------------|---|-----------|---|------------|---|---|---|------------|---|---|---|--------|---|---|---|------------|---|---|---|-------------|---|---|---|-------------|---|---|---|------------|---|---|---|
| VEE | 1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201 | P | I/O power supply. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LA[21:0] | 2-7, 10-16, 19-23, 204-207 | O | RISC port address bus. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | 8, 17, 26, 34, 43, 60, 67, 76, 84, 91, 98, 103, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208 | G | Ground. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VCC | 9, 35, 44, 83, 121, 139, 172 | P | Core power supply. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RESET# | 24 | I | Reset input; (5V tolerant input). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDMDX | 25 | O | TDM transmit data output. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RSEL | | I | LCS3 ROM Boot Data Width Select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>RSEL</th> <th>Selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>16-bit ROM</td> </tr> <tr> <td>1</td> <td>8-bit ROM</td> </tr> </tbody> </table> | RSEL | Selection | 0 | 16-bit ROM | 1 | 8-bit ROM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RSEL | Selection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 16-bit ROM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 8-bit ROM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDMDR | 28 | I | TDM receive data input; (5V tolerant input). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDMCLK | 29 | I | TDM clock input; (5V tolerant input). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDMFS | 30 | I | TDM frame sync input; (5V tolerant input). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDMTSC# | 31 | O | TDM output enable. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TWS | 32 | O | Audio transmit frame sync output. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SEL_PLL2 | | I | System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SEL_PLL2</th> <th>SEL_PLL1</th> <th>SEL_PLL0</th> <th>PLL Settings</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>DCLK × 4.5</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>DCLK × 5.0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Bypass</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>DCLK × 4.0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>DCLK × 4.25</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>DCLK × 4.75</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>DCLK × 5.5</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>DCLK × 6.0</td> </tr> </tbody> </table> | SEL_PLL2 | SEL_PLL1 | SEL_PLL0 | PLL Settings | 0 | 0 | 0 | DCLK × 4.5 | 0 | 0 | 1 | DCLK × 5.0 | 0 | 1 | 0 | Bypass | 0 | 1 | 1 | DCLK × 4.0 | 1 | 0 | 0 | DCLK × 4.25 | 1 | 0 | 1 | DCLK × 4.75 | 1 | 1 | 0 | DCLK × 5.5 | 1 | 1 | 1 |
| SEL_PLL2 | SEL_PLL1 | SEL_PLL0 | PLL Settings | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | DCLK × 4.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | DCLK × 5.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | Bypass | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | DCLK × 4.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | DCLK × 4.25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | DCLK × 4.75 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | DCLK × 5.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | DCLK × 6.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSD0 | 33 | O | Audio transmit serial data output 0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SEL_PLL0 | | I | Refer to the description and matrix for SEL_PLL2 pin 32. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



Table 1 ES6128 Pin Description (Continued)

| Name | Pin Numbers | I/O | Definition | | | | | | |
|-----------|---------------------|----------------|---|----------|--------------|---|--------------------|---|------------|
| TSD1 | 36 | O | Audio transmit serial data output 1. | | | | | | |
| SEL_PLL1 | | I | Refer to the description and matrix for SEL_PLL2 pin 32. | | | | | | |
| TSD2 | 37 | O | Audio transmit serial data output 2. This pin must be pulled down to VSS via a 4.7-kΩ resistor for proper operation. | | | | | | |
| TSD3 | 38 | O | Audio transmit serial data output 3. | | | | | | |
| MCLK | 39 | I/O | Audio master clock for audio DAC. | | | | | | |
| TBCK | 40 | I/O | Audio transmit bit clock. TBCK is an input during reset and subsequently is programmed as an output via the AUDIOXMT register (addr 0x2000D00Ch, bit 4). | | | | | | |
| SEL_PLL3 | 41 | I | Clock source select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SEL_PLL3</th> <th>Clock Source</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Crystal oscillator</td> </tr> <tr> <td>1</td> <td>DCLK input</td> </tr> </tbody> </table> | SEL_PLL3 | Clock Source | 0 | Crystal oscillator | 1 | DCLK input |
| SEL_PLL3 | | Clock Source | | | | | | | |
| 0 | Crystal oscillator | | | | | | | | |
| 1 | DCLK input | | | | | | | | |
| SPDIF_OUT | O | S/PDIF output. | | | | | | | |
| SPDIF_IN | 42 | I | S/PDIF input; (5V tolerant input). | | | | | | |
| RSD | 45 | I | Audio receive serial data; (5V tolerant input). | | | | | | |
| RWS | 46 | I | Audio receive frame sync; (5V tolerant input). | | | | | | |
| RBCK | 47 | I | Audio receive bit clock; (5V tolerant input). | | | | | | |
| CAMIN3 | 48 | I | Camera YUV 3. | | | | | | |
| PIXIN3 | | I | CCIR656 input pixel 3. | | | | | | |
| XIN | 49 | I | 27-MHz crystal input. | | | | | | |
| XOUT | 50 | O | 27-MHz crystal output. | | | | | | |
| AVEE | 51 | P | Analog power for PLL. | | | | | | |
| AVSS | 52 | G | Analog ground for PLL. | | | | | | |
| DMA[11:0] | 53-58, 61-66 | O | DRAM address bus. | | | | | | |
| DCAS# | 69 | O | DRAM column address strobe. | | | | | | |
| DOE# | 70 | O | DRAM output enable. | | | | | | |
| DSCCK_EN | | O | DRAM clock enable. | | | | | | |
| DWE# | 71 | O | DRAM write enable. | | | | | | |
| DRAS# | 72 | O | DRAM row address strobe. | | | | | | |
| DMBS0 | 73 | O | DRAM bank select 0. | | | | | | |
| DMBS1 | 74 | O | DRAM bank select 1. | | | | | | |
| DB[15:0] | 77-82, 85-90, 93-96 | I/O | DRAM data bus. | | | | | | |
| DCS[1:0]# | 97,100 | O | DRAM chip select. | | | | | | |
| DQM | 101 | O | Data input/output mask. | | | | | | |
| DSCCK | 102 | O | Output clock to DRAM. | | | | | | |
| DCLK | 105 | I | Clock input to PLL; (5V tolerant input). | | | | | | |



Table 1 ES6128 Pin Description (Continued)

| Name | Pin Numbers | I/O | Definition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|-------------|-----------------|---|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|-------------|-------|---|---|-----|---|-------------|-------|---|---|-------|---|-------------|-----|---|---|-----|---|-------------|-------|-----|-----|-------|---|-------------|-------|-----|-----|-----|---|-------------|-------|---|----|----|---|-------------|-----|---|----|----|---|-----|------|---|---|---|---|-------------|--------|---|----|----|---|------|-------|---|---|---|----|------|-------|---|---|---|----|-----|------|---|---|---|----|-------------|-----|---|----|----|----|-------------|-------|---|----|----|----|--------|---|---|---|---|
| UDAC | 106 | O | Video DAC output. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Value</th> <th>F DAC (pin 115)</th> <th>V DAC (pin 114)</th> <th>Y DAC (pin 113)</th> <th>C DAC (pin 108)</th> <th>U DAC (pin 106)</th> </tr> </thead> <tbody> <tr><td>0</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td></tr> <tr><td>1</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td></tr> <tr><td>2</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td></tr> <tr><td>3</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td></tr> <tr><td>4</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr><td>5</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr> <tr><td>6</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr> <tr><td>7</td><td>N/A</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr> <tr><td>8</td><td>CVBS/Chroma</td><td>Chroma</td><td>Y</td><td>Pb</td><td>Pr</td></tr> <tr><td>9</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr> <tr><td>10</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr> <tr><td>11</td><td>N/A</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr> <tr><td>12</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr> <tr><td>13</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr> <tr><td>14</td><td>Chroma</td><td>Y</td><td>G</td><td>R</td><td>B</td></tr> </tbody> </table> <p>F: CVBS/chroma signal for simultaneous mode. Y: Luma component for YUV and Y/C processing. C: Chrominance signal for Y/C processing. U: Chrominance component signal for YUV mode. V: Chrominance component signal for YUV mode.</p> | Value | F DAC (pin 115) | V DAC (pin 114) | Y DAC (pin 113) | C DAC (pin 108) | U DAC (pin 106) | 0 | CVBS/Chroma | CVBS1 | Y | C | N/A | 1 | CVBS/Chroma | CVBS1 | Y | C | CVBS2 | 2 | CVBS/Chroma | N/A | Y | C | N/A | 3 | CVBS/Chroma | CVBS1 | N/A | N/A | CVBS2 | 4 | CVBS/Chroma | CVBS1 | N/A | N/A | N/A | 5 | CVBS/Chroma | CVBS1 | Y | Pb | Pr | 6 | CVBS/Chroma | N/A | Y | Pb | Pr | 7 | N/A | SYNC | G | B | R | 8 | CVBS/Chroma | Chroma | Y | Pb | Pr | 9 | CVBS | CVBS1 | G | B | R | 10 | CVBS | CVBS1 | G | R | B | 11 | N/A | SYNC | G | R | B | 12 | CVBS/Chroma | N/A | Y | Pr | Pb | 13 | CVBS/Chroma | CVBS1 | Y | Pr | Pb | 14 | Chroma | Y | G | R | B |
| Value | | F DAC (pin 115) | V DAC (pin 114) | Y DAC (pin 113) | C DAC (pin 108) | U DAC (pin 106) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | CVBS/Chroma | CVBS1 | Y | C | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | CVBS/Chroma | CVBS1 | Y | C | CVBS2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | | CVBS/Chroma | N/A | Y | C | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | | CVBS/Chroma | CVBS1 | N/A | N/A | CVBS2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | | CVBS/Chroma | CVBS1 | N/A | N/A | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | | CVBS/Chroma | CVBS1 | Y | Pb | Pr | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | | CVBS/Chroma | N/A | Y | Pb | Pr | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | | N/A | SYNC | G | B | R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | | CVBS/Chroma | Chroma | Y | Pb | Pr | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | | CVBS | CVBS1 | G | B | R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | | CVBS | CVBS1 | G | R | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | | N/A | SYNC | G | R | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | | CVBS/Chroma | N/A | Y | Pr | Pb | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | CVBS/Chroma | CVBS1 | Y | Pr | Pb | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | Chroma | Y | G | R | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| YUV0 | | O | YUV pixel 0 output data. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PIXOUT0 | | O | CCIR656 output pixel 0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VREF | 107 | I | Internal voltage reference to video DAC. Bypass to ground with 0.1- μ F capacitor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| YUV1 | | O | YUV pixel 1 output data. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PIXOUT1 | | O | CCIR656 output pixel 1. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CDAC | 108 | O | Video DAC output. Refer to description and matrix for UDAC pin 106. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| YUV2 | | O | YUV pixel 2 output data. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PIXOUT2 | | O | CCIR656 output pixel 2. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| COMP | 109 | I | Compensation input. Bypass to ADVEE with 0.1- μ F capacitor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| YUV3 | | O | YUV pixel 3 output data. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PIXOUT3 | | O | CCIR656 output pixel 3. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RSET | 110 | I | DAC current adjustment resistor input. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| YUV4 | | O | YUV pixel 4 output data. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PIXOUT4 | | O | CCIR656 output pixel 4. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ADVEE | 111 | P | Analog power for video DAC. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



Table 1 ES6128 Pin Description (Continued)

| Name | Pin Numbers | I/O | Definition |
|-----------|-------------|-----|---|
| ADVSS | 112 | G | Analog ground for video DAC. |
| YDAC | 113 | O | Video DAC output. Refer to description and matrix for UDAC pin 106. |
| YUV5 | | O | YUV pixel 5 output data |
| PIXOUT5 | | O | CCIR656 output pixel 5. |
| VDAC | 114 | O | Video DAC output. Refer to description and matrix for UDAC pin 106. |
| YUV6 | | O | YUV pixel 6 output data. |
| PIXOUT6 | | O | CCIR656 output pixel 6. |
| FDAC | 115 | O | Video DAC output. Refer to description and matrix for UDAC pin 106. |
| YUV7 | | O | YUV pixel 7 output data. |
| PIXOUT7 | | O | CCIR656 output pixel 7. |
| PCLK2XSCN | 116 | I/O | 27-MHz video output pixel clock. |
| CAMIN4 | | I | Camera YUV 4. |
| PIXIN4 | | I | CCIR656 input pixel 4. |
| PCLKQSCN | 117 | O | 13.5-MHz video output pixel clock. |
| AUX3[2] | | I/O | Aux3 data I/O; (5V tolerant input). |
| CAMIN5 | | I | Camera YUV 5. |
| PIXIN5 | | I | CCIR656 input pixel 5. |
| VSYNC# | 118 | I/O | Vertical sync; (5V tolerant input). |
| AUX3[1] | | I/O | Aux3 data I/O; (5V tolerant input). |
| CAMIN6 | | I | Camera YUV 6. |
| PIXIN6 | | I | CCIR656 input pixel 6. |
| HSYNC# | 119 | I/O | Horizontal sync; (5V tolerant input). |
| AUX3[0] | | I/O | Aux3 data I/O; (5V tolerant input). |
| CAMIN7 | | I | Camera YUV 7. |
| PIXIN7 | | I | CCIR656 input pixel 7. |
| HD[5:0] | 122-127 | I/O | Host data bus lines; (5V tolerant input). |
| DCI[5:0] | | I/O | DVD channel data I/O; (5V tolerant input). |
| AUX1[5:0] | | I/O | Aux1 data I/O; (5V tolerant input). |
| HD6 | 128 | I/O | Host data bus line; (5V tolerant input). |
| DCI6 | | I/O | DVD channel data I/O; (5V tolerant input). |
| AUX1[6] | | I/O | Aux1 data I/O; (5V tolerant input). |
| VFD_DOUT | | I | VFD data output. |
| HD7 | 131 | I/O | Host data bus line; (5V tolerant input). |
| DCI7 | | I/O | DVD channel data I/O; (5V tolerant input). |
| AUX1[7] | | I/O | Aux1 data I/O; (5V tolerant input). |
| VFD_DIN | | I | VFD data input. |



Table 1 ES6128 Pin Description (Continued)

| Name | Pin Numbers | I/O | Definition |
|----------|-------------|-----|--|
| HD8 | 132 | I/O | Host data bus line; (5V tolerant input). |
| DCI_FDS# | | I/O | DVD input sector start; (5V tolerant input). |
| AUX2[0] | | I/O | Aux2 data I/O; (5V tolerant input). |
| VFD_CLK | | I | VFD clock input. |
| HD9 | 133 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[1] | | I/O | Aux2 data I/O; (5V tolerant input). |
| HD10 | 134 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[2] | | I/O | Aux2 data I/O; (5V tolerant input). |
| HD11 | 135 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[3] | | I/O | Aux2 data I/O; (5V tolerant input). |
| IRQ | | O | IRQ. |
| HD12 | 136 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[4] | | I/O | Aux2 data I/O; (5V tolerant input). |
| C2PO | | I | C2PO error correction flag from CD-ROM; (5V tolerant input). |
| HD13 | 137 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[5] | | I/O | Aux2 data I/O; (5V tolerant input). |
| SP | | I | 16550 UART serial port input. |
| HD14 | 140 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[6] | | I/O | Aux2 data I/O; (5V tolerant input). |
| HD15 | 141 | I/O | Host data bus line; (5V tolerant input). |
| AUX2[7] | | I/O | Aux2 data I/O; (5V tolerant input). |
| IR | | I | IR remote control input; (5V tolerant input). |
| HWRQ# | 142 | O | Host write request. |
| DCI_REQ# | | O | DVD control interface request. |
| AUX4[1] | | I/O | Aux4 data I/O; (5V tolerant input). |
| HRRQ# | 143 | O | Host read request. |
| AUX4[0] | | I/O | Aux4 data I/O; (5V tolerant input). |
| CAMIN2 | | I | Camera YUV 2. |
| PIXIN2 | | I | CCIR656 input pixel 2. |
| HIRQ | 144 | I/O | Host interrupt. |
| DCI_ERR# | | I/O | DVD channel data error; (5V tolerant input). |
| AUX4[7] | | I/O | Aux4 data I/O; (5V tolerant input). |
| HRST# | 145 | O | Host reset. |
| AUX3[5] | | I/O | Aux3 data I/O; (5V tolerant input). |
| HIORDY | 146 | I | Host I/O ready. |
| AUX3[3] | | I/O | Aux3 data I/O; (5V tolerant input). |



Table 1 ES6128 Pin Description (Continued)

| Name | Pin Numbers | I/O | Definition |
|------------|------------------------------|-----|---|
| HWR# | 149 | I/O | Host write. |
| DCI_CLK | | I/O | DVD channel data clock; (5V tolerant input). |
| AUX4[5] | | I/O | Aux4 data I/O; (5V tolerant input). |
| HRD# | 150 | O | Host read. |
| DCI_ACK# | | I/O | DVD channel data valid; (5V tolerant input). |
| AUX4[6] | | I/O | Aux4 data I/O; (5V tolerant input). |
| HIOCS16# | 151 | I | Device 16-bit data transfer. |
| AUX3[4] | | I/O | Aux3 data I/O; (5V tolerant input). |
| CAMCLK | | I | Camera port pixel clock input. |
| PIXIN_CLK | | I | CCIR656 input pixel clock. |
| HCS1FX# | 152 | O | Host select 1. |
| AUX3[7] | | I/O | Aux3 data I/O; (5V tolerant input). |
| HCS3FX# | 153 | O | Host select 3. |
| AUX3[6] | | I/O | Aux3 data I/O; (5V tolerant input). |
| HA[2:0] | 154, 155, 158 | I/O | Host address bus. |
| AUX4[4:2] | | I/O | Aux4 data I/Os; (5V tolerant input). |
| AUX0 | 160 | I/O | Auxiliary port 0 (open collector); (5V tolerant input). |
| I2CDATA | | I/O | I ² C data I/O; (5V tolerant input). |
| AUX1 | 161 | I/O | Auxiliary port 1 (open collector); (5V tolerant input). |
| I2C_CLK | | I/O | I ² C clock I/O; (5V tolerant input). |
| AUX2 | 162 | I/O | Auxiliary port; (5V tolerant input). |
| IOW# | | O | I/O write strobe (LCS1). |
| AUX3 | 165 | I/O | Auxiliary port; (5V tolerant input). |
| IOR# | | O | I/O read strobe (LCS1). |
| AUX4-7 | 166-169 | I/O | Auxiliary ports; (5V tolerant input). |
| LOE# | 170 | O | RISC port output enable. |
| LCS0# | 173 | O | RISC port chip select 0. |
| PIXOUT_CLK | | O | CCIR656 output pixel clock. |
| LCS[3:1]# | 174-176 | O | RISC port chip select [3:1]. |
| LD[15:0] | 178-182, 185-191, 194-197 | I/O | RISC port data bus; (5V tolerant input). |
| LWRLL# | 198 | O | RISC port low-byte write enable. |
| LWRHL# | 199 | O | RISC port high-byte write enable. |
| CAMIN0 | 202 | I | Camera YUV 0. |
| PIXIN0 | | I | CCIR656 input pixel 0. |
| CAMIN1 | 203 | I | Camera YUV 1. |
| PIXIN1 | | I | CCIR656 input pixel 1. |



SYSTEM BLOCK DIAGRAM

A sample system block diagram for the ES6128 Vibratto-S DVD player board design is shown in Figure 2.

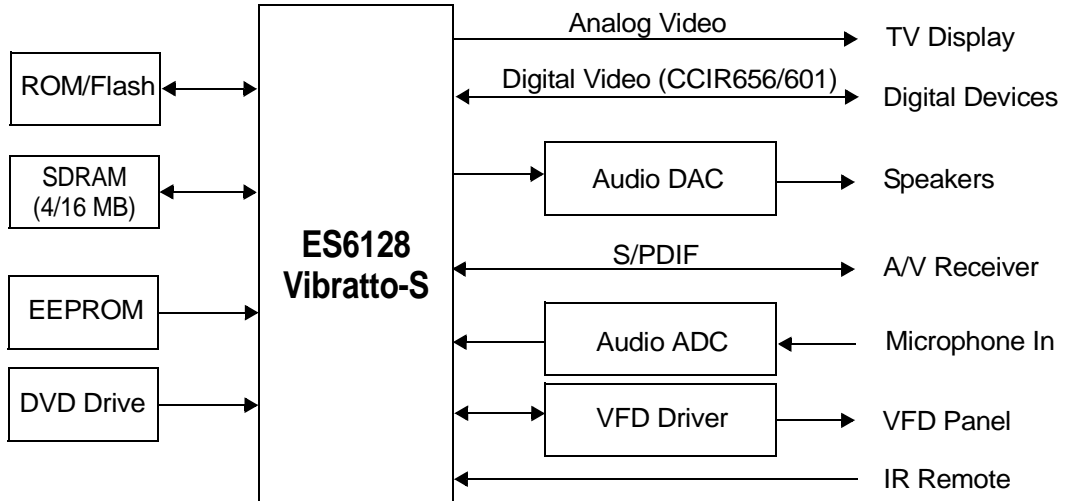


Figure 2 ES6128 Vibratto-S System Block Diagram

FUNCTIONAL DESCRIPTION

Figure 3 shows the internal block diagram for the ES6128 Vibratto-S DVD processor.

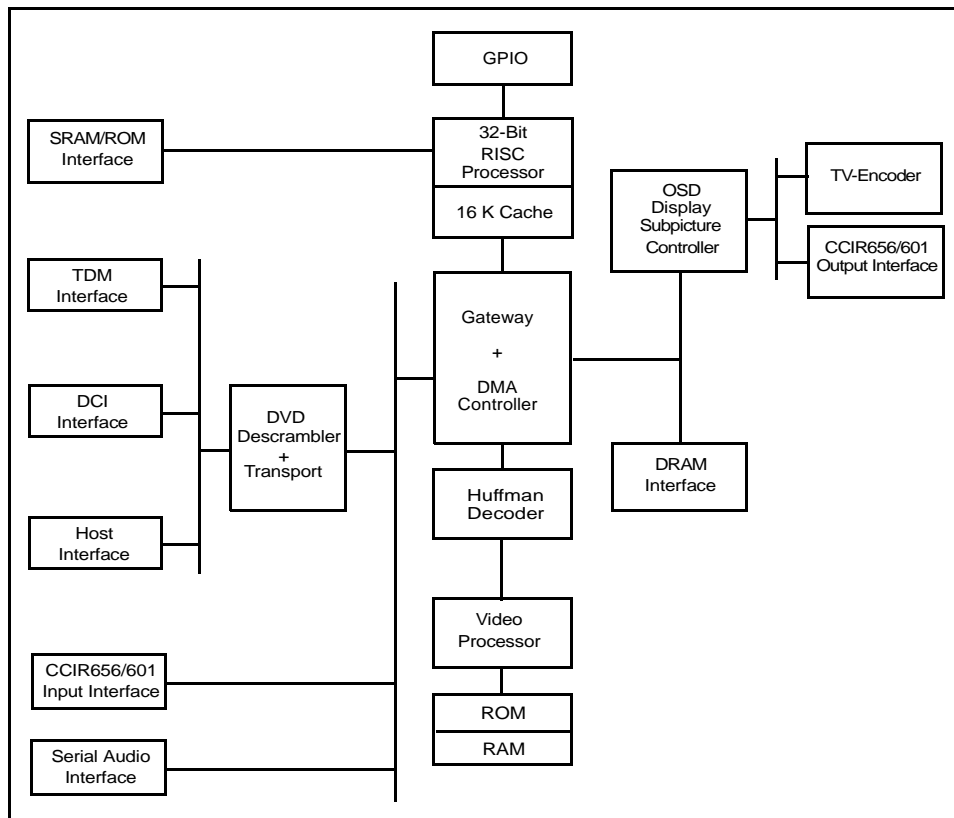


Figure 3 ES6128 Vibratto-S Block Diagram

ORDERING INFORMATION

| Part Number | Description | Package |
|-------------|---|--------------|
| ES6128F | Vibratto-S DVD, Progressive scan, and TV encoder | 208-pin PQFP |
| ES6128FF | Vibratto-S DVD, Progressive scan, and TV encoder with lead-free leads | 208-pin PQFP |

The letter F at the end of the part number identifies the package type PQFP. The second letter F indicates lead-free leads with the device.

Other Vibratto-S DVD Processors

| Part Number | Description | Package |
|-------------|--|--------------|
| ES6168FA | Vibratto-S DVD, Progressive scan, MPEG-4, DVD-Audio, and TV encoder | 208-pin PQFP |
| ES6168FAF | Vibratto-S DVD, Progressive scan, MPEG-4, DVD-Audio, and TV encoder with lead-free leads | 208-pin PQFP |
| ES6178F | Vibratto-S DVD, Progressive scan, DivX (certified), DVD-Audio, and TV encoder | 208-pin PQFP |
| ES6178FF | Vibratto-S DVD, Progressive scan, DivX (certified), DVD-Audio, and TV encoder with lead-free leads | 208-pin PQFP |

The letter F at the end of the part number identifies the package type PQFP. The second letter F indicates lead-free leads with the device.



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