PM7375

Revision F Device Errata

Issue 4: December, 1997

CONTENTS

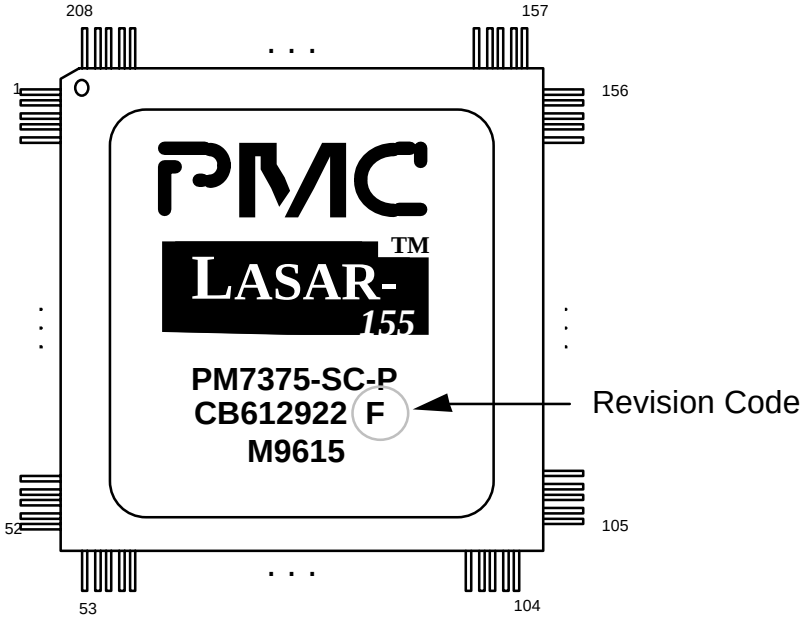
1. INTRODUCTION

This document is the Device Errata Sheet for the Revision F of the PM7375 LASAR-155™. This document is **not** the errata sheet for the LASAR-155 Long form Datasheet (PMC-931127).

1.1. Device Identification

This document applies only to Revision F of PM7375 LASAR-155. As illustrated in Figure 1.1, the Revision Code is marked on the face of the device. The LASAR-155 Revision F is either package in a 208-pin MQFP or a 208-pin slugged PQFP.

Figure 1.1: LASAR-155 Branding Format.



1.2. References

- PMC-931127, LOCAL ATM SEGMENTATION AND REASSEMBLY & PHYSICAL LAYER INTERFACE, Issue 4, September, 1996.
- PMC-951042, LASAR-155 Network Interface Card (NIC) Optical Reference Design, Issue 2, April, 1996.

  PCI Special Interest Group, PCI Local Bus Specification, June 1, 1995, Version 2.1.

2. LASAR-155 REVISION F ANOMALIES

This section describes any anomalies associated with Revision F of the LASAR-155. For each anomaly, the known work-around and the operating constraints, with and without the work-around, are also described.

2.1. (FIXED) PCID Controller Synchronization

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.2. (FIXED) PCI problem During Target Burst

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.3. (FIXED) PCI Bus Release problem

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.4. (FIXED) CRU Diagnostic Loopback

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.5. (FIXED) AD[15:8] Byte Corruption

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.6. (FIXED) PCI Bus Device Select (IDSEL) problem

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.7. (FIXED) Retry Transaction After a Target Abort

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.8. (FIXED) PCI Bus Lock-up During Burst Read Transaction

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.9. (FIXED) Incorrectly Sets the Parity Error

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.10. (FIXED) Incorrect RMDR Status Field for CRC-10

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.11. (FIXED) Transmit Buffer Must Be DWORD in Size

This problem was first reported in PMC-960529 Issue 2 has been fixed in Rev F.

2.12. Race Condition in Reference Queues

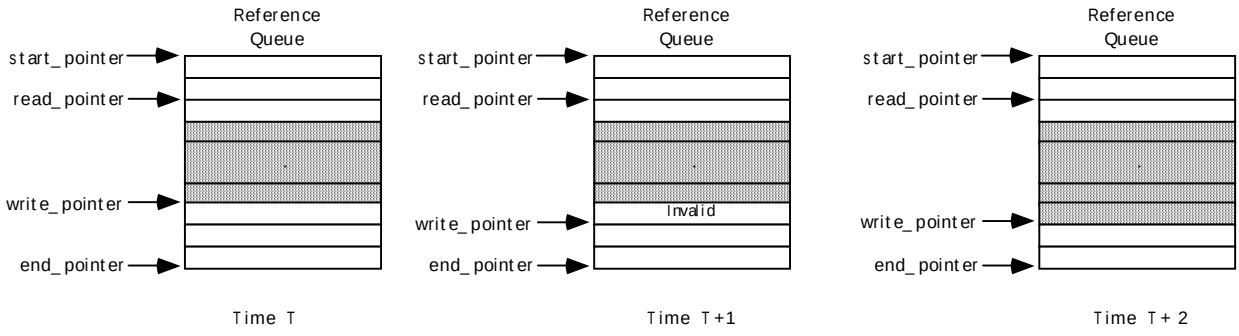
Description

There is a possibility of a race condition when the LASAR-155 inserts a new element into the following queues:

- Receive Management Descriptor Reference (RMDR) Ready Queue,
- Receive Packet Descriptor Reference (RPDR) Ready Queue, or
- Transmit Descriptor Reference (TDR) Free Queue.

The race condition is that the write_pointer may be incremented before the element is fully written into the queue. When this occurs, the last queue element is invalid until the write operation is fully completed. This is illustrated in the example below:

Figure 2.1: Queue Race Condition Example.

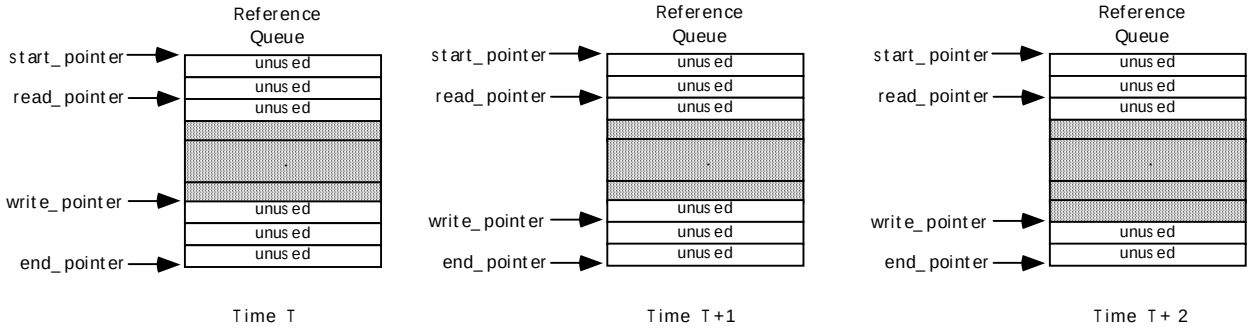


- At "Time T", the LASAR-155 is ready to insert a new element into the Reference Queue.
- At "Time T+1", the write_pointer is increment before the new element is written into the queue. As a result, the position referenced by the write_pointer contains invalid data.
- At "Time T+2", the new element is added. Now the position referenced by the write_pointer contains valid data.

Work Around

To ensure that only valid queue elements are read, the device driver first marks all queue elements as "unused". This is done when initializing the queues. When there is a notification that one or more elements are inserted into the queue, the device driver checks whether the queue element is "unused". If it is marked as "unused", the device driver will read the same position again until the new element is added. This is illustrated in the following example:

Figure 2.2: Work Around to Queue Race Condition.



- At "Time T", the LASAR-155 is ready to insert a new element into the Reference Queue. All the unused elements are marked "unused".
- At "Time T+1", the write_pointer is increment before the new element is written into the queue. As a result, the position referenced by the write_pointer still contains the "unused" tag.
- At "Time T+2", the new element is added. Now the position referenced by the write_pointer contains valid data.

It is recommended that the "unused" be defined as "FFFFF".

Operating Constraints With Work Around

None.

Operating Constraints Without Work Around

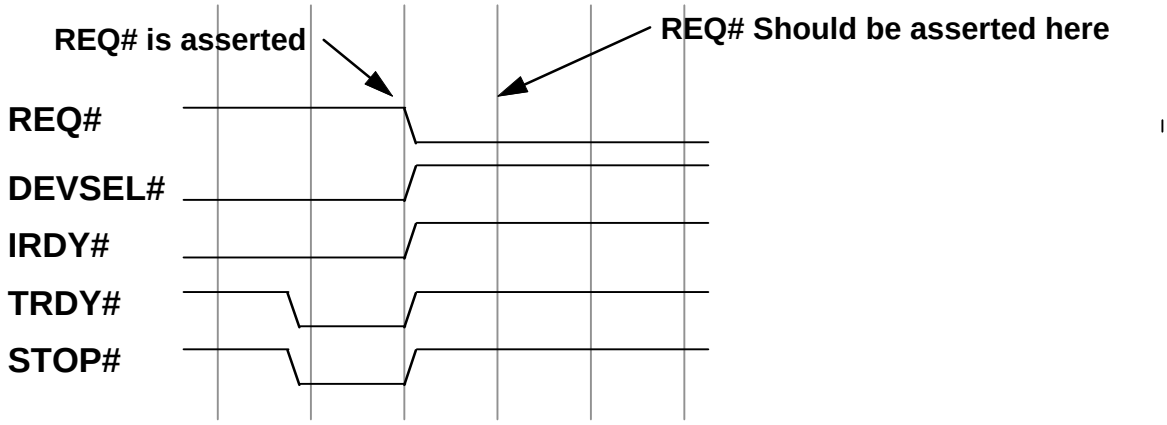
There is a possibility that the queue element may contain invalid data.

2.13. REQ# is asserted during Idle State after target disconnect

Description

After a target disconnect, the LASAR-155 does not deassert the REQ# for two clock cycles when it should. According to the PCI 2.1 specification, when the current data transaction is terminated by the target, either Retry or Disconnect, the master must deassert its REQ# for a minimum of two clock cycles. These two clock cycles are defined as follows: the first clock cycle being when the bus transitions to the Idle state (at the end of the transaction where STOP# is asserted) and the second either one clock cycle before or one clock cycle after the Idle state. The LASAR-155 correctly deasserts REQ# for one clock cycle before the Idle state and then incorrectly reasserts the REQ# during the Idle state.

Figure 2.3 After a Target Disconnect the REQ# is asserted during Idle State.



Work Around

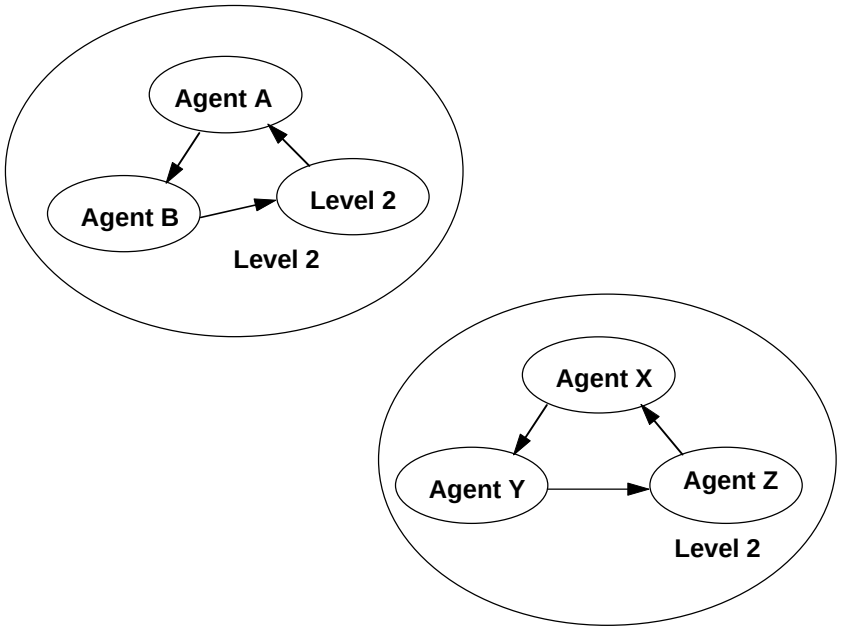
The impact of this problem depends on the arbitration scheme used. This problem should not affect normal operation of the PCI bus.

Typical arbitration schemes use a combination of agent priority and round robin access. The LASAR-155 will request the bus one clock cycle earlier than it should. However, other agents will still have access to the bus via the round robin arbitration.

A typical arbitration example that implements a fairness algorithm is found in the PCI Local Bus Specification 2.1. This example assumes a two level bus architecture with the higher priority agents attached to level 1 (low latency or greater bandwidth).

Second level agents have equal access to the bus with respect to other second level agents. However, second level agents, as a group, have equal access to the bus as level one agents as shown in the following example:

Figure 2.4 Typical PCI Bus Arbitration using a "Fairness Algorithm"



First level:

Agent A, Agent B, and Level 2 (where level 2 is the next level 2 agent requesting the bus.

Second Level:

Agent X, Agent Y, Agent Z

If all agents have their REQ# lines asserted then the agents accessing the bus would be as follows:

A, B, Level 2 (this time it is X)

A, B, Level 2 (this time it is Y)

A, B, Level 2 (this time it is Z)

Normal operation should not be affected with the appropriate use of a Fairness algorithm for bus arbitration.

Operating Constraints With Work Around

None

Operating Constraints Without Work Around

There is a possibility that the LASAR-155 would unfairly request access to the bus.

2.14. LASAR-155 Changes STOP# during the current data phase

Description

During a Target Termination (Retry and Disconnect termination) the assertion of STOP# must be asserted at the beginning of the data phase (for a Target Retry and Target Disconnect) or at the end of the data phase (Target Disconnect). The LASAR-155 changes STOP# after the beginning of the data phase but before the end of the data phase when a parity error on the address phase and 3 wait states on IRDY#.

Work Around

There is no work around required. According to the PCI Local Bus 2.1 specification, once the Master (assertion of IRDY#) or Target (assertion of TRDY# or STOP#) has committed to the current data transfer, they cannot stop the data transfer until the data phase is complete. Therefore, even if STOP# is asserted in the middle of the data phase, the current data transfer is completed before the Master or Target will end the transaction.

Operating Constraints With Work Around

None

Operating Constraints Without Work Around

None

2.15. Transaction without driving the address and command bus

Description

During a multiple transaction when the bus is parked on the LASAR-155, the address of the second transfer is not properly synchronized with the FRAME# assertion during the address phase.

Work Around

This error does not occur if the bus is not parked on the LASAR-155. An alternative is to program the arbiter to park the bus on itself and not on the LASAR-155.

Operating Constraints With Work Around

None

Operating Constraints Without Work Around

The PCI bus may lock-up if the bus is parked on the LASAR-155

2.16. LASAR-155 still acts as master after a Target Abort and SOE_E=1

Description

During a Target Abort, the LASAR-155 continues acting as a PCI master and completes transmission of the PDU. This also occurs when SOE_E = 1.

Work Around

There is no work around.

A target abort is generated when the target determines that the master has requested a transaction that the target is incapable of completing or has determined that a fatal error has occurred. This is a serious error where the target indicates that the transaction must be stopped and it does not want the master to repeat the request again. The LASAR-155 should stop the transaction after a target abort, however, by completing transmission of the PDU, the LASAR-155 does not stop operation gracefully when there is a major system error. A target abort will require that the system be reset regardless of how the LASAR-155 completes the transaction.

Operating Constraints With Work Around

None

Operating Constraints Without Work Around

None

2.17. Burst read of LASAR-155 PCI registers causes DMA error

Description

A burst read of registers in the range 0x310 - 0x3B4 H during LASAR-155 DMA access corrupts the state of the internal DMA engine. As a result the LASAR-155 performs a Master Abort and generates a SERRI interrupt. After the failure, the MABT bit is set high and the system may require a hardware reset.

Work Around

There is no problem when the above registers are accessed with single data phase transactions. These transactions must be out of sequence or from higher address to lower address to avoid bursts.

Operating Constraints With Work Around

None

Operating Constraints Without Work Around

The LASAR-155 may cause the system to crash as a result of a SERRI error.

2.18. Thermal Considerations

Description

The LASAR-155 may require heat sinking in certain applications. Please consult PMC's application note: PMC-970394 Heat Sinking and the LASAR-155.

2.19 Boundary Scan

Description and Work Around

The bi-directional multi-purpose port of the of the RDAT[7:0], RSOC, TDAT[15:0] and TSOC signals is non-compliant with the boundary scan standard in the input direction. To make them fully bidirectional, two external inputs, outside the boundary scan cell chain, need to be controlled as indicated in the following table (in addition to the RDATENB and TDATENB cells). Consequently, the boundary scan file, to be provided by PMC-SIERRA will be a subset of the full boundary scan file.

Input Pins	Value on SYSCLK	Value on RXPHYBP
RSOC	L	H

RDAT	L	H
TSOC	L	X
TDAT	L	X

NOTES

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PMC-960529 (r4) Issue date: December 1997.