75A, 600V MAGNUM MOTOR DRIVES

FEATURES

- ***600 Vdc Drive for 270 Vdc Motors***
- ***75 Amps @25°C, 50 Amps @85°C***
- ***Operates with Brushless, Brush and Induction Motors***
- ***Input to Output Ground Isolation with Floating Output Stage***
- ***Short Circuit Protection***
- ***Trapezoidal or Sinusoidal Compatible***
- ***DSP/Microprocessor Compatible***
- ***PW-83075P6 - Half-Bridge Drive***
- ***PW-84075P6 - Half-Bridge Drive with Current Sense***
- ***PW-85075P6 - Half-Bridge Drive with Regenerative Clamp***

DESCRIPTION

The PW-83075P6, PW-84075P6 and PW-85075P6 are half-bridge drive modules which contain isolated switch drivers, a pair of solid state switches, an isolated power supply, current sensing feedback (PW-84075P6 only) and a regenerative clamp protection circuit (PW-85075P6 only). The three modules can be used, in any combination, to create drives for brush, brushless DC motors or AC induction motors. The logic inputs and current sense signal are compatible with DSP/microprocessors and/or FPGA/ASIC circuits used to control the motor drives. These modular drives are capable of operating from either ±135Vdc or 270Vdc power source that is totally isolated from the logic input signals. The modules are fault tolerant from output shorts, loss of any or all power supplies and power supply sequencing.

APPLICATIONS

The high reliability and flexibility of these drives make them suitable for Military and Aerospace applications. Among the many applications are: actuator systems for primary and secondary flight controls on aircraft; fan and compressor motor drives for environmental conditioning; pump motors for fuel and hydraulic fluid; antenna and radar positioning; and thrust vector position control of missiles, drones, and RPV's.

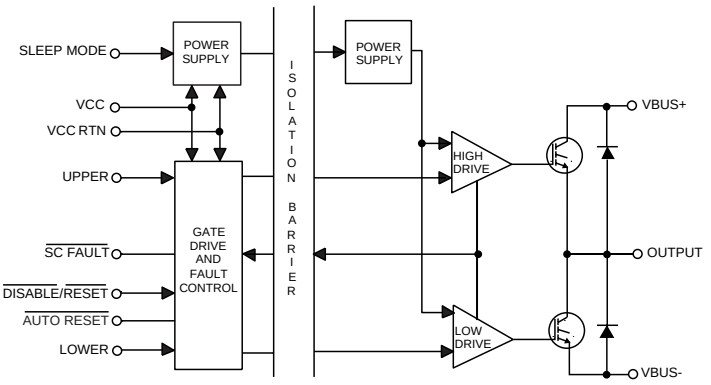


FIGURE 1A. PW-83075P6 BLOCK DIAGRAM

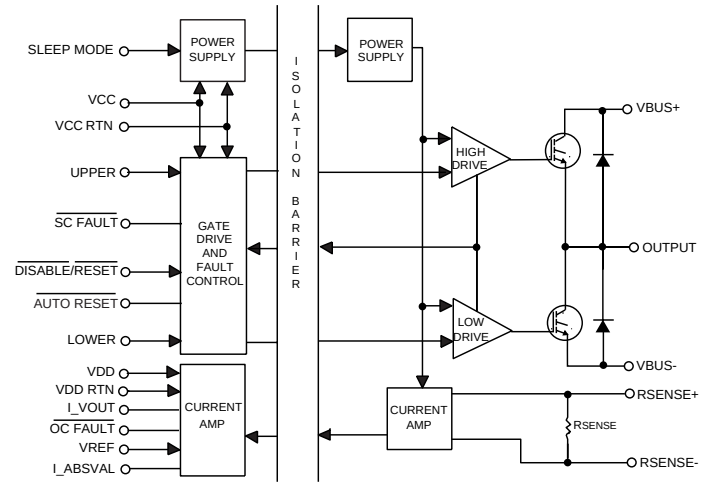


FIGURE 1B. PW-84075P6 BLOCK DIAGRAM

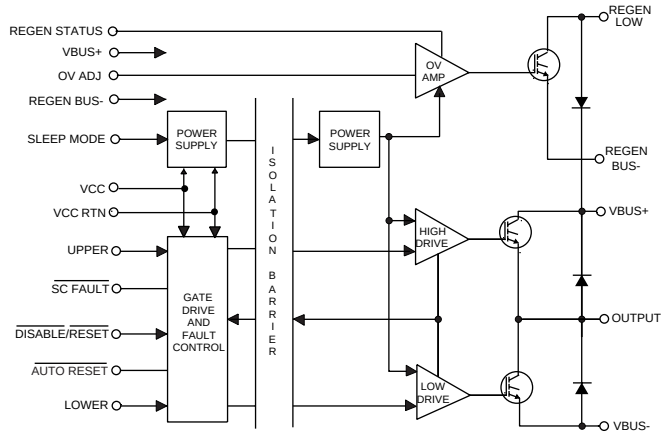


FIGURE 1C. PW-85075P6 BLOCK DIAGRAM

TABLE 1. PW-8X075P6 ABSOLUTE MAXIMUM RATINGS
(TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	VALUE	UNITS
Drive Supply Voltage	VBUS+ to VBUS-	600	Vdc
Logic Power-In Supply Voltage	VCC	5.5	Vdc
Input Logic Voltage	UPPER, LOWER, $\overline{\text{DISABLE/RESET}}$, SLEEPMODE, $\overline{\text{AUTO RESET}}$	5.5	Vdc
Continuous Output Current	I_O	75	A
Peak Output Current (10 ms)	I_{PEAK}	150	A
Storage Temperature Range	Tcs	-65 to +125	°C
Intermittent Case Operating Temperature	T_{CI}	-55 to +125	°C
Continuous Case Operating Temperature	Tc	-55 to +100	°C
Junction Temperature, Power Devices	Tj	+150	°C
Junction Temperature, Other Components	T_J	+125	°C
Ground Isolation Voltage (Note 2)	V_{ISO}	2500	Vdc

TABLE 2. PW-8X075P6 SPECIFICATIONS
(TC = +25°C, VCC = VDD = 5V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT STAGE						
Drive Supply Voltage (motor)	VBUS+ to VBUS-	Unipolar/Bipolar	0	270	600	Vdc
Output Switch Transistors (each)						
Continuous Current Drive	I_O	+25°C case			75	A
		+85°C case			50	A
Peak Current	I_{PEAK}	+85°C case, ≤15 ms			100	A
Short Circuit Trip Current (note 1)	I_{SC}	≤5 µs	200	350	400	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$	I_O = 50A		2.2	2.6	Vdc
FLYBACK DIODE						
Instant Forward Voltage	V_F	I_O = 50A		1.7	1.9	Vdc
Reverse Recovery Time @ T_j = +125° C	T_{rr}	I_O = 50A		175		ns
Reverse recovery Peak Current	Irm	di/dt = 480A/µs		19	33	A
		IF = 50A (90 °C)				
Reverse Leakage Current @ T_j = +25° C	I_r	VBUS = 480Vdc		30	325	µA
Reverse Leakage Current @T_j = +125° C	I_r	VBUS = 480Vdc			17	mA
OUTPUT SWITCHING CHARACTERISTICS (See FIGURE 5)						
Turn-on Propagation Delay	t_d(on)		390		470	ns
Turn-off Propagation Delay	t_d(off)		740		840	ns
Disable Propagation Delay	t_{sd}			100		µs
Turn-on Rise Time	t_r		100		200	ns
Turn-off Fall Time	t_f		140		200	ns
Sleep_Mode Delay	tsleepu			3.7		ms
Output Switching Frequency	fPWM		0		35	KHz
POWER AND LOGIC SUPPLY (PW83075P6 ONLY)						
Voltage	VCC		4.5	5.0	5.5	Vdc
Current	ICC	f = 25 KHz		110		mA
Control Inputs						
UPPER, LOWER, $\overline{\text{DISABLE/RESET}}$						
$\overline{\text{AUTO RESET}}$		VCC = 4.5V				
High Level Input Voltage	VIH		1.55	2.5	3.15	Vdc
Low Level Input Voltage	VIL		0.9	1.6	2.45	Vdc
Hysteresis Voltage	VHYST		0.4	0.9	2.1	Vdc
UPPER, LOWER						
High Level Input Current	IIH	Vin = VCC	22	23	24	µA
Low Level Input Current	IIL	Vin = 0V	0	0.1	100	nA
RESET/DISABLE						
High Level Input Current	IIH	Vin = VCC		0		µA
Low Level Input Current	IIL	Vin = 0V	22	23	24	µA
AUTO_RESET						
High Level Input Current	IIH	Vin = VCC		0		µA
Low Level Input Current	IIL	Vin = 0V	1.3	1.4	1.5	mA
SLEEP_MODE		VCC = 4.5V				
High Level Input Voltage	VIH		2.4			Vdc
Low Level Input Voltage	VIL				0.8	Vdc
High Level Input Current	IIH	Vin = VCC		0.1		µA
Low Level Input Current	IIL	Vin = 0V	0.4		0.5	mA

TABLE 2. PW-8X075P6 SPECIFICATIONS
(TC = +25°C, VCC = VDD = 5V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
UPPER-LOWER DEADTIME	tdead		1.0			µs
AUTO_RESET Delay to output off	tdoff.auto			202		ms
AUTO_RESET Delay to output enabled	tdon.auto			3.0		ms
RESET pulsewidth to clear SC_FAULT	tpw.reset		100			ns
Cycle time between AUTO_RESET retries	tcycle.auto		40	100		ms
CONTROL OUTPUTS						
SC_FAULT						
High Level Current	ISCFLTH	Vo = VCC	22	23	24	µA
Low Level Current	ISCFLTL	Vo = 0.4V	5	10		mA
THERMAL						
Maximum Thermal Resistance - IGBT	θjc	Each Output Switch		0.5	0.55	°C/W
- Diode	θjc			0.8		°C/W
Junction Temperature Range	Tj		-55		+150	°C
Case Operating Temperature	Tc		-55		+100	°C
Case Storage Temperature	Tcs		-65		+125	°C
MECHANICAL						
Maximum Lead Soldering Temp	Ts				+250	°C
Mounting Torque					3	in-lbs
Weight					TBD	oz (gr)

Notes: 1. VBUS+ to VBUS- must be ≥ 10V (during short circuit) for short circuit protection to operate.
2. From VCC RTN to VBUS+, VBUS-, OUTPUT, REGEN LOW, RSENSE+, RSENSE-.

TABLE 3. PW-84075P6 SPECIFICATIONS
(TC= +25°C VCC = VDD = 5V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Amplifier						
I_Vout Trasnfer Ratio	Gvout	Vref = 5.0V		29.76		mV/A
I_Vout Gain Error	Evout		-6		6	%
I_Vout Offset	Vos	Vref = 5.0V	-30		30	mV
I_Vout Offset Drift	TCVos	Vref = 5.0V	-90		110	ppm/°C
I_Vout Gain %	Gvout%	0A = Vref/2		0.595		%Vref/A
I_Vout Offset %	Vos%Vref		-0.6		0.6	%Vref
I_Vout Offset % Drift	TCVos%		-18		22	ppm/Vref/°C
I_VABS Gain	Gvabs	0A = 0V		59.52		mV/A
I_VABS Gain Error	Evabs		-8		8	%
I_VABS Offset	Vosabs	Vref = 5.0V	-131		131	mV
I_VABS Offset Drift	TCVosabs	Vref = 5.0V	-90		110	ppm/°C
I_VABS Gain %	Gvout%	0A = 0V		1.19		%Vref/A
I_VABS Offset %	Vosabs% Vref		-2.6		2.6	%Vref
I_VABS Offset % Drift	TCVosabs%		-18		22	ppm/Vref/°C
Delay Time	tdelay			9	20	µs
Bandwidth	fBW		20	30		kHz
Linear Range	Irange			±50		A
OC_FAULT trip level	IOC		±75	±85	±95	A
Reference voltage input current	Ivref			0.26	1	mA
OC_FAULT						
High Level Input Current	IOCFLTH	Vo = VDD		0.2	15	uA
Low Level Input Current	IOCFLTL	Vo = 0.8V	4			mA
Power and Logic Supply						
Voltage	VCC, VDD		4.5	5	5.5	V
Logic Supply Current	ICC	Gate Off / SLEEP MODE		11		mA
		25Khz Gate Pulsing		136	200	mA
Current Amplifier Supply Current	IDD		8	10	20	mA

TABLE 4. PW-85075P6 SPECIFICATIONS
(TC = +25°C, VCC = VDD = 5V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Over Voltage Transistor						
Continuous Current Drive	Io	+25°C Case			35	A
		+85°C Case			30	A
Peak Current	I_{PEAK}	+85°C Case, 15 ms			60	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$			2.0	3.0	Vdc
Reverse Leakage @ T_J = +25°C	Ir	600 Vdc			250	µA
Reverse Leakage @ T_J = +125°C	Ir	600 Vdc			1.0	mA
Over Voltage flyback Diode						
Reverse Leakage @ Tc = +25°C	Ir	480 Vdc		20	50	µA
Reverse Leakage @ Tc = +125°C	Ir	480 Vdc		1	7	mA
Over Voltage Trip	Vtrip	no external adjustments	370	400	430	Vdc
Trip Level Hysteresis	Vhyst		35	40	45	Vdc
Power and Logic Supply						
Voltage	VCC		4.5	5	5.5	V
Current	ICC	Gate Off/ Sleep Mode		11		mA
		25Khz Gate Pulsing		137	250	mA
REGEN STATUS (ref. to REGEN BUS-)						
High Level Output Voltage	VOHstatus	I0 = 0	13.8	15	15.6	Vdc
Low Level Output Voltage	VOLstatus	I0 = 0		0.2	0.4	Vdc
Output resistance	Rstatus		4.2	4.75	4.8	KΩ
Vtrip rise to status ON Delay	tdon.status			36		µs
Vtrip fall status OFF Delay	tdoff.status			48		µs
THERMAL						
Maximum Thermal Resistance	θjc	Over Voltage Switch		0.7	0.85	°C/W

INTRODUCTION

The PW-8X075P6 is a universal modular half-bridge motor drive intended for use with brush, brushless DC and AC induction motors in aerospace applications.

The isolation barrier, which separates the power and control stage, attenuates the ground noise generated from high speed, high power switching. All signals from the control to the power sections are isolated from power and ground of the other section. This eliminates false triggering of the input signals and the need for creative grounding schemes. The isolation barrier also allows the user to operate the output stage from either unipolar or bipolar power supplies without level shifting the input signals.

A built in power supply located in the control stage provides power to all electronics in the power stage. This eliminates the need for refresh cycles or external power supplies for the gate drive circuitry and allows switching duty cycles from 0 - 100%.

PW-84075P6 provides current sensing of either motor current or DC bus current. This current signal can be used as a feedback signal in a servo drive to create a torque loop.

The output power transistors are protected from a short circuit or overvoltage condition (requires PW-85075P6) applied to the output pins. When a short circuit condition is detected, the output transistor is shut down and a flag is active indicating a short has occurred. When an overvoltage condition is detected, the overvoltage switch is enabled and a external load dump resistor is connected across the high voltage bus. A status flag is active indicating an overvoltage condition has occurred.

FUNCTIONAL AND *PIN* DESCRIPTIONS: (FOR PW-83075P6, PW-84075P6 AND PW-85075P6 UNLESS NOTED)

UPPER, LOWER

The UPPER and LOWER are CMOS Schmitt-trigger inputs and control the gate drives of the output transistors. Each input is electrically isolated from the output. A deadband, as shown in FIGURE 2, between UPPER and LOWER inputs is necessary to prevent output cross conduction.

$\overline{\text{SC FAULT}}$

The $\overline{\text{SC FAULT}}$ output signal indicates when the output of the motor drive has experienced a short circuit condition. The signal is normally at a logic high (H). A transition to a logic low (L) will occur once a short circuit condition is detected. See **SHORT CIRCUIT OPERATION** for more detail.

$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$

The $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$ control input is CMOS Schmitt-trigger input and enables (reset) or disables the controller. When the $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$ input receives a logic low (L) pulse for at least 0.1 µs, the $\overline{\text{SC FAULT}}$ output will go high (H) indicating that the internal circuitry has been enabled or reset. To reset the motor drive, a logic low (L) must be presented to the $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$ inputs when the $\overline{\text{AUTO RESET}}$ is inactive or at a logic high (H).

$\overline{\text{AUTO RESET}}$

When the $\overline{\text{AUTO RESET}}$ is tied to $\overline{\text{SC FAULT}}$, the protection circuit will reset automatically after the short circuit fault has occurred, enabling the output to respond to the input commands. See **SHORT CIRCUIT OPERATION** for more detail.

SHORT CIRCUIT OPERATION

The PW-8X075P6 outputs are completely short-circuit-protected from either a hard or soft short (required PW-84075 and some external circuit) to the VBUS+ or VBUS- lines. Each output transistor is individually short-circuit (hard) protected by circuitry that detects the desaturation voltage for that transistor during a short condition. Once a hard short circuit condition is detected, the active output transistors are shutdown. If the $\overline{\text{AUTO RESET}}$ is tied to $\overline{\text{SC FAULT}}$, the circuit will auto reset, remove the short circuit flag, and reactivate the output transistor within 40 to 100ms.

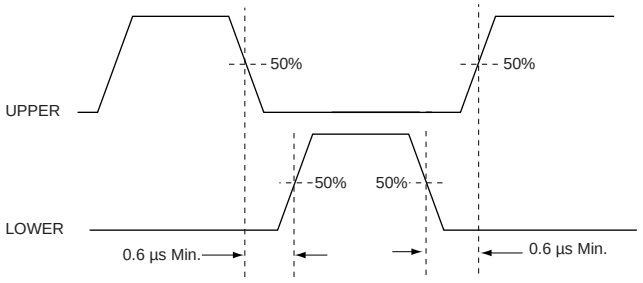


FIGURE 2. PW-8X075P6 DEAD BAND REQUIREMENT

If the short is still present, the circuit will repeat the shut down and auto reset until the short is clear. The users can use the DISABLE/RESET (H) to shut down the gate drivers if a short persists. The AUTO RESET is inactive when it presented a logic high (H). Protecting against a soft-short requires a PW-84075 (current sensing) and external circuitry. When a soft-short occurs, the external circuit can activate the SLEEPMODE (H) and shut down the gate drivers.

SLEEP MODE

The SLEEP MODE input turns the internal power supply on or off. A logic high (H) on the SLEEP MODE input disables the internal power supply, disabling the motor drive output. No damage will occur to the motor drive during turn on or turn off of the power supply. Additionally, no special power up sequence is required. A logic low (L) turns the power supply on and allows the motor drive to operate normally.

VCC, VCC RTN

The VCC and VCC RTN are power connections that supply input power to the internal power supply, the gate drive and fault control circuits.

VBUS+, VBUS-

VBUS+ and VBUS- are the high voltage power connections to the output stage. The high voltage can be either unipolar, +V and ground or bipolar, +/- V. External capacitor filtering will be required. See DDC applications note AN/H-6.

OUTPUT

The output connects to one input of the motor and applies VBUS+, VBUS-, or high impedance to the motor based on the state of the control inputs. It is capable of sourcing or sinking up to 75 Amps, and the output can withstand a short circuit to VBUS+ or VBUS- without any damage by automatically turning itself off (Zstate).

VDD, VDD RTN (APPLIES TO THE PW-84075P6 ONLY)

The VDD and VDD RTN supply input power to the current amplifier.

I_VOUT (APPLIES TO PW-84075P6 ONLY)

The voltage on the I_VOUT pin represents current passing through RSENSE in the direction shown in the block diagram. This I_VOUT voltage is scaled by the input voltage at VREF, where

$$I\_VOUT = (VREF/2) + (VREF/150) * I\_RSENSE$$

where, I_RSENSE is current through RSENSE

I_VOUT is electrically isolated from the output stage. When the power supply is shut down (SLEEP MODE input high), the voltage at I_VOUT will indicate 0V.

VREF (APPLIES TO PW-84075P6 ONLY)

A voltage reference from an external source is connected to the VREF pin to set the output voltage scale for I_VOUT.

RSENSE+, RSENSE- (APPLIES TO PW-84075P6 ONLY)

These pins are across RSENSE and can be connected in series with the output, VBUS+ or VBUS- to measure current. The internal connections to RSENSE are Kelvin to minimize errors. However, these pins can be connected absolutely anywhere within the isolation restrictions on the pins (600V to power pins, 2500V to logic pins).

I_ABSVAL (APPLIES TO PW-84075P6 ONLY)

The I_ABSVAL output voltage is the absolute value of the I_VOUT voltage signal. The scale is 0 to VREF for +/- current in RSENSE.

OC FAULT (APPLIES TO PW-84075P6 ONLY)

The OC FAULT output is an open drain output which indicates that current flowing through RSENSE has exceeded the overcurrent threshold. Once the fault threshold is exceeded, the output transitions from open drain to low within 6 µs.

REGEN STATUS (APPLIES TO PW-85075P6 ONLY)

The REGEN STATUS pin is referenced to REGEN BUS-. It indicates the state of the regen clamp switch, H = on, L = off. An external opto-isolator input can be connected between REGEN STATUS and REGEN BUS- to translate this status to logic circuits, if desired.

OV ADJ (APPLIES TO PW-85075P6 ONLY)

The PW-85075P6 is internally set for a trip voltage of 400V. To set a different trip voltage, an external resistor is connected from the OV ADJ pin to either REGEN BUS- or VBUS+ pins (See FIGURES 4A and 4B). These pins are available on the control pins. This resistor should be selected for the voltage, Vmax, for the overvoltage switch to turn on.

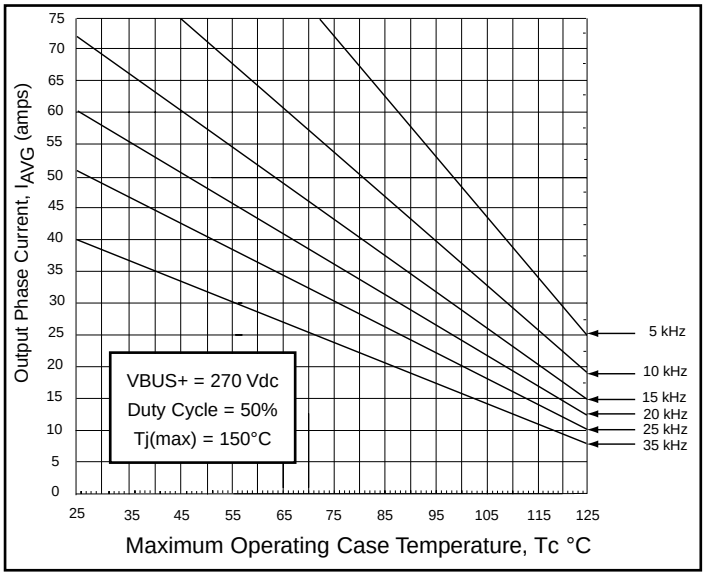
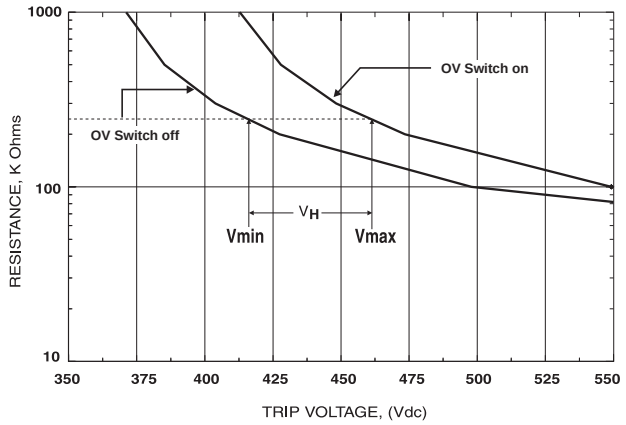


FIGURE 3. PW-8X075P6 OUTPUT PHASE CURRENT VS. MAXIMUM OPERATING CASE TEMPERATURE

NOTE:
VBUS+ (27) and REGEN BUS- (26) on the power-pin side are also connected to pin 22 and 17 on the control-pin side, respectively, for ease of connecting the external resistor.

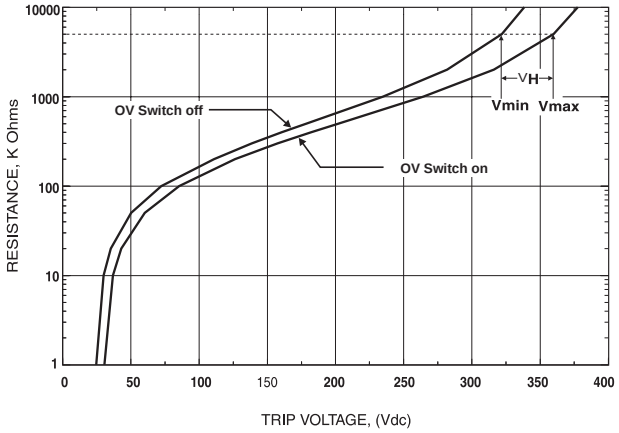
REGEN LOW, REGEN BUS-(APPLIES TO PW-85075P6 ONLY)

An external load dump resistor is connected between REGEN LOW and VBUS+. When VBUS+ reaches the level set by the OV ADJ, the internal clamp circuit will apply the load dump resistor from VBUS+ to the VBUS-, thereby dissipating the regenerative energy in the external resistor. In addition, REGEN BUS- has to be externally connected to VBUS- for the clamp circuit to work properly. This connection (PCB traces or wire) has to be able to carry the regenerative current.



NOTE: V_H = HYSTERESIS VOLTAGE

FIGURE 4A. PW-8X075P6
TYPICAL OVER VOLTAGE TRIP VS. OV ADJUST SETTING WITH EXTERNAL RESISTOR CONNECTED TO REGEN BUS-



NOTE: V_H = HYSTERESIS VOLTAGE

FIGURE 4B. PW-8X075P6
TYPICAL OVER VOLTAGE TRIP VS. OV ADJUST SETTING WITH EXTERNAL RESISTOR CONNECTED TO VBUS+

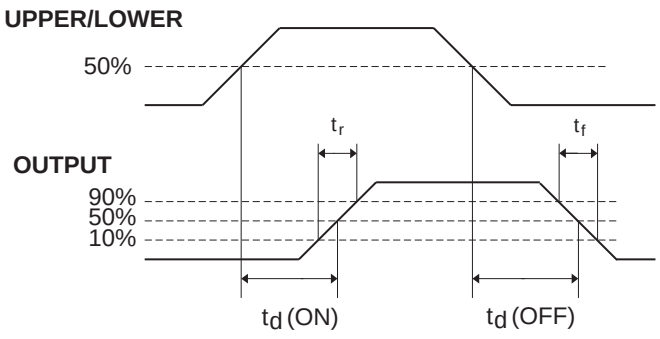


FIGURE 5. PW-8X075P6 INPUT/OUTPUT TIMING RELATIONSHIP

TABLE 5. PW-8X075P6 TRUTH TABLE

UPPER	LOWER	$\overline{\text{DISABLE}}$/ $\overline{\text{RESET}}$	SLEEP-MODE	OUTPUT
0	0	0	1	Z
1	0	0	1	VBUS+
0	1	0	1	VBUS-
1	1	0	1	*
X	X	1	X	Z
X	X	X	0	Z

X = Indicates that this input is irrelevant
Z = High Impedance (off).
* = Illegal command that will cause one of the outputs to fault.

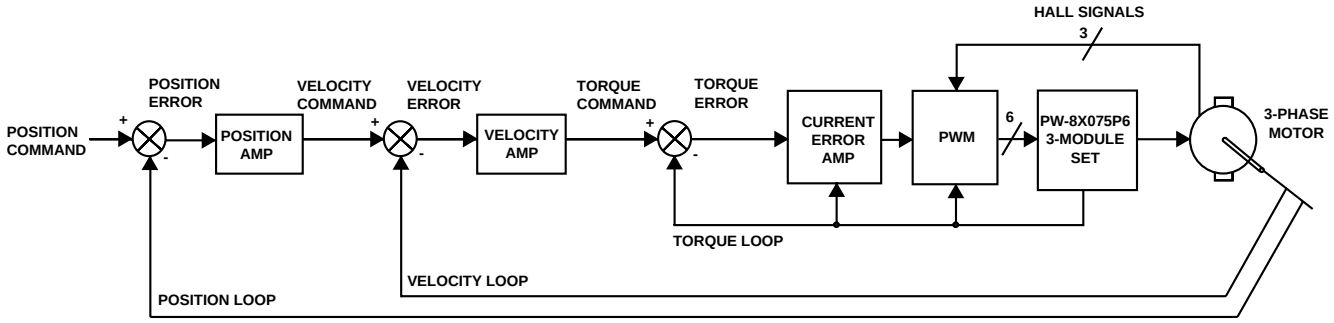


FIGURE 6. TYPICAL POSITION AND VELOCITY CONTROL LOOP

POWER DISSIPATION (see FIGURE 7)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses. Consider the following operating conditions

VBUS = +270V
I_{OA} = 40A (see FIGURE 7); I_{OB} = 50A (see FIGURE 7)
ton = 50µs (see FIGURE 7); T = 100µs (period)
$V_{CE(SAT)}$ = 2.0V (see TABLE 2, I_O = 50A, T_C = +25°C)
ts1 = 200ns (see Figure 7); ts2 = 200ns (see FIGURE 7)
fo = 10kHz (switching frequency)
V_F is the diode forward voltage, TABLE 2, I_0 = 50A, TC = +25°C
V_F(avg) = 1.35V

1. Conduction Losses (P_C)

$P_C = I_{AVE} \times V_{CE(SAT)} \times (ton / T)$
$I_{AVE} = (I_{OB} + I_{OA}) / 2$
$I_{AVE} = (50A + 40A) / 2 = 45$
$P_C = 45A \times 2.0V \times (50µs / 100µs)$
$P_C = 45W$

2. Switching Losses (P_S)

$P_S = (E_{ON} + E_{OFF}) \times fo$
$E_{ON} = ts1 \times VBUS \times I_{OA} / 6$
$E_{ON} = 200ns \times 270V \times 40A / 6$
$E_{ON} = .00045J$

$E_{OFF} = ts2 \times VBUS \times I_{OB} / 6$
$E_{OFF} = 200ns \times 270V \times 50A / 6$
$E_{OFF} = .00036J$
$P_S = 10000 \times (.00045 + .00036)$
$P_S = 8.1W$

3. Flyback diode Losses (Pd)

$Pd = I_{AVE} \times V_F(avg) \times (1- (ton / T))$
$Pdf = 45A \times 1.35V \times [1 - (50µs / 100µs)]$
$Pdf = 30.38W$

Transistor Power Dissipation (P_T)

To calculate the maximum power dissipation of the output transistor / diode pair as a function of the case temperature, use the following equation.

$$P_Q = P_C + P_S + Pdf$$

Total Hybrid Power Dissipation (P_{Hybrid})

To calculate Total Power Dissipated in the hybrid add the power dissipation of each conducting transistor / diode pair. Typically, only two transistor / diode pairs are conducting at any given time.

$$P_{TOTAL} = \sum_{i=1}^{6} [P_{Qi}] \text{ where i = each transistor/diode pair}$$

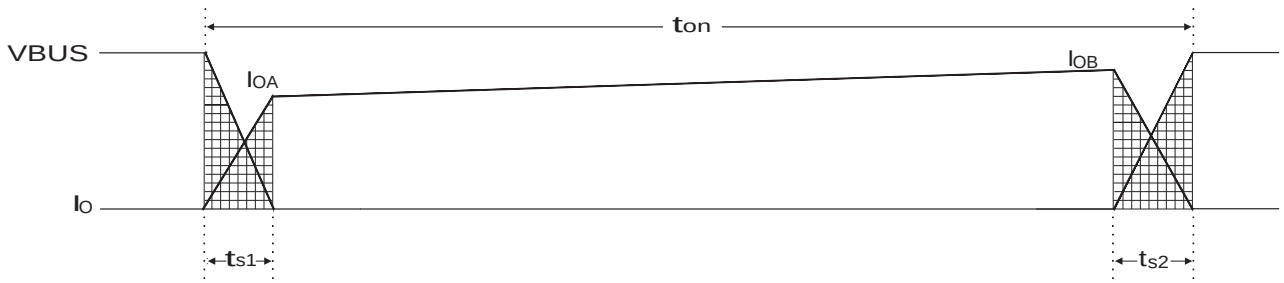


FIGURE 7. OUTPUT CHARACTERISTICS

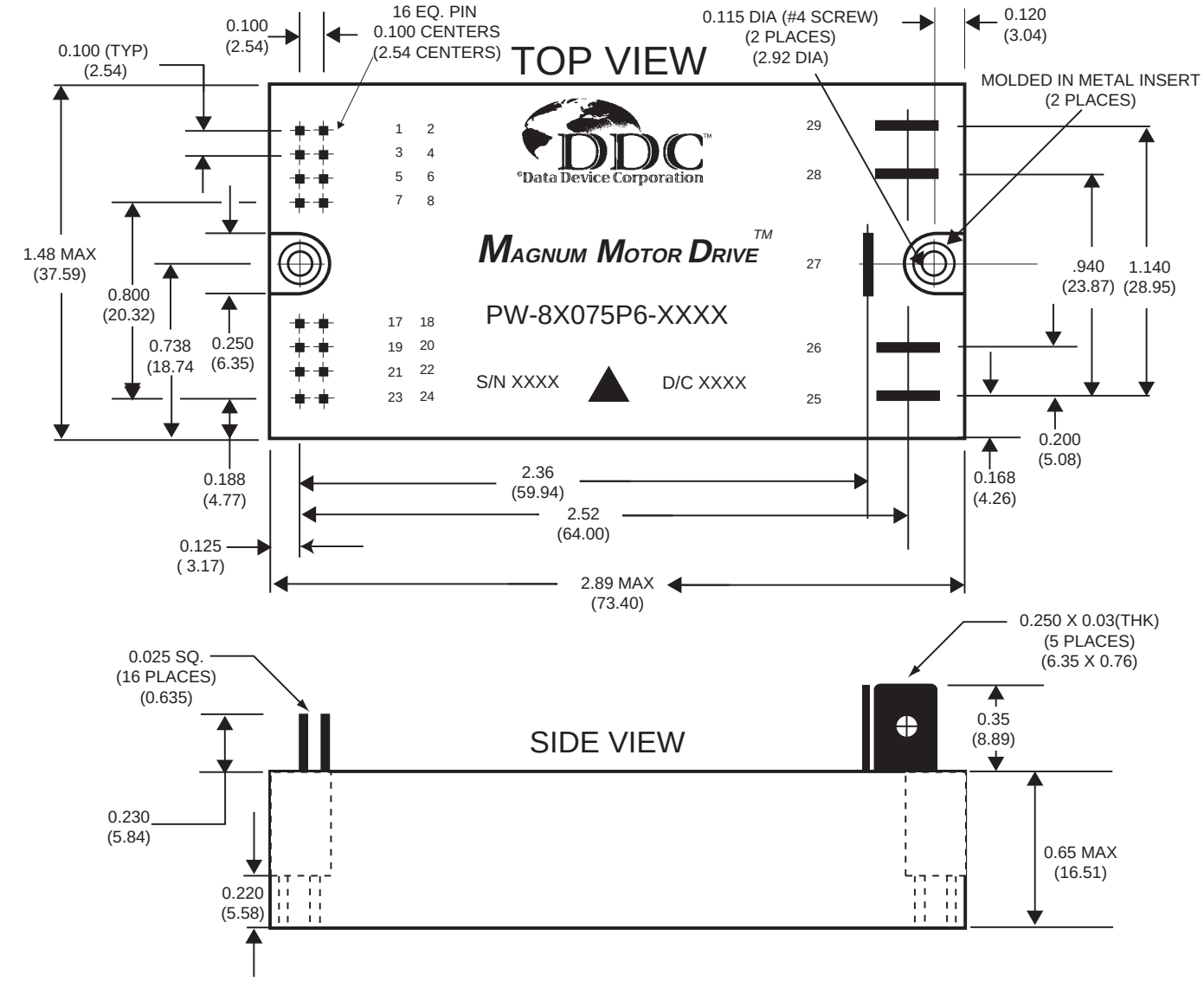
TABLE 5: PIN ASSIGNMENTS - PRELIMINARY (contact factory for latest pin assignment)			
PIN #	**FUNCTIONS DESCRIPTION**		
	PW-83075P6	***PW-84075P6***	***PW-85075P6***
1	$\overline{\text{DISABLE}}/\overline{\text{RESET}}$	$\overline{\text{DISABLE}}/\overline{\text{RESET}}$	$\overline{\text{DISABLE}}/\overline{\text{RESET}}$
2	VCC	VCC	VCC
3	UPPER	UPPER	UPPER
4	VCC RTN	VCC RTN	VCC RTN
5	LOWER	LOWER	LOWER
6	SLEEP MODE	SLEEP MODE	SLEEP MODE
7	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$
8	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$
17	NC	VREF	REGEN BUS-
18	NC	I_VOUT	REGEN STATUS
19	NC	I_ABSVAL	NC
20	NC	VDD	OV ADJ
21	NC	VDD RTN	NC
22	NC	$\overline{\text{OC FAULT}}$	VBUS+
23	NC	NC	NC
24	NC	NC	NC
25	NC	RSENSE-	REGEN LOW
26	NC	RSENSE+	REGEN BUS-
27	VBUS+	VBUS+	VBUS+
28	OUTPUT	OUTPUT	OUTPUT
29	VBUS-	VBUS-	VBUS-

APPLICATIONS:

Figure 9A shows an example of position and/or velocity control hook-up with inner torque loop using the Digital Signal Processor (DSP) for motor control. Using software, the DSP can be implemented with one of a range of several motor control algorithms, such as SVM (Space Vector modulation) or other FO (Field Oriented) control depending on the specific application.

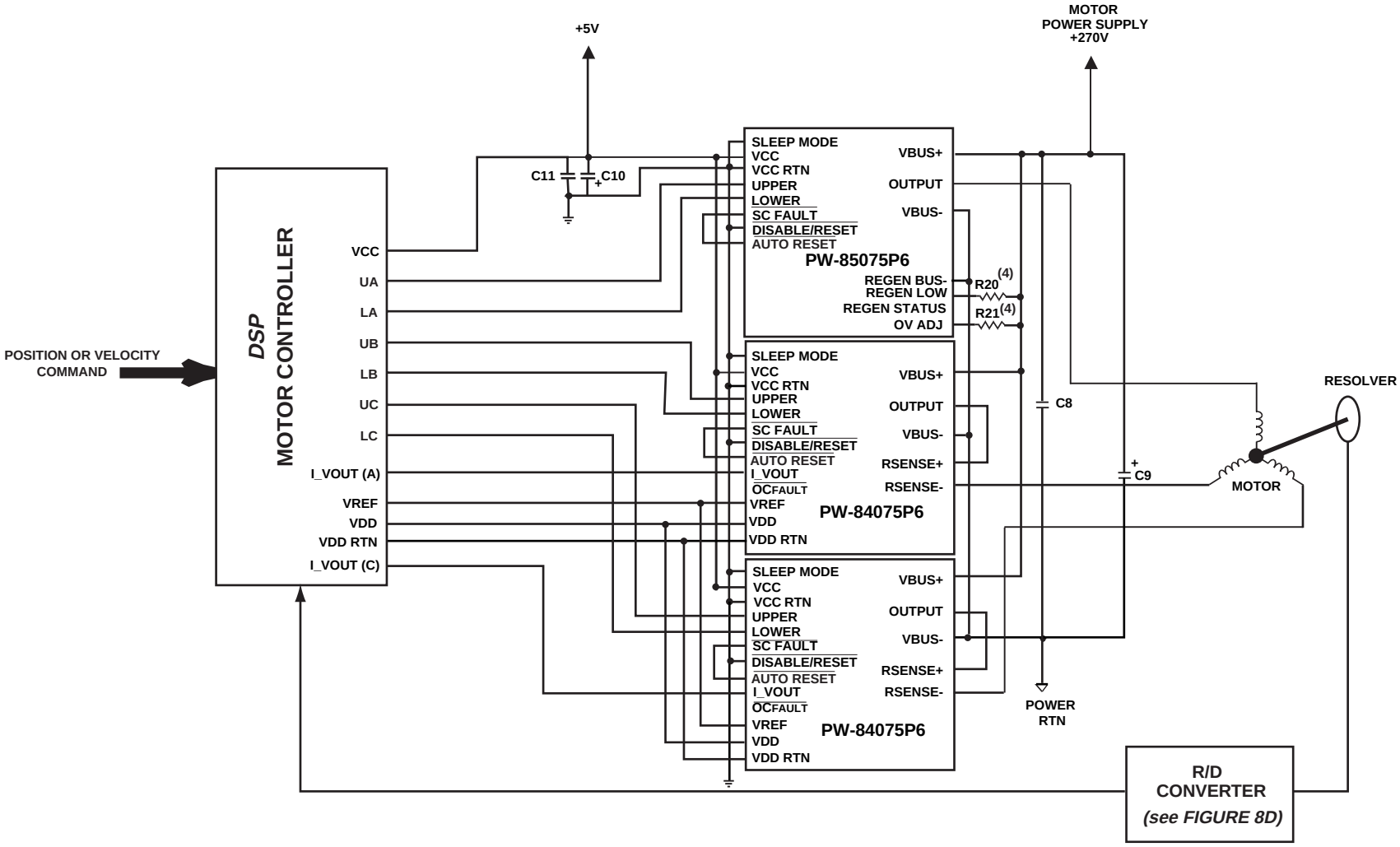
Figure 9B shows an example of torque control loop with regenerative clamp protection using UC-1625, two PW-84075P6 and one PW-85075P6. Two PW-84075P6 (½ bridge with current sense) sense the current in motor phase A and C. I_ABSVAL pins on each of the PW-84075P6 can be tied together to generate a single composite analog output which is compared to the torque commanded input to produce an error signal. UC1625 use this error signal to regulate the output current (or torque) by controlling the duty cycle of the output transistors.

For the case when the resolver/syncho are available instead of Hall-effect devices, the circuit shown in Figure 9C converts the resolver (sin and cos) signals to Hall signals which can used to commutate the output transistors.



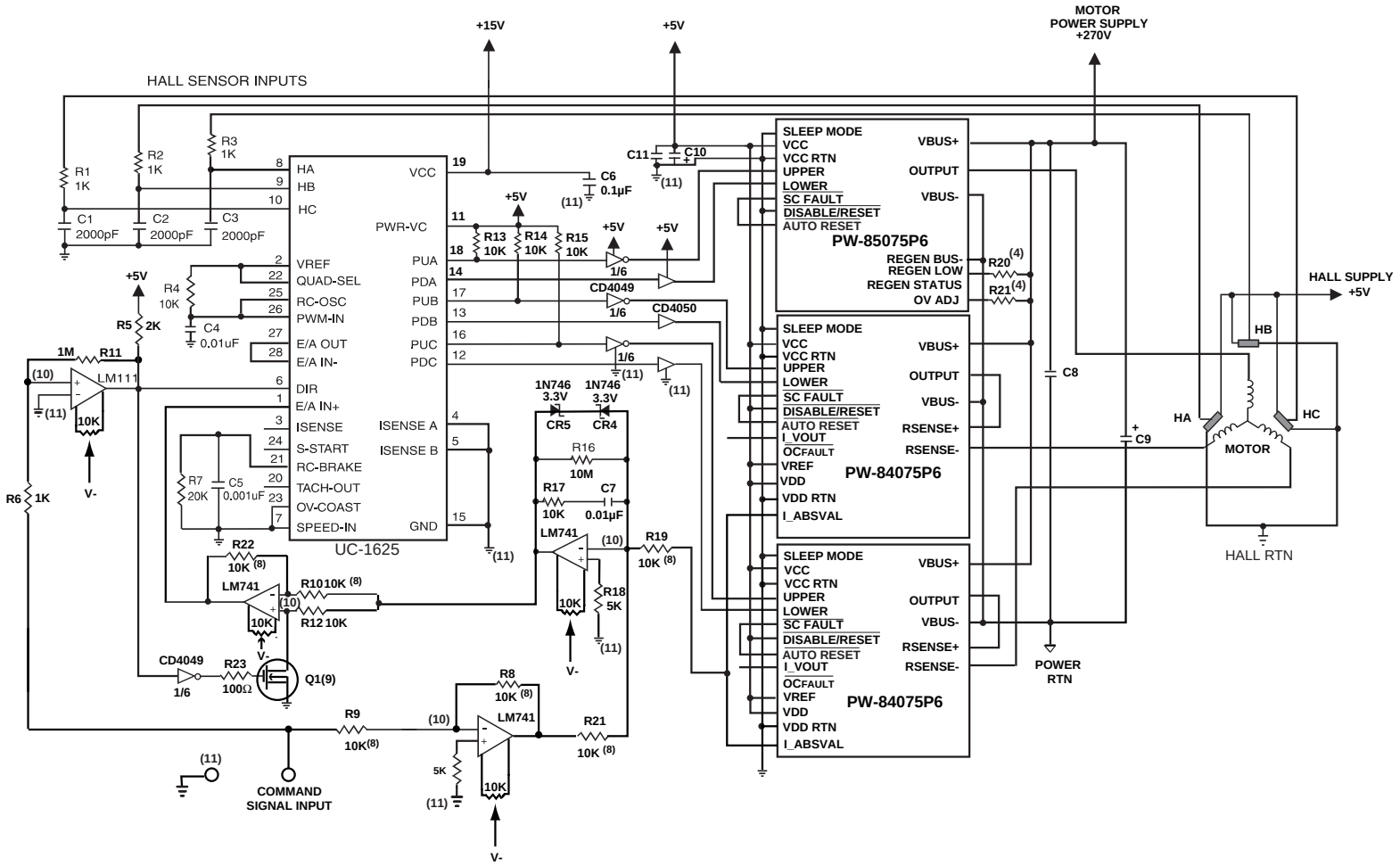
NOTES:
1. Dimensions are in inches (MM).

FIGURE 8. PW-8X075P6 OUTLINE



NOTES:
1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-6, *PW-82351 Motor Drive Power Supply*, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-6, *PW-82351 Motor Drive Power Supply,* equation 1.
3. C10 is 22 µF, 15 V electolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20, R21 is application specific.

FIGURE 9A. PW-8X075P6 POSITION OR VELOCITY HOOK-UP USING DSP MOTOR CONTROLLER



NOTES:

1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-6, *PW-82351 Motor Drive Power Supply*, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-6, *PW-82351 Motor Drive Power Supply,* equation 1.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 and R21 is application specific.
5. All resistors have a tolerance of ±10%, unless otherwise specified.
6. The CD4050 converts the +15V logic output of the UC-1625 to +5V logic signals.
7. The CD4049 (or equivalent) inverts the upper signal from the UC-1625.
8. 1% or better, depending on required accuracy.
9. Q_1 can be either IRML2402 or IRMU014 ir IRLD014.
10. These high impedance inputs and summing junctions of the operational amplifiers are highly sensitive to noise.
11. These grounds should be closely tied together to reduce ground noise effect.

FIGURE 9B. PW-8X075P6 TORQUE HOOK-UP USING UC-1625 MOTOR CONTROLLER

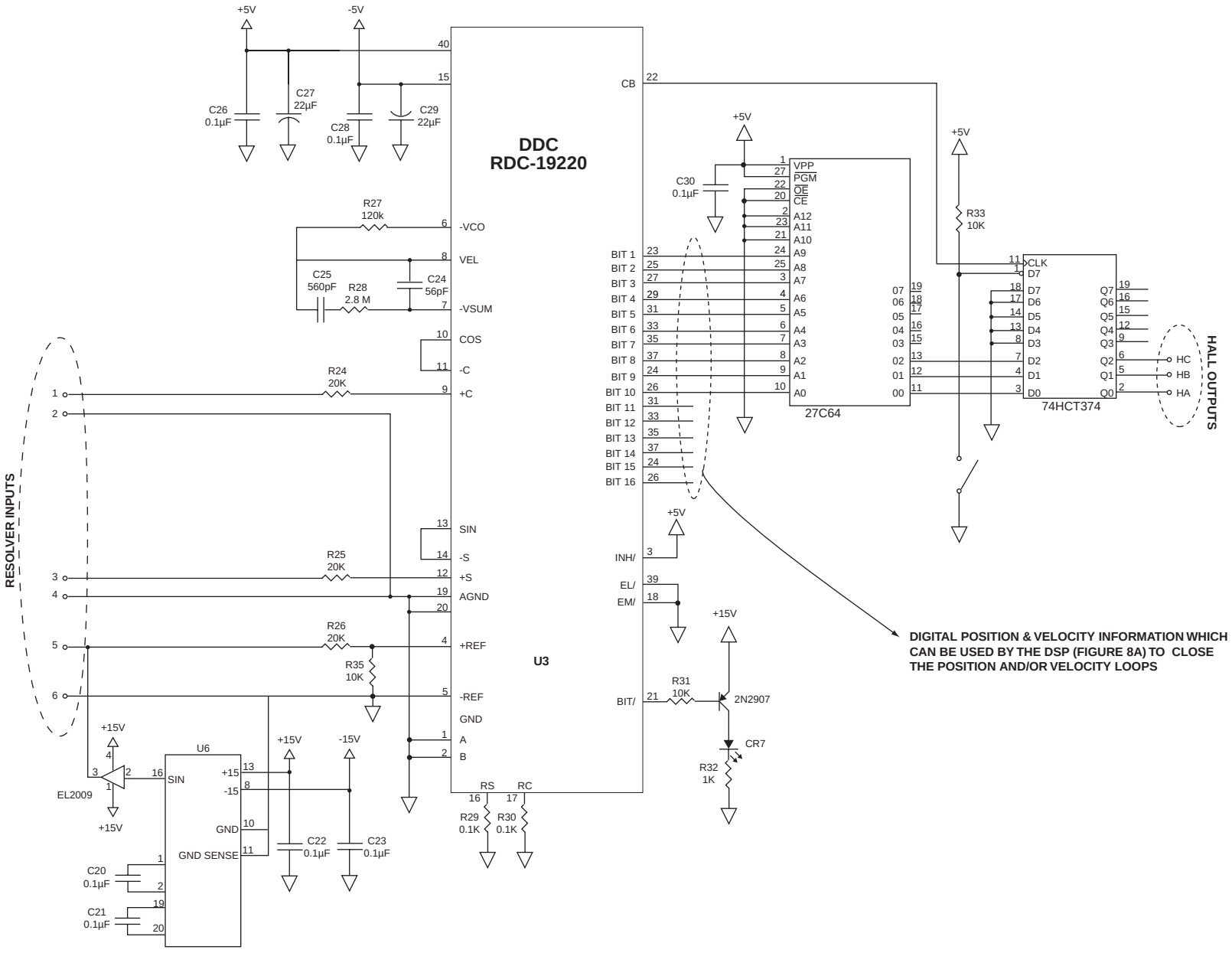


FIGURE 9C. RESOLVER TO HALL SIGNAL CONVERSION CIRCUIT

ORDERING INFORMATION

PW - 8 X 075 PX - X X 0

Process Requirements:
- **0 = Standard DDC Procedures no, Burn-In**
- **2 = High Reliability Processing with Burn-In**

Temperature Grade/Data Requirements:
- **1 = -55°C to +125°C**
- **3 = -0°C to +70°C**
- **4 = -55°C to +125°C with Variables Test Data**
- **8 = 0°C to +70°C with Variables Test Data**
- **9 = -55°C to 85°C**

Voltage Rating
- **6 = 600V**

Current Rating
- **075 = 75A**

Features
- **3 = Standard ½ Bridge**
- **4 = Standard ½ Bridge w/ current sense**
- **5 = Standard ½ Bridge w/ regenerative voltage clamp**

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