Winbond Electronics Corp.

DUAL PCM CODEC

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1. GENERAL DESCRIPTION

The Winbond dual PCM Codec is a 2 channel chip incorporating two ΣΔ PCM codec filter complying with the 64K bps A/Mu law specified in CCITT G.711 standard. In addition, this chip also meets the PCM conformance specification of the CCITT G.714 recommendation.

This chip is operated at 5 volts typically. It consists of some dual OP amplifiers integrated with a ΣΔ PCM codec-filter to allow for easy control of the input/output analog interface. And the device also includes dual serial data port(SDP) to access the digital A/D and D/A data.

2. FEATURES

- Single 5.0 Volt Power Supply
- Master Clock Rate: 2.048 MHz, or 1.536 MHz
- Power Comsumption of 19 mA for 5 Volt; Power Down of 0.2 mA for 5 Volt
- Dual Linear 14 Bits ΣΔ PCM Codec-Filter for A/D and D/A Converters
- Full-duplex 2 Channel Speech Codec
- Complete A/Mu-law Companding or 14 Bit Linear Output
- Meet PCM Conformance Spec. of CCITT G.712/G.714
- 3 Types transfer rate: long frame, short frame and GCI(general circuit interface)
- Serial PCM Transfer Data Rate from 128 to 4096 Kbps for long frame and short frame
- Serial PCM Transfer Data Rate from 512 to 4096 Kbps for GCI frame Interface
- Separate Power Down Mode
- Dual Analog Input OP. Amplifier with External Gain Adjust
- Dual Analog Ouput
  - Single-End Power Driver with 2K Ω Load
  - Differential Power Driver with 300 Ω Load and External Gain Adjust
- 2.7 Volt Regulator for Digital Circuit
- Packaged in 44-pin PQFP

3. PIN CONFIGURATION

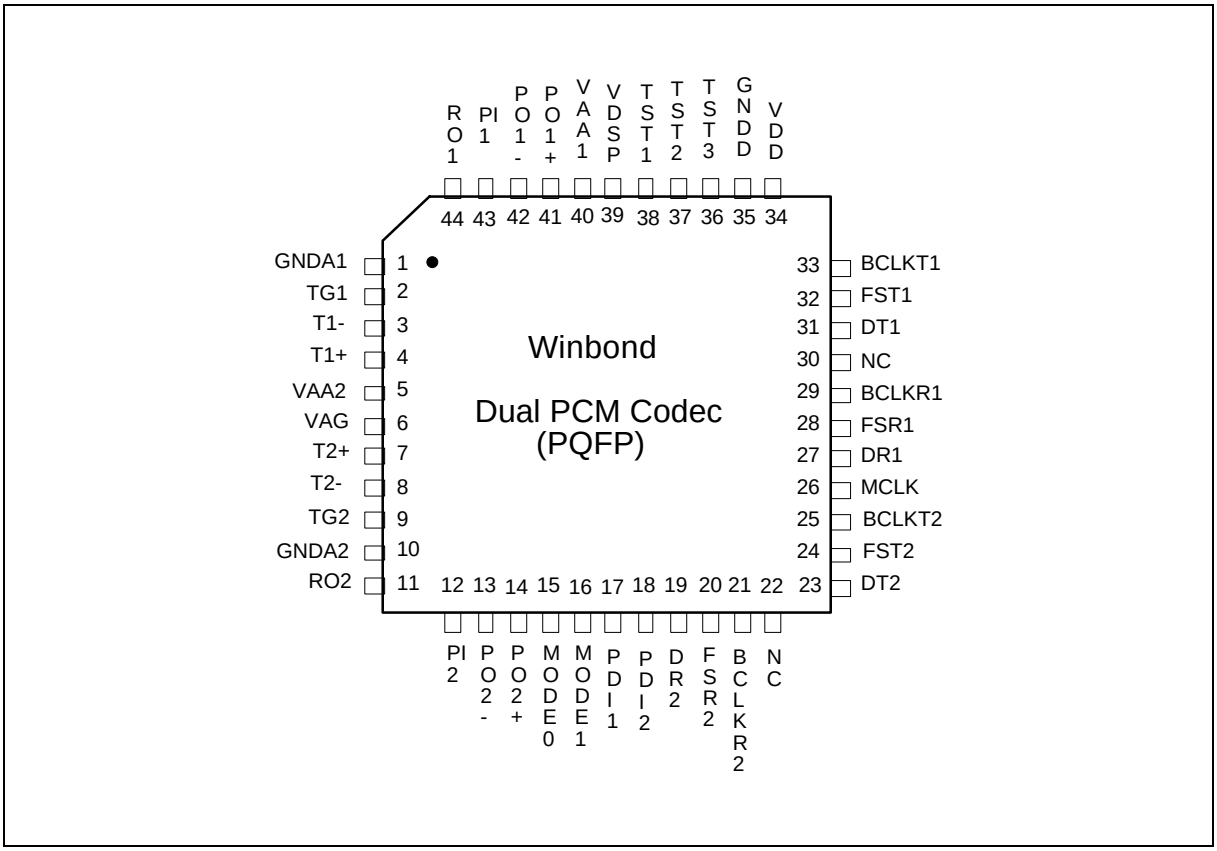

Figure 3-1 Dual PCM Codec Pin Assignment

4. PIN DESCRIPTIONS

4.1. Power Control Interface

PIN NAME	PIN NO.	I/O	FUNCTION
VDD	34	I	This pin is the digital power supply at 5 volt. This pin should be decoupled to GNDD with a 0.1 µF capacitor.
VDSP	39	O	This is the output of the on-chip 2.7 volt regulator which supplies the digital circuit of the chip. This pin should be decoupled to GNDA2 with a 0.1 µF ceramic capacitor. This pin cannot be used for powering external loads.
GNDD	35	I	This pin connects the digital ground and is typically connected to 0 volt.
VAA1	40	I	This pin is the first analog power supply at 5 volt. This pin should be decoupled to GNDA1 with a 0.1 µF capacitor.

4.1. Power Control Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
VAA2	5	I	This pin is the second analog power supply at 5 volt. This pin should be decoupled to GNDA2 with a 0.1 µF capacitor.
GNDA1	1	I	This pin connects the first analog ground and is typically connected to 0 volt.
GNDA2	10	I	This pin connects the second analog ground and is typically connected to 0 volt.
VAG	6	O	This is the analog signal reference ground output pin which supplies a 2.5 volt reference voltage for all analog signal processing. This pin should be decoupled to GNDA1 with 0.1 µF capacitor. This pin becomes high impedance when the chip enters an analog power down mode.

4.2. Analog Interface

PIN NAME	PIN NO.	I/O	FUNCTION
TG1	2	O	This pin is the analog output of the first transmit input amplifier. It can be used to set the gain by external resistors. When the chip is in analog power down mode, this pin is high impedance.
T1-	3	I	This pin is the inverting input of the first transmit input amplifier.
T1+	4	I	The non-inverting input of the first transmit input amplifier. Note this pin may be connected to the VAG pin for an inverting configuration if the input signal is referenced to the VAG pin.
TG2	9	O	This pin is the analog output of the second transmit input amplifier. It can be used to set the gain by external resistors. When the chip is in analog power down mode, this pin is high impedance.
T2-	8	I	This pin is the inverting input of the second transmit input amplifier.
T2+	7	I	The non-inverting input of the second transmit input amplifier. Note this pin may be connected to the VAG pin for an inverting configuration if the input signal is referenced to the VAG pin.
RO1	44	O	This pin is the first non-inverting analog output of the receive smoothing filter. This pin can typically drive a 2K Ω load to 1.579 volt peak referenced to the analog ground level.
PI1	43	I	This pin is the first inverting input to the PO1- power amplifier. It is dc referenced to the VAG pin. This pin and PO1- are used to set the gain by using external resistors.
PO1-	42	O	This pin is the first inverting power amplifier output. This pin can drive the a 300 Ω load to 1.579 volt peak referenced to the VAG pin.

4.2. Analog Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
PO1+	41	O	This pin is the first non-inverting power amplifier output. This pin can drive the a 300 Ω load to 1.579 volt peak referenced to the VAG pin.
RO2	11	O	This pin is the second non-inverting analog output of the receive smoothing filter. This pin can typically drive a 2K Ω load to 1.579 volt peak referenced to the analog ground level.
PI2	12	I	This pin is the second inverting input to the PO1- power amplifier. It is dc referenced to the VAG pin. This pin and PO1- are used to set the gain by using external resistors.
PO2-	13	O	This pin is the second inverting power amplifier output. This pin can drive the a 300 Ω load to 1.579 volt peak referenced to the VAG pin.
PO2+	14	O	This pin is the second non-inverting power amplifier output. This pin can drive the a 300 Ω load to 1.579 volt peak referenced to the VAG pin.

4.3. PCM Serial Interface

PIN NAME	PIN NO.	I/O	FUNCTION
MCLK	26	I	This pin is the system master clock input pin. It is 2.048 MHz or 1.536 MHz. It must be **synchronized with FST1, FST2 pin.**
FST1	32	I	This pin is an 8 KHz pulse for the first transmission of frame syncs. It enables the DT1 PCM output by BCLKT1 pin.
BCLKT1	33	I	This pin is the transmit bit clock. It shifts out the data on the DT1 pin on the rising edge. The frequency may vary from 128K to 4096 KHz.
DT1	31	O	This pin is tri-state PCM output data for transmission controlled by FST1 and BCLKT1 pin.
NC	30	O	No connection for reservation
FSR1	28	I	This pin is an 8 KHz pulse to receive the first frame syncs. It enables the DR1 PCM input by BCLKR1 pin.
BCLKR1	29	I	This pin is the receive bit clock. It shifts data on the DR1 pin into the chip on the falling edge. The frequency varies from 128K to 4096 KHz.
DR1	27	I	This pin is the PCM receive input data controlled by the FSR1 and BCLKR1 pins.
FST2	24	I	This pin is an 8 KHz pulse for the first transmission of frame syncs. It enables the DT1 PCM output by BCLKT1 pin.

4.3. PCM Serial Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
BCLKT2	25	I	This pin is the transmit bit clock. It shifts out the data on the DT1 pin on the rising edge. The frequency may vary from 128K to 4096 KHz.
DT2	23	O	This pin is tri-state PCM output data for transmission controlled by FST1 and BCLKT1 pin.
NC	22	O	No connection for reservation
FSR2	20	I	This pin is an 8K Hz pulse to receive the first frame syncs. It enables the DR1 PCM input by BCLKR1 pin.
BCLKR2	21	I	This pin is the receive bit clock. It shifts data on the DR1 pin into the chip on the falling edge. The frequency varies from 128K to 4096 KHz.
DR2	19	I	This pin is the PCM receive input data controlled by the FSR1 and BCLKR1 pins.
PDI1	17	I	It is power down for Codec 1. When the pin is logic zero, all clocks for codec1 are off and all bias current for codec 1 turn off.
PDI2	18	I	This pin is power down for Codec 2. When the pin is logic zero, all clocks for codec 2 are off and all bias current for codec 2 turn off.
MODE0	15	I	This pin and MODE1 pin can select the PCM output mode including A-law, Mu-law, linear 14 bit PCM.
MODE1	16	I	This pin and MODE0 pin can select the PCM output mode including A-law, Mu-law, linear 14 bit PCM.

4.4. Miscellaneous

PIN NAME	PIN NO.	I/O	FUNCTION
TST1	38	I	This pin is internal pull-high test input pin. It is reserved by test mode.
TST2	37	I	This pin is internal pull-high test input pin. It is reserved by test mode.
TST3	36	I	This pin is internal pull-high test input pin. It is reserved by test mode.

5. BLOCK DIAGRAM

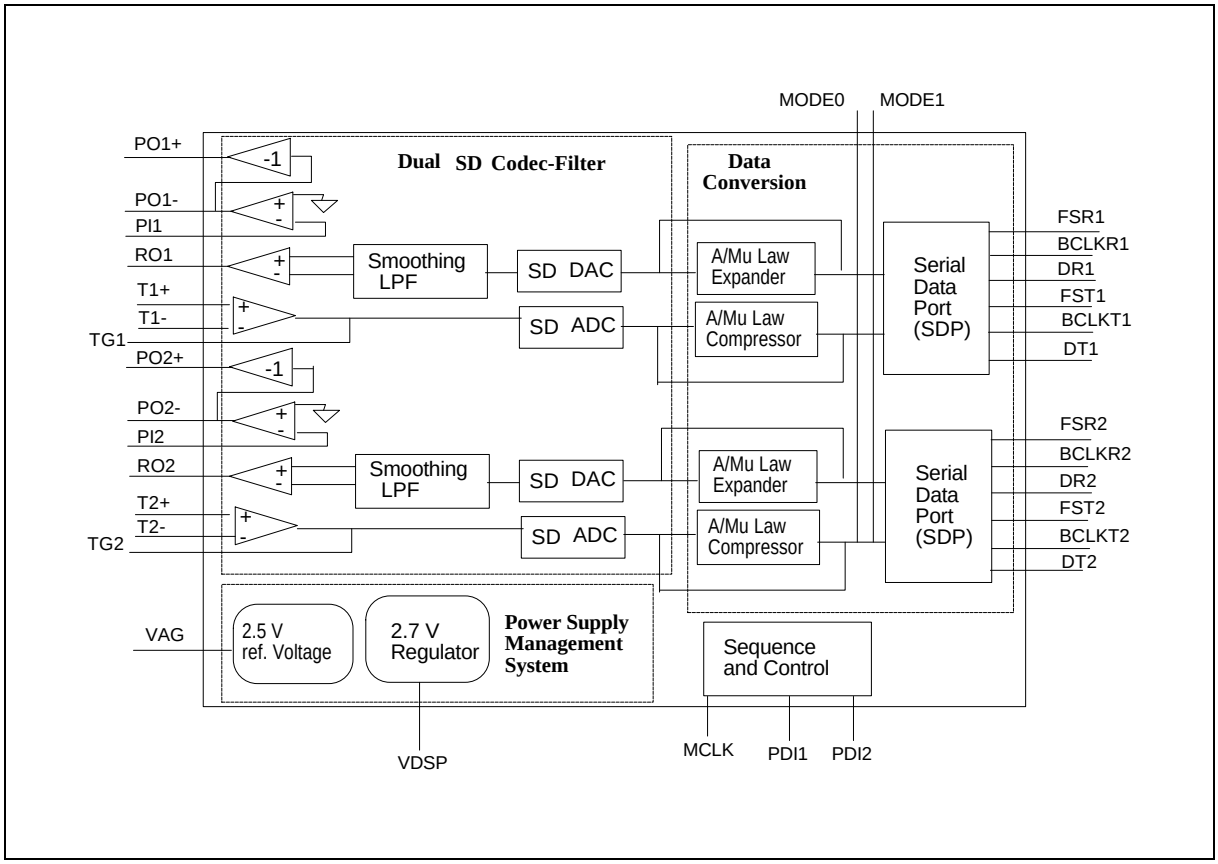

Figure 5. Winbond Dual PCM ΣΔ Codec Block Diagram

6. FUNCTIONAL DESCRIPTIONS

Figure 5 illustrates the functional blocks of the Winbond Dual PCM ΣΔ codec.

6.1. Power Supply Management System

6.1.1. Power Supply for All Analog Signals Processing

All analog circuits are supplied with VAA1 and VAA2, two 5±5% volt power supply. VAA1 power provides the first ΣΔ codec-filter and OP amplifier; the VAA2 power provides the second ΣΔ codec-filter and OP. amplifier.

6.1.2. Power Supply for All Digital Signals Processing

All digital circuits are supplied by the V_{DSP} pin from a 2.7-volt regulator circuit. This reduces the chip power consumption. Note that the V_{DSP} pin should be decoupled to GNDA with a 0.1 µF capacitor and that this pin cannot be used for powering external loads.

6.1.3. Reference Voltage Control System

All analog signal reference voltages such as OP amplifier is 2.5 volt.

6.2. SD Codec-filter

This device has built in dual linear 14-bit PCM codec-filter using ΣΔ technology. There are two paths in the block, a transmit path and a receive path.

6.2.1. Transmit Path in ΣΔ Codec-filter

The two analog signal inputs are passed to three terminal operational amplifiers (TG1, TG2) driving a typical 2 KΩ load externally to amplify the input analog signal. Then the ΣΔ ADC converts the analog signal into linear 14-bit data.

6.2.2. Receive Path in ΣΔ Codec-filter

Dual 14-bit linear digital signal from the digital conversion circuit is first passed to the ΣΔ DAC block. It will convert the 14-bit samples to the analog signal. Then the analog signal will reduce the spectral components of the switched capacitor filter by the analog smoothing filter. Finally, the analog output signal is sent to the power amplifier, RO1 or RO2, which is capable of driving a 2K Ω load connected to to the analog ground.

Note the device provides another power amplifier, PO1 or PO2, connected in a push-pull configuration. The PO1 or PO2 driver can accommodate large gain ranges by adjusting two external resistors for applications such as driving a telephone line or a handset receiver.

6.3. Data Conversion

This block is the digital data convsersion circuit. There are two paths in this block, a transmit path and a receive path.

6.3.1. Transmit Path in the Data Conversion

A linear 14 bit sample input from the transmit path of the ΣΔ Codec-filter block is sent in two processing directions: A/Mu law compressor, and Linear conversion selected by MODE1 and MODE0 pin. The mode selection refers to Table 6-1. In the A/Mu law compressor, the 14 bit linear data will converted into 8-bit Log-PCM. In the Linear conversion, the 14-bit data will be sent into serial data port directly. The final result outputs the PCM signal through pin DT1 or DT2 under the control of the FST1 or FST2 (8K frame sync pulse) and BCLKT1 or BCLKT2 pins. The data output rate for BCLKT1 or BCLKT2 is from 128K to 4096 KHz.

MODE SELECTION	MODE1 PIN	MODE0 PIN
A-Law Compressor/Expander	0	0
Mu-Law Compressor/Expander	0	1
14-bit Linear Input/Output	1	0
14-bit Linear Input/Output	1	1

Table 6-1 The Mode Selection for the Data Conversion

6.3.2. Receive Path in the Data Conversion

The device receives PCM data from the DR1 or DR2 pin via the serial data port (SDP) under the control of the BCLKR1 or BCLKR2 and FSR1 or FSR2 pins. The clock of the receive frame sync FSR is 8 KHz. The serial data rate in the BCLKR1 or BCLKR2 is from 128 KHz to 4096 KHz range.

The received PCM will be processed by two paths depended by the mode selection, see Table 6-1. One path converts the 8-bit Log-PCM into 14 bit linear PCM via A/Mu Law expander. The other one is sent 14 bit linear PCM directly. The finial 14-bit linear is sent into ΣΔ codec filter to convert into the analog signal.

6.3.3. Frame Sync. Types

The frame sync operation uses three industrial control types for the transfer of the PCM data words. These three types are the long frame sync , short frame sync and GCI frame sync.

6.3.3.1. Long Frame Sync

The long frame sync types for various data rates are shown in Figure 6-1 and 6-2. The bit rate for the PCM is determined by the mode selection MODE1, MODE0 pin, shown in Table 6-1. The length of the frame sync is calculated by the number of falling edges at the BCLKT1, BCLKT2 or BCLKR1, BCLKR2 pin when the frame sync FST1, FST2 or FSR1, FSR2 pin is high.When the frame sync is **held logic one for two consecutive falling edges of the BCLKT1/2(BCLKR1/2)**, the device is in long frame sync mode. The device shifts out the data on the DT1 or DT2 pin at the BCLKT1 or BCLKT2 rising edge and shifts in the data on the DR1 or DR2 pin at the BCLKR1 or BCLKR2 falling edge. The PCM data remain low impedence until seven and a half data clock cycles for 64K bps **if frame sync cycle is less than eight data clcok** and thirteen and a half data clock cycles for 112 Kbps **if frame sync cycles is less than fourteen data clcok**. After the data transmission, the DT1(DT2) outputs will return to high impedence state. The length of the frame sync may be changed on a frame by frame basis.

6.3.3.2. Short Frame Sync

The short frame sync types for 64 Kbps or 112 kbps PCM, controlled by the MODE1, MODE0 pin. The timing is shown in Figure 6-3 and 6-4. The length of the frame sync is equal to 1. The device shifts out data on the DT1 or DT2 pin at the BCLKT1 or BCLKT2 rising edge and shifts in data on the DR1 or DR2 pin at the BCLKR1 or BCLKR2 falling edge. The DT1(DT2) pin is going low impedance when the logic AND of the FST1(FST2) pin and BCLKT1(BCLKT2) pin is the rising edge in the first. The PCM data remain low impedence until seven and a half data clock cycles for 64 Kbps and thirteen and a half data clock cycles for 112 k bps. After the data transmission, the DT1(DT2) outputs will return to high impedence state. Switching between long frame sync and short frame sync without going through a power down operation is not recommended.

6.3.3.3. GCI(General Circuit Interface) Frame Sync

The GCI frame sync is for two B channels access interface in ISDN application. The type is selected by **BCLKR1** pin when the BCLKR1 pin is held low. This interface is only suitable for 8-bit Log-PCM data, not 14-bit linear PCM data. The timing is shown in Figure 6-5. The timing is controlled by 4 pins, FSC(FST1), DCL(BCLKT1), Dout(DT1), and Din(DR1). The pulse length of the frame sync(FSC) is equal to 1 clock of DCL(BCLKT1). The DCL(BCLKT1) clcok rate is twice the actual PCM data rate. The PCM data for Dout(DT1) or Din(DR1) is two 8-bit B channel data, i.e., 16 DCL(BCLKT1) clcok rate. The previous 8 bit data is for Codec1 , and the left 8 bit data is for Codec 2. The Dout pin is going low impedance when the logic AND of the FSC pin and DCL pin is high and remains the low impedance for 15 and 1/2 DCL cycles. Note if the codec 1 enters the power down, the control timing is switched to the Codec 2, FSC(FST2), DCL(BCLKT2), Dout(DT2), and Din(DR2). Meanwhile, the output of Codec 1 part becomes the high impedance. If the Codec 2 is power down, the output of Codec 2 part becomes the high impedance.

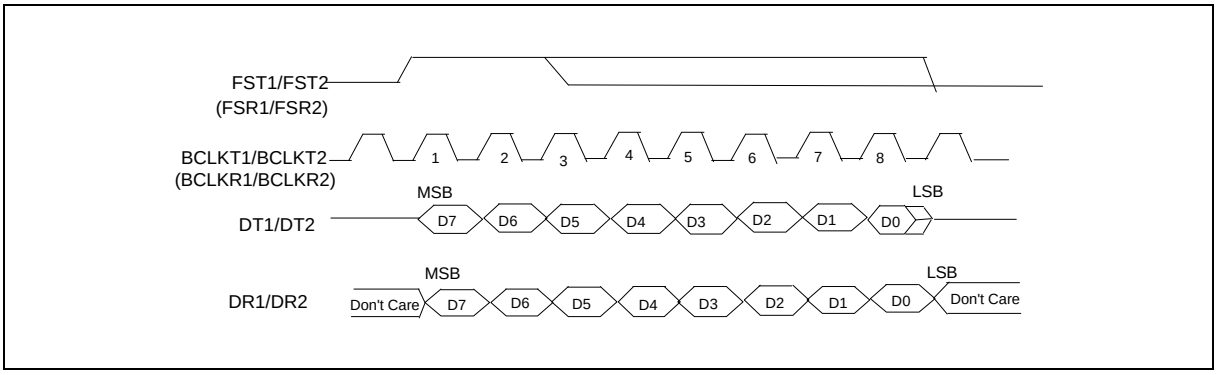

Figure 6-1 Long Frame Sync for 64 Kbps PCM Timing

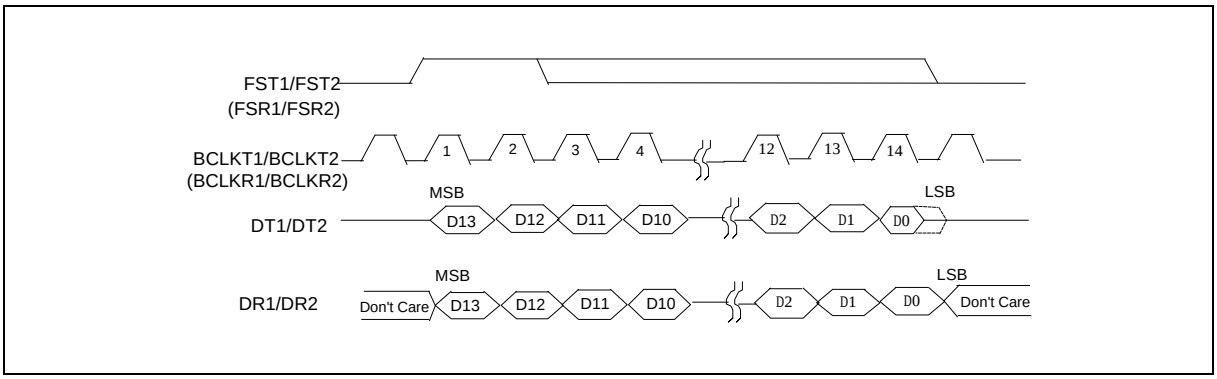

Figure 6-2 Long Frame Sync for 112 Kbps PCM Timing

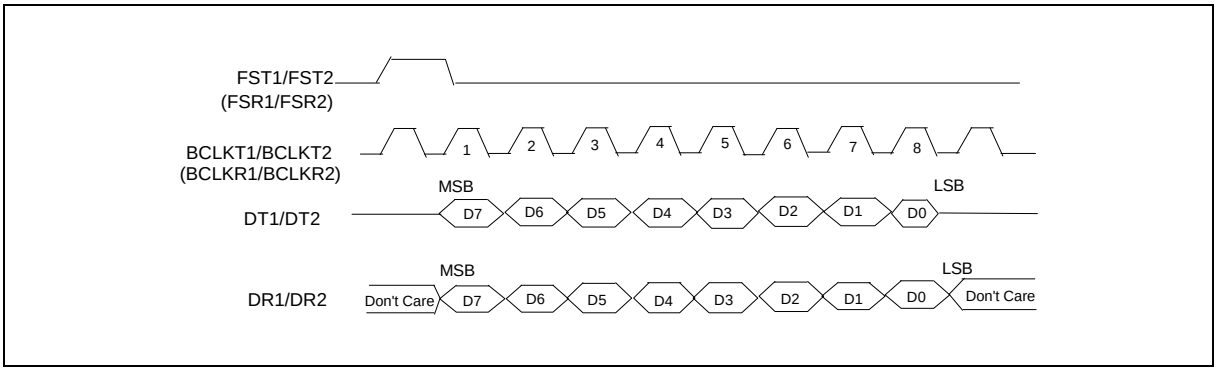

Figure 6-3 Short Frame Sync for 64 Kbps PCM Timing

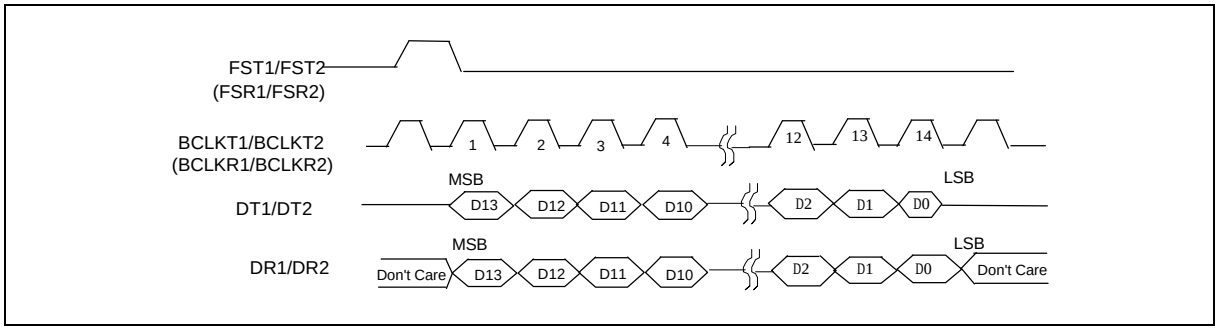

Figure 6-4 Short Frame Sync for 112 Kbps PCM Timing

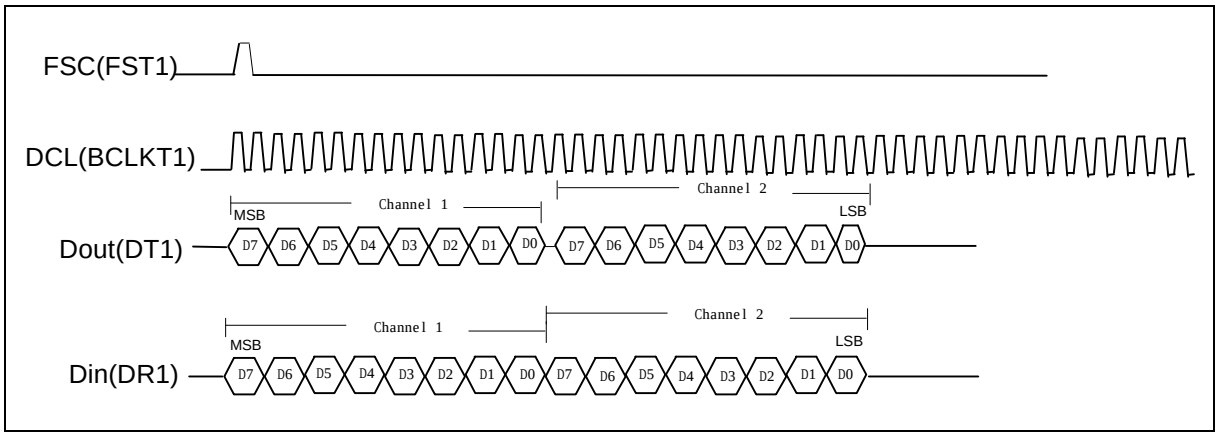

Figure 6-5 GCI Frame Sync for 128 Kbps PCM Timing

6.4. Sequence and Control

This block generates some internal clocks, providing clocks for ΣΔ codec-filter operation. The master clock MCLK pin, which supports the clock of the digital circuit, may be asynchronous to all other blocks but synchronous to FST1 and FST2 frame sync pulse, 8 KHz. Its frequency is 2.048 MHz or 1.536 MHz. As for jitter tolerence of MCLK pin, it is **146.5 nS for 2.048 MHz; but 260 nS for 1.536 MHz**. In addition, the duty cycle of MCLK pin must be **50**%

The rising edge of MCLK pin must be approximately aligned with the rising edge of the FST1 or FST2 pin depent on whether the codec of device is power down. If the device does not enter the power down mode, **the master clock is refered to FST1 in default**. If the codec1 is power down, the master clock is refered to FST2 pin. The device will automatically detect the clock rate of MCLK pin by a prescaler circuit for MCLK and FST1 (or FST2).

When the Codec is start-up initially such as power-on reset or power-up after power-down, the steady codec output data will be delay by about 60 samples.

When the PDI1 pin is held to logic 0, the codec 1 will become the hardware power down. The VAG, TG1, RO1, PO1, DT1 outputs enter high impedance. When the PDI2 pin is held to logic 0, the codec 2 will become the hardware power down. The TG2, RO2, PO2, DT2 outputs are all high impedance. If the device is **GCI mode**, the channel can be powered down separatedly by PDI1 or PDI2 pin. The device is built-in **power-on reset circuit in default**.

6.5. I/O Level

Digital I/O for the device can be programmed in either Mu-law or A-law for Log-PCM mode. Full scale and zero words for these two Log-PCM forms are shown in Table 6-2. For analog signal processing, the maximum transmit level is 3.17 dBm0 for Mu-Law or 3.14 dBm0 for A-Law. These values meet the CCITT G.711specifications.

	MU-LAW			A-LAW		
Level	Sign	Segment Bits	Step Bits	Sign	Segment Bits	Step Bits
+ max. scale	1	000	0000	1	010	1010
+Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- max. scale	0	000	0000	0	010	1010

Table 6-2 Full Scale and Zero Word for Mu/A-Law

7. ELECTRICAL CHARACTERISTICS

7.1. Absolute Maximum Ratings

(Voltage Referenced to GNDA1, GNDA2, and GNDD pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	VAA1, VAA2, V_{DD}	-0.3 to 6.0	V
Analog Input/Output Voltage	---	-0.3 to VAA1(VAA2) + 0.3	V
Digital Input/Output Voltage	---	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STG}	-85 to +85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2. DC Characteristics

(GNDA1 = GNDA2 = GNDD = 0 volt ; T_{OP} = -40 to +85° C)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	VDD, VAA1, VAA2	----	4.75	5.0	5.25	V
Operating Current	Iop	MCLK = 2.048 MHz, no load (VAA1 = VAA2 = 5V)	---	19	--	mA
Power Down Current	I_{PWDN}	MCLK/PDI Off, no load	---	---	0.3	mA
Input High Voltage	V_{IH}	All digital input pins	V_{DD} -0.5	---	-----	V
Input Low Voltage	V_{IL}	All digital input pins	0	----	0.5	V
Output High Voltage	V_{OH}	DT1, DT2	V_{DD} -0.5	----	-----	V
Output Low Voltage	V_{OL}	DT1, DT2	0	---	0.4	V
Input High Current	I_{IL}	GNDD≤ Vin ≤ V_{DD}	-10	---	+10	µA
Input Low Current	I_{IH}	GNDD≤ Vin ≤ V_{DD}	-10	---	+10	µA

7.3. Analog Transmission Characteristics

(VAA1 = VAA2 = +5V ±5%, GNDA1 = GNDA2 = 0 volt , Top = -40 to +85° C ; all analog signal referenced to VAG; 64 Kbps Log-PCM; FST1(FST2) = FSR1(FSR2) = 8 KHz; BCLKT1(BCLKT2) = BCLKR1(BCLKR2) = 2.048 MHz; MCLK = 2.048 MHz synchronous with FST1(FST2) ; Unless otherwise noted)

7.3.1. Amplitude Response for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	LABS	0 dBm0 = +0 dBm @ 600 Ω	1.096	---	---	---	---	Vpk
Max. Transmit Level	TXMAX	3.17 dBm0 for Mu-Law	1.579	---	---	---	---	Vpk
		3.14 dBm0 for A-Law	1.573	---	---	---	---	Vpk
Frequency Response, Relative to 0 dBm0 @ 1020Hz	GRTV	15 Hz	----	----	-40	-0.5	0	dB
		50 Hz	----	---	-30	-0.5	0	
		60 Hz	---	---	-26	-0.5	0	
		200 Hz	---	-1.0	-04	-0.5	0	
		300 to 3000 Hz	---	-0.20	+0.15	-0.20	+0.15	
		3300 Hz	---	-0.35	+0.15	-0.35	+0.15	
		3400 Hz	---	-0.8	0	-0.8	0	
		4000 Hz	---	---	-14	---	-14	
		4600 to 100, 000 Hz	---	---	-32	---	-30	
Gain Variation vs. Level Tone (1020 Hz relative to -10 dBm0)	GLT	+3 to -40 dBm0	---	-0.3	+0.3	-0.2	+0.2	dB
		-40 to -50 dBm0	---	-1.0	+1.0	-0.4	+0.4	
		-50 to -55 dBm0	---	-1.6	+1.6	-0.8	+0.8	

7.3.2. Distortion Characteristics for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Group Delay	DABS	1600 Hz	---	---	440	---	---	µS
Total Distortion vs. Level Tone (1020 Hz, Mu-Law, C-Message)	DLT	+3 dBm0	---	36	---	34	---	dBC
		0 to -30 dBm0	---	36	---	36	---	
		-40 dBm0	---	29	---	30	---	
		-45 dBm0	---	25	---	25	---	

7.3.3. Noise Characteristic for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Idle Channel with Equipment Noise	NIDE	Mu-Law, C-Message	---	---	+5	---	+13	dBrn
Spurious Out-of-Band at SPKO (300 to 3400 Hz @ 0 dBm0)	NSPO	4600 to 7600 Hz 7600 to 8400 Hz 8400 to 100,000 Hz	--- --- ---	--- --- ---	--- --- ---	--- --- ---	-30 -40 -30	dB
In-Band Spurious (1020 Hz @ 0 dBm0)	NIBS	300 to 3000 Hz	---	---	-47	---	-47	dB
Crosstalk (1020 Hz @ 0 dBm0)	NCTK	300 to 3000 Hz	---	---	-70	---	-70	dB

7.4. Analog Electrical Characteristics

(OP Amplifer TG1, TG2, RO1, RO2; Power Amplifer PO1, PO2; VAA1 = VAA2 = +5V ±5%, GNDA1 = GNDA2 = 0V; Top = -40 to +85° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset voltage of TG1, TG2	VOFIN	T1+, T1-, T2+, T2-	---	---	±25	mV
Load Capacitance for RO1, RO2	CLRO	RO1, RO2	---	---	100	pF
Load Resistance for RO1,RO2	RLDRO	RO1, RO2	2	---	---	KΩ
Load Resistance for TG1,TG2	RLDTG	TG1, TG2	2	---	---	KΩ
VAG Output Voltage	VAG	to GNDA1, GNDA2	2.3	2.5	2.6	V
Power Supply Rejection Ratio (0 to 100 KHz @ 100m Vrms to VAA1(VAA2) with C-Message)	PSRRdd	TG1, TG2	---	40	---	dBC
Load Capacitance for PO1, PO2	Clpo	PO- to PO+	---	----	150	pF
Load Resistance differentially for PO1, PO2	Rldpo	PO- to PO+	300	---	----	Ω
Input Offset Voltage for PI	Vofpi	ref to VAG	---	----	±25	mV

7.5. Digital Switching Characteristics

7.5.1 Long frame and short frame sync timing

(V_{DD} = 5 ±5% V; GNDD = 0V; all digital circuits referenced to GNDD; Top = -40 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Master Clock Frequency	TMAST	MCLK	----	2.048 1.536	----	MHz MHz
Bit Clock Frequency	TBCLK	BCLKT1, BCLKT2, BCLKR1, BCLKR2	128	---	4096	KHz
Frame Sync. Frequency	TSYNC	FST1, FST2, FSR1, FSR2	---	8	- -	KHz
Clock Duty Cycle	DC	MCLK, BCLKT1, BCLKT2, BCLKR1, BCLKR2	---	50	---	%
Rise Time	TIR	All digital input pins	---	---	50	nS
Fall Time	TIF	All digital input pins	---	---	50	nS
Hold Time for 2nd cycle of BCLKT1/2(BCLKR1/2)	THLD	BCLKT1/2(BCLKR1/2) Low to FST1/2(FSR1/2) Low	50	---	---	nS
Transmit Sync. Timing	TXS TSX	BCLKT1/2 to FST1/2 FST1/2 to BCLKT1/2	20 80	--- ---	--- ---	nS
Receive Sync. Timing	TRS TSR	BCLKR1/2 to FSR1/2 FSR1/2 to BCLKR1/2	20 80	--- ---	--- ---	nS
Setup Time for DR1(DR2) Valid	TSTDR	---	20	---	---	nS
Hold Time for DR1(DR2) Valid	THDDR	---	50	---	---	nS
Output Delay Time for 1st DT1(DT2) Valid	TDV1	BCLKT1/2 to DT1/2	10	---	120	nS
Output Delay Time for 2nd DT1(DT2) Valid	TDV2	BCLKT1/2 to DT1/2	10	---	120	nS
Output Delay Time for DT1(DT2) High Impedance	TDHI	BCLKT1/2 to DT1/2	10	---	120	nS

Note: these parameters are shown in Figure 7-1 and 7-2.

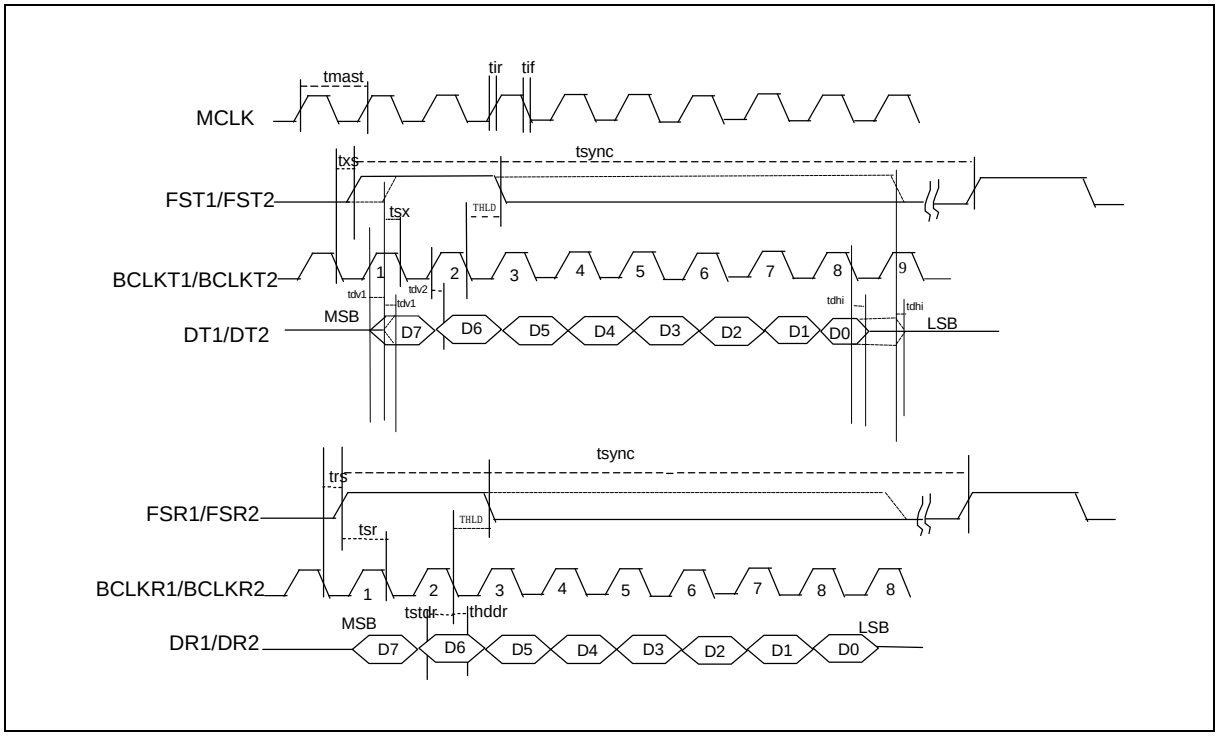

Figure 7-1 Long Frame Sync Timing

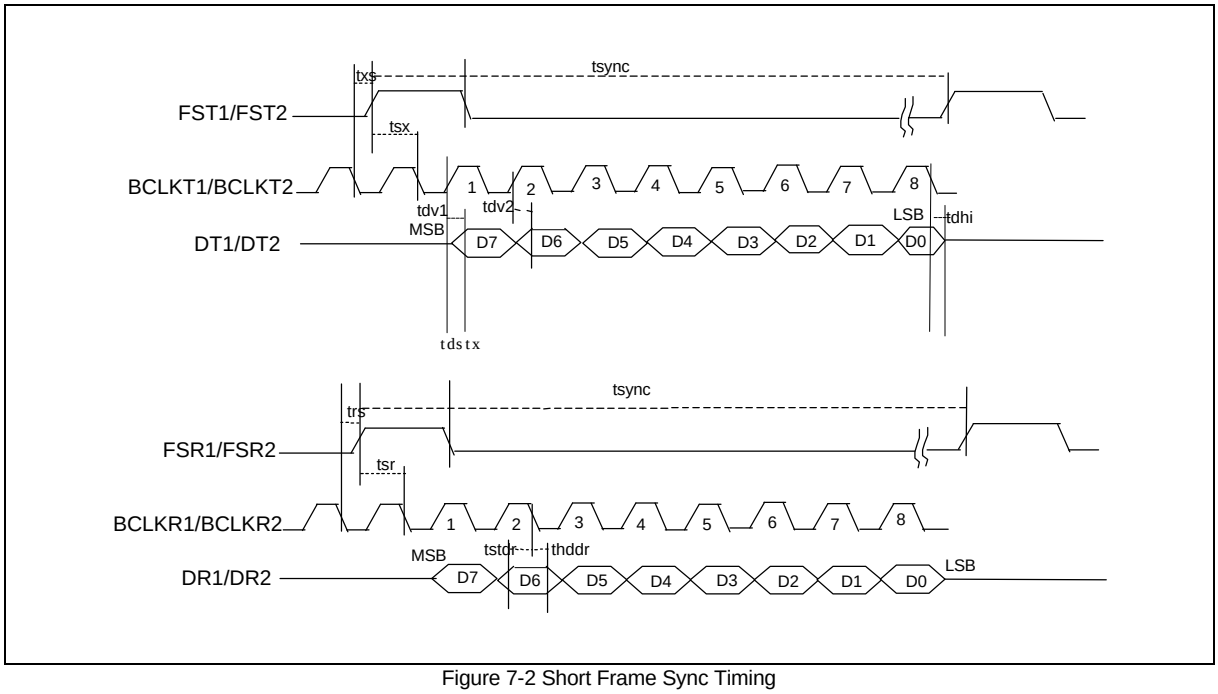

Figure 7-2 Short Frame Sync Timing

7.5.2 GCI frame sync timing

(V_{DD} = 5 ±5% V; GNDD = 0V; all digital circuits referenced to GNDD; Top = -40 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bit Clock Frequency	T_{DCL}	DCL (BCLKT1)	**512**	---	**4096**	KHz
Frame Sync. Frequency	T_{FSC}	FSC(FST1)	---	**8**	- -	KHz
Setup Time for Din(DR1) Valid	T_{STDIN}	---	20	---	---	nS
Hold Time for Din(DR1) Valid	T_{HDDIN}	---	50	---	---	nS
Output Delay Time for Dout(DT1) Valid	T_{DV}	DCL to Dout	10	---	60	nS
Output Delay Time for Dout(DT1) High Impedance	T_{DHI}	DCL to Dout	10	---	60	nS

Note: these parameters are shown in Figure 7-3

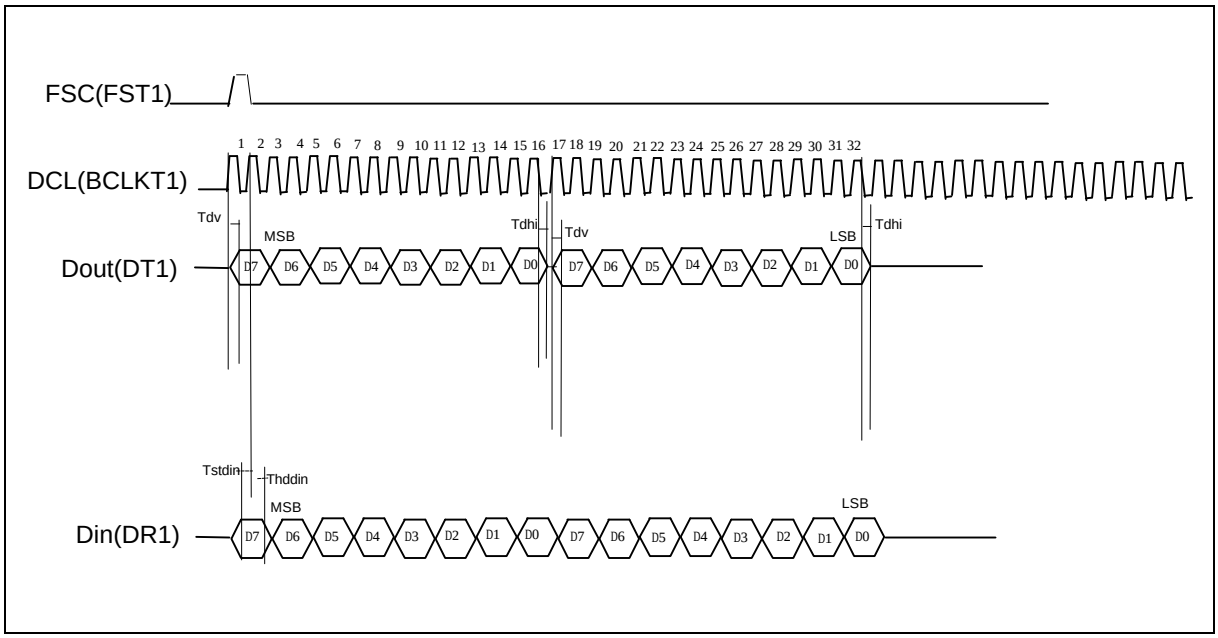

Figure 7-3 GCI Frame Sync Timing

8. APPLICATION INFORMATION

For the transformer application, VAA1 = VAA2 = V_{DD} = +5V ±5%

The application circuit, Figure 8-1 is as follows.

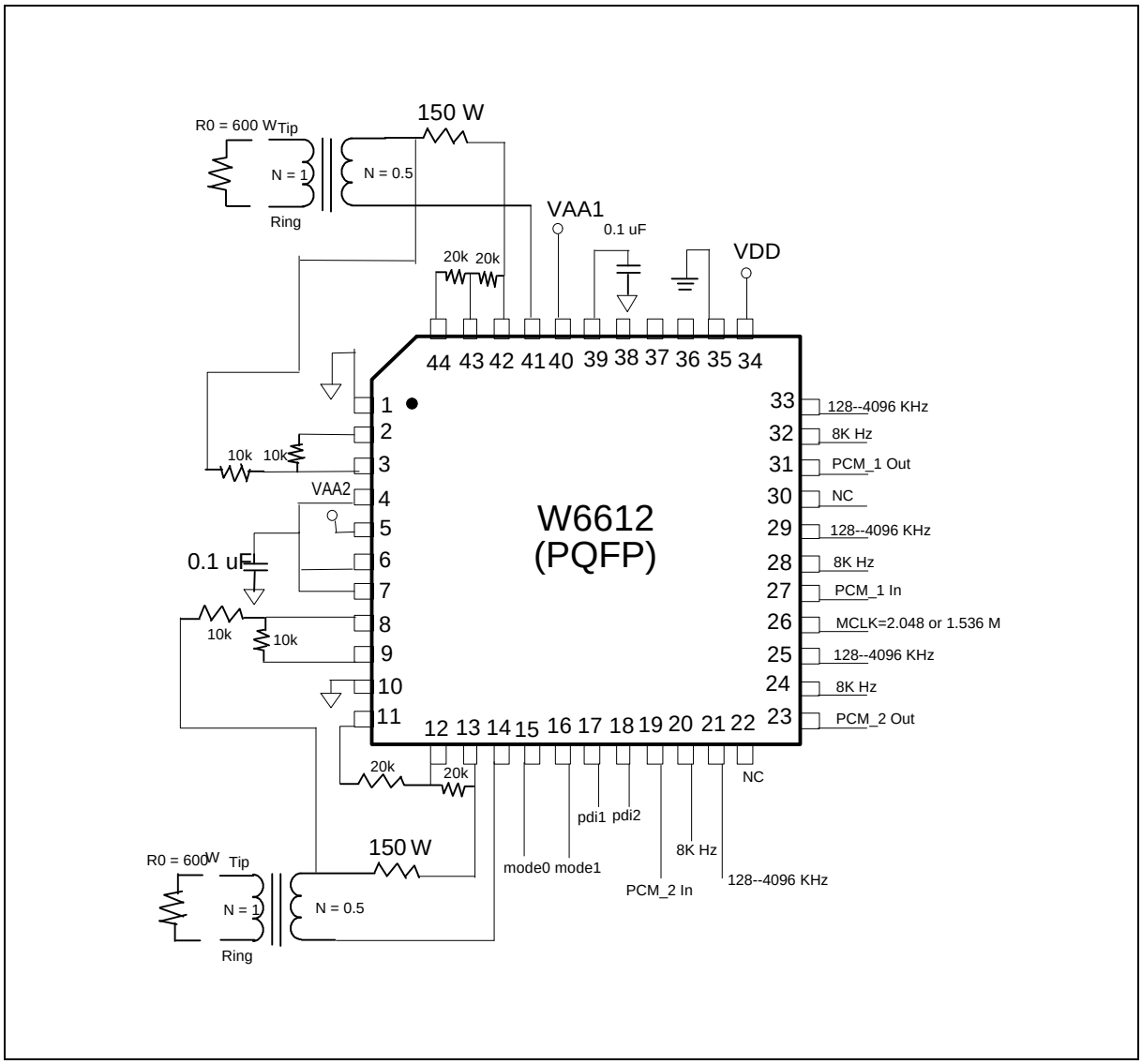

Figure 8-1 Typical Transformer Application

For the SLIC(subsciber Line Interface Circuit) application, VAA1 = VAA2 = V_{DD} = +5V ±5%

The application circuit, Figure 8-2 is as follows.

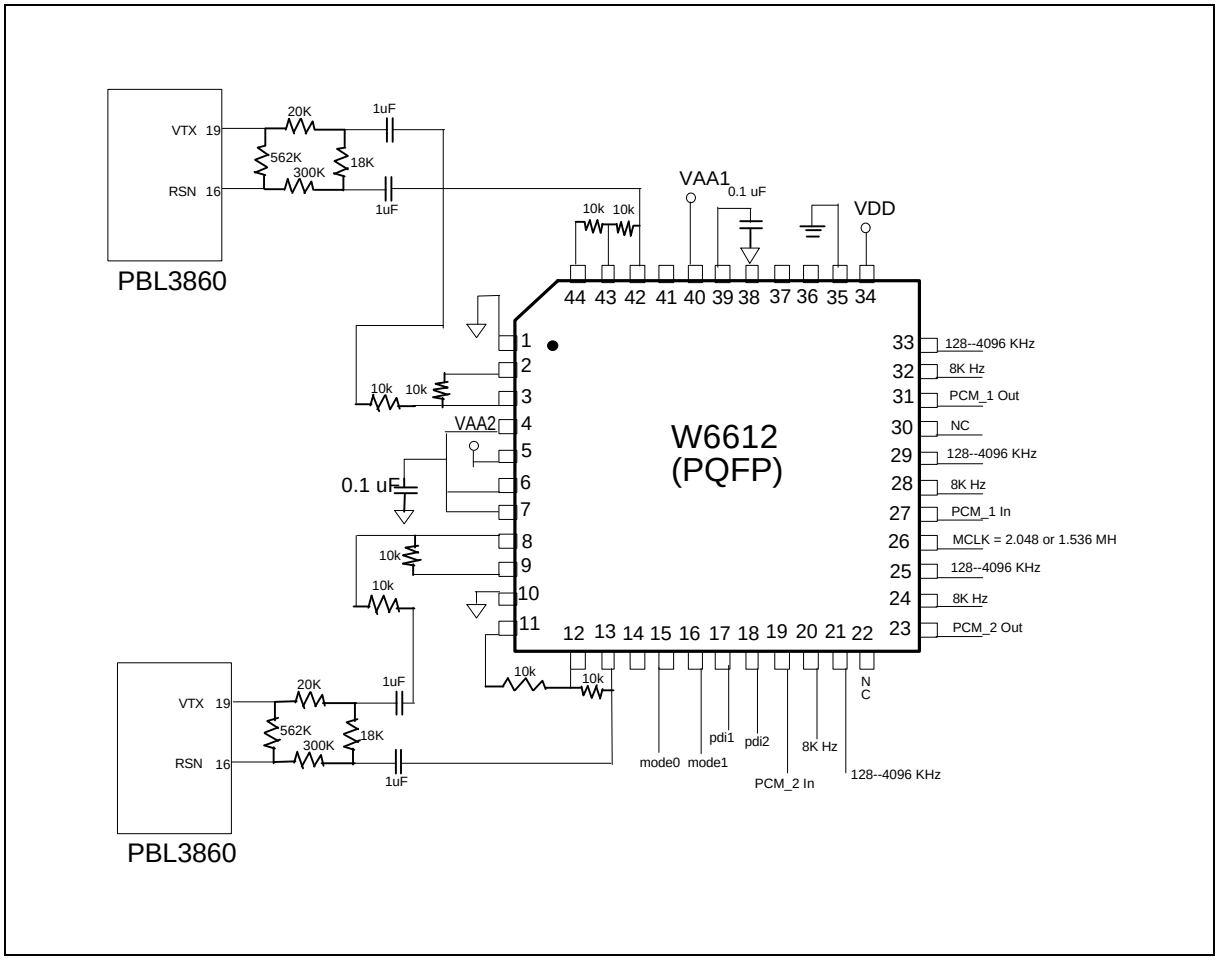

Figure 8-2 Typical SLIC Application

9. PACKAGE DIMENSIONS

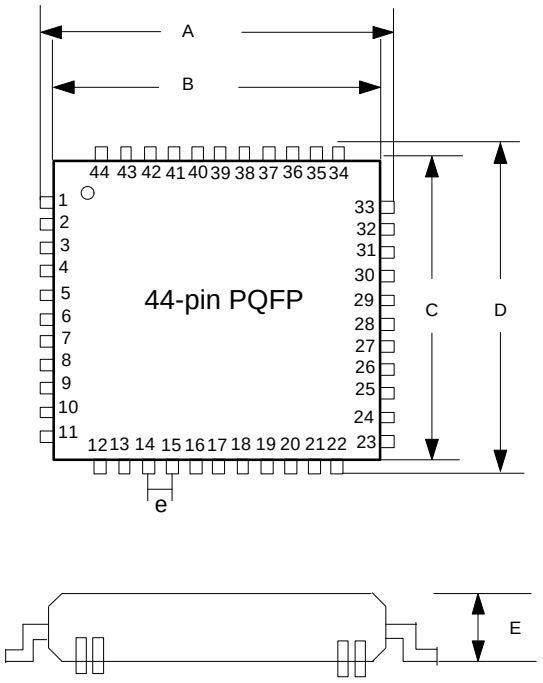

Figure9-1 44-Lead PLCC Package

SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.52	13.2
B	0.394	10.0
C	0.394	10.0
D	0.52	13.2
e	0.031	0.8
E	0.091	2.3

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