# Dual Serial Input PLL with 2.0 and 1.1 GHz Prescalers

## Features

- IC WORKS BiCMOS process
- Operating voltage 2.7V to 5.5V
- Operating frequency to 2.0GHz on PLL1 and 1.1 GHz on PLL2 with inputs of –15dBm and Vcc of 3.0V
- Lock detect feature
- Power-down mode Icc < 1µA typical at 3.0V
- Serial data input accepts data clock rates as low as 1KHz
- Low power/voltage operation with low current standby mode
- On chip reference oscillator
- Available in a 20-pin TSSOP (Thin Shrink Small Outline Package)

## Applications

The IC WORKS WB1336 is a dual serial input PLL frequency synthesizer designed for high performance dual conversion TV, VCR, and Set-top tuner sections, as well as downstream receivers for cable modems. The WB1336 is also well suited for high volume, low cost wireless communications applications. One 2.0GHz and 1.1GHz prescaler, each with pulse swallow capability are included. The device operates from 2.7V and dissipates only 38mW.

**Figure 1 Pin Diagram**

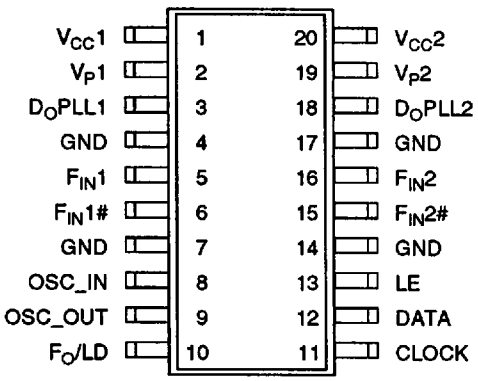



**Table 1 Order Information: WB1336TX-TR**

| Part Number | Part Revision | Package | TR |
|---|---|---|---|
| WB1336 | T | X = TSSOP (0.173" Wide) | Tape & Reel Option |

**Note:** Operating temperature range: –40°C to +85°C.

**Figure 2 Dual PLL Block Diagram**

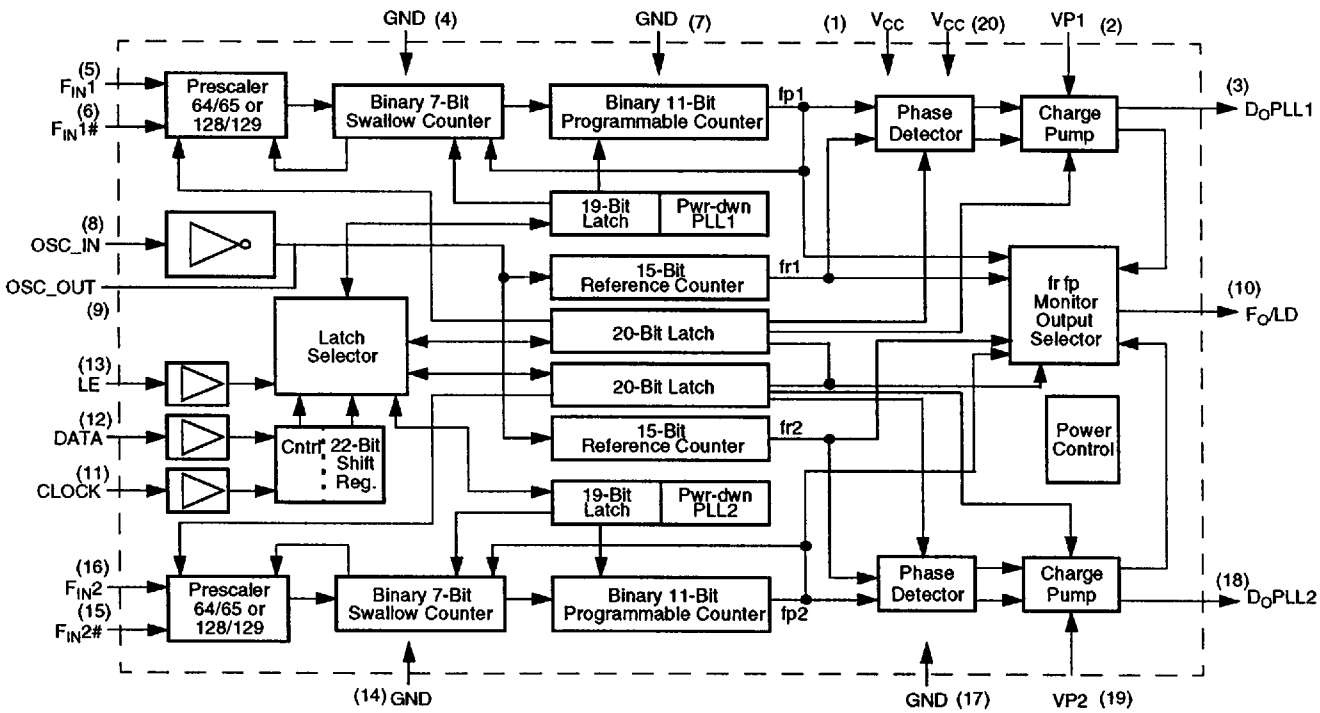
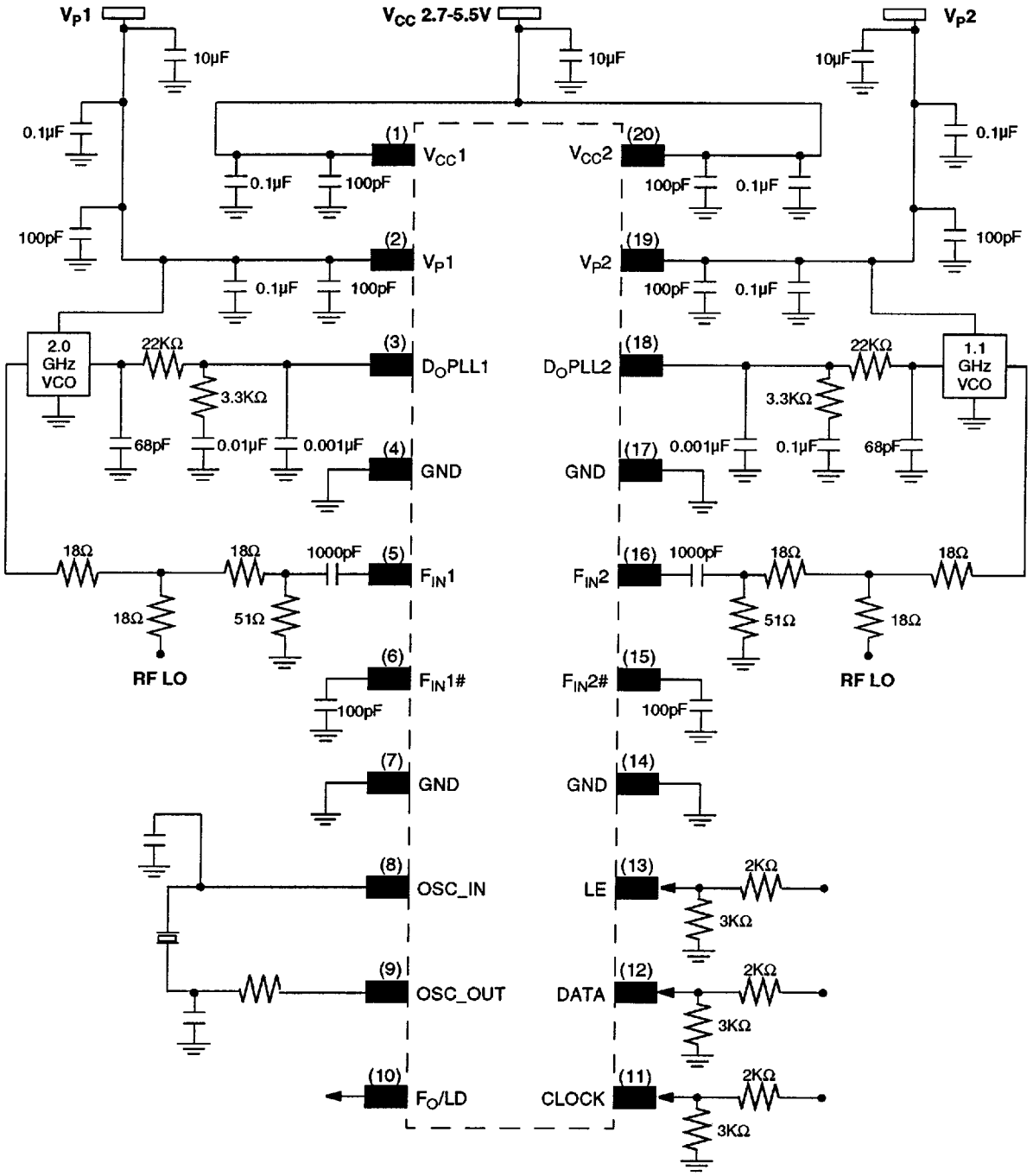


**Figure 3 Application Diagram Example - WB1336 2.01.1GHz Dual Hi/Hi PLL**



## Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|---|---|---|---|
| $V_{CC}1$ | 1 | P | ***Power Supply Connections for PLL1 and PLL2:*** When power is removed from both the Vcc1 and Vcc2 pins, all latched data is lost. |
| VP1 | 2 | P | ***PLL1 Charge Pump Rail Voltage:*** This voltage accommodates VCO circuits with tuning voltages higher than the Vcc of PLL1. |
| $D_O$PLL1 | 3 | O | ***PLL1 Charge Pump Output:*** The phase detector gain is $\flat/2\pi$. Sense polarity can be reversed by setting the FC bit in software (via the Shift Register). |
| GND | 4 | G | ***Analog and Digital Ground Connections:*** This pin must be grounded. |
| $F_{IN}1$ | 5 | I | ***Input to PLL1 Prescaler:*** Maximum frequency 2.0GHz. |
| $F_{IN}1$# | 6 | I | ***Complementary Input to PLL1 Prescaler:*** A bypass capacitor should be placed as closely as possible to this pin and must be connected directly to the ground plane. |
| GND | 7 | G | ***Analog and Digital Ground Connections:*** These pins must be grounded. |
| OSC_IN | 8 | I | ***Oscillator Input:*** This input has a Vcc/2 threshold and CMOS logic level sensitivity. |
| OSC_OUT | 9 | O | ***Oscillator Output:*** |
| $F_O$/LD | 10 | O | ***Lock Detect Pin:*** The output is high when the loop is locked. It is multiplexed to the output of the programmable counters or reference dividers in the test program mode. (Refer to Table 4 for configuration) |
| CLOCK | 11 | I | ***Data Clock Input:*** On the rising edge, one bit of data is loaded into the Shift Register. |
| DATA | 12 | I | ***Serial Data Input*** |
| LE | 13 | I | ***Load Enable:*** On the rising edge of this signal, the data stored in the Shift Register is latched into the counters and configuration controls, PLL1 or PLL2 depending on the control bit states. |
| GND | 14 | G | ***Analog and Digital Ground Connections:*** This pin must be grounded. |
| $F_{IN}2$# | 15 | I | ***Complementary Input to PLL2 Prescaler:*** A bypass capacitor should be placed as closely as possible to this pin and must be connected directly to the ground plane. |
| $F_{IN}2$ | 16 | I | ***Input to PLL2 Prescaler:*** Maximum frequency 1.1GHz. |
| GND | 17 | G | ***Analog and Digital Ground Connections:*** These pins must be grounded. |
| $D_O$PLL2 | 18 | O | ***PLL2 Charge Pump Output:*** The phase detector gain is $\flat/2\pi$. Sense polarity can be reversed by setting the FC bit in software (via the Shift Register). |
| $V_P2$ | 19 | P | ***PLL2 Charge Pump Rail Voltage:*** This voltage accommodates VCO circuits with tuning voltages higher than the Vcc of PLL2. |
| $V_{CC}2$ | 20 | P | ***Power Supply Connections for PLL1 and PLL2:*** When power is removed from both the Vcc1 and Vcc2 pins, all latched data is lost. |

**Note:** Never have both PLLs programmed to the same frequency. They will lock to each other under these conditions. The divide ration can be calculated using the following equation:

fvco = {(P * B) + A} * fosc / R where (A < B)

fvco: Output frequency of the external VCO.
fosc: The crystal reference oscillator frequency.
A: Preset divide ratio of the 7-bit swallow counter (0 to 127).
B: Preset ratio of the 11-bit programmable counter (3 to 2047).
P: Preset divide ratio of the dual modulus prescaler (64/65 or 128/129).
R: Preset ratio of the 15-bit programmable reference counter (3 to 32767).

The divide ratio N = (P * B) + A.

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ or $V_P$ | Power Supply Voltage | –0.5 to + 6.5 | V |
| $V_{OUT}$ | Output Voltage | –0.5 to $V_{CC}$+0.5 | V |
| $I_{OUT}$ | Output Current | ±15 | mA |
| $T_L$ | Lead Temperature | +260 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +150 | °C |

## Handling Precautions

Devices should be transported and stored in antistatic containers.

These devices are static sensitive. Ensure that equipment and personnel contacting the devices are properly grounded.

Cover workbenches with grounded conductive mats.

Always turn off power before adding or removing devices from system.

Protect leads with a conductive sheet when handling or transporting PC boards with devices.

If devices are removed from the moisture protective bags for more than 36 hours, they should be baked at 85°C in a moisture free environment for 24 hours prior to assembly in less than 24 hours.

## Recommended Operating Conditions

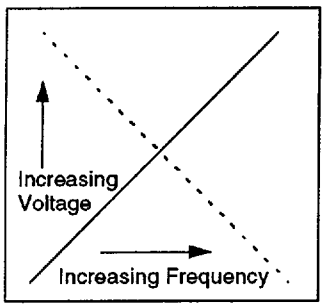
| Symbol | Parameter | Rating | Unit | Test Condition |
|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 2.7 to 5.5 | V | |
| $V_P$ | Charge Pump Voltage | $V_{CC}$ to + 5.5 | V | |
| $T_A$ | Operating Temperature | –40 to +85 | °C | Ambient air at 0 CFM flow |

## Electrical Characteristics: $V_{CC} = V_P = 5V$, $T_A = -40°C$ to $+85°C$ Unless otherwise specified

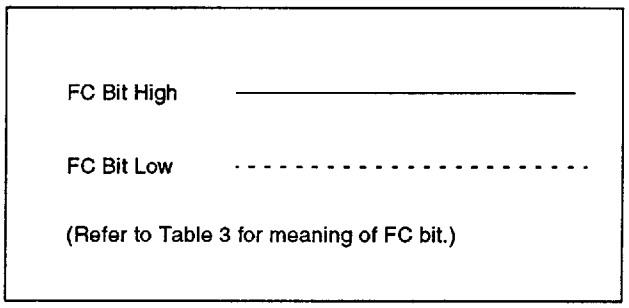
| Symbol | Parameter | Pin | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current PLL1 + PLL2 | $V_{CC}1$, $V_{CC}2$ | | 15 | | mA | |
| $I_{PD}$ | Power-down Current | $V_{CC}1$, $V_{CC}2$ | | 1 | 25 | µA | Power-down, $V_{CC} = 3.0V$ |
| $F_{IN}1$ | Operating Frequency | $F_{IN}1$ | 100 | | 2000 | MHz | PLL1 |
| $F_{IN}2$ | | $F_{IN}2$ | 100 | | 1100 | MHz | PLL2 |
| $F_{OSC}$ | Oscillator Input Frequency | OSC_IN | 2 | | 25 | MHz | with OSC_OUT loaded |
| | | | 2 | | 40 | MHz | with OSC_OUT unloaded |
| $F\phi$ | Maximum Phase Detector Frequency | | 10 | | | MHz | |
| $V_{IN}$ | Input Sensitivity | $F_{IN}1$ and $F_{IN}2$ | -15 | | 4 | dBm | $V_{CC} = 3.0V$ |
| | | | -10 | | 4 | dBm | $V_{CC} = 5.0V$ |
| $V_{OSC}$ | Oscillator Input Sensitivity | OSC_IN | 0.5 | | | $V_{P-P}$ | |
| $I_{IH}$, $I_{IL}$ | High/Low Level Input Current | | | ±50 | | µA | |
| $V_{IH}$ | High Level Input Voltage | DATA, CLOCK, LE | $V_{CC} * 0.8$ | | | V | |
| $V_{IL}$ | Low Level Input Voltage | | | | $V_{CC} * 0.2$ | V | |
| $I_{IH}$, $I_{IL}$ | High/Low Input Current | | −10 | 0.05 | 10 | µA | |
| $V_{OH}$ | High level Output Voltage | $F_O$/LD | $V_{CC} * 0.8$ | | | V | $V_I = 1mA$ |
| $V_{OL}$ | Low Level Output Voltage | | | | $V_{CC} * 0.2$ | V | |
| $ID_{OH(SO)}$ | $ID_O$ High, Source Current | $D_O$PLL1 $D_O$PLL2 | | 4.3 | | mA | $D_O = V_P/2$ |
| $ID_{OL(SO)}$ | $ID_O$ Low, Source Current | | | 1.25 | | mA | |
| $ID_{OH(SI)}$ | $ID_O$ High, Sink Current | | | 4.3 | | mA | |
| $ID_{OL(SI)}$ | $ID_O$ Low, Sink Current | | | 1.25 | | mA | |
| $\Delta ID_O$ | $ID_O$ Charge Pump Sink and Source Mismatch | | | 3 | | % | $D_O = V_P/2$ $ID_{O(SO)} - ID_{O(SI)}/ID_{O(SI)}$ T = 25°C |
| $I_{OFF}$ | High Impedance Leakage Current | | | ±2.5 | | nA | Loop locked, between reference spikes |

## Timing Waveforms

### Key:




VCO Characteristics




Phase Comparator Sense

**Figure 4 Phase Detector Output Waveform**

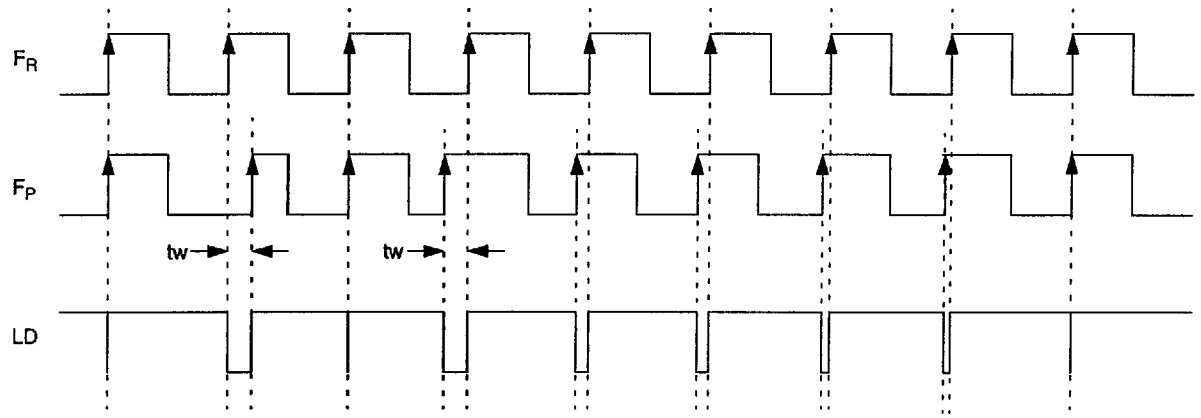



**Figure 5 DO Charge Pump Output Current Waveform**

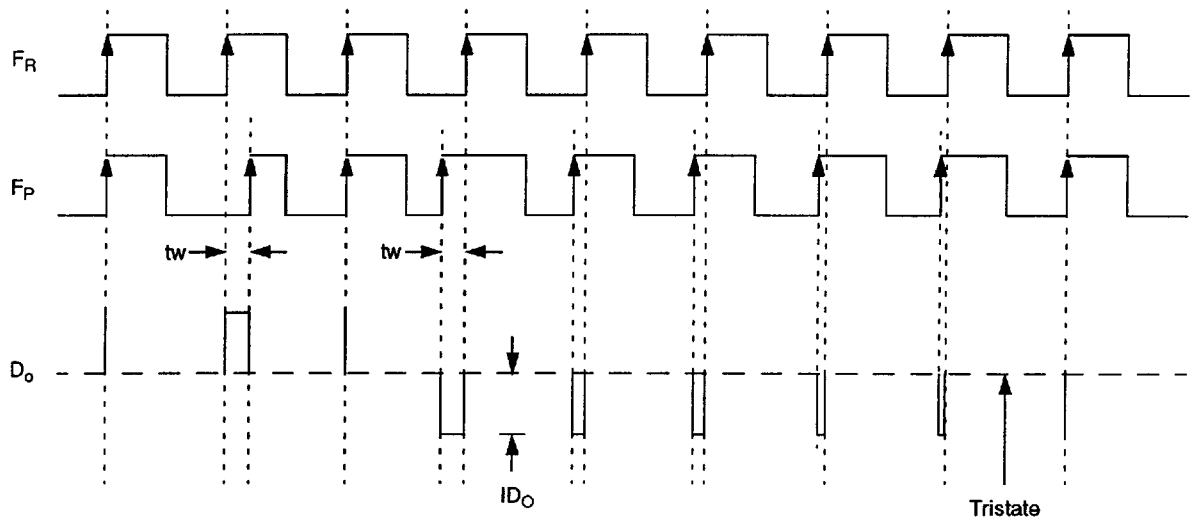
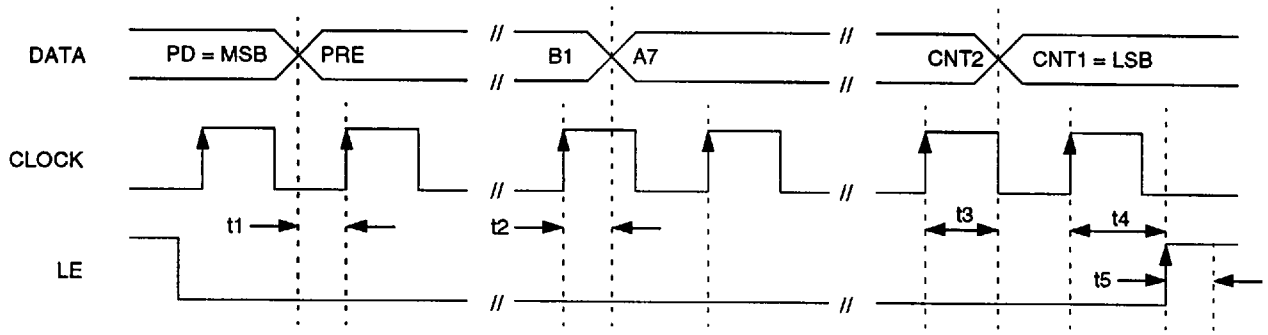


**Figure 6 Serial Data Input Timing Waveform**




**Notes:** 1. t1-t5 = 50 > t > 0.5µs

2. CLOCK may remain high after latching in data.
3. DATA is shifted in with the MSB first.
4. For DATA definitions, refer to Table 3.

## Serial Data Input

Data is input serially using the DATA, CLOCK, and LE pins. Two control bits direct data into the locations given in Table 2.

**Table 2 Control Configuration**

| CNT1 | CNT2 | Function |
|---|---|---|
| 0 | 0 | ***Program Reference 2***: R = 3 to 32767, set PLL2 (low frequency) phase detector polarity, set current in PLL2, set PLL2 tristate, set monitor selector to PLL2. |
| 0 | 1 | ***Program Reference 1:*** R = 3 to 32767, set PLL1 (high frequency) phase detector polarity, set current in PLL1, set PLL1 tristate, set monitor selector to PLL1. |
| 1 | 0 | ***Program Counter for PLL2:*** A = 0 to 127, B = 3 to 2047, set PLL2 prescaler ratio, set power-down to PLL2. |
| 1 | 1 | ***Program Counter for PLL1:*** A = 0 to 127, B = 3 to 2047, set PLL1 prescaler ratio, set power-down to PLL1. |

### Table 3 Shift Register Configuration (Note 1)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Reference Counter and Configuration Bits** | | | | | | | | | | | | | | | | | | | | | |
| CNT1 | CNT2 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 | R13 | R14 | R15 | FC | IDO | TS | LD | FO |
| **Programmable Counter bits** | | | | | | | | | | | | | | | | | | | | | |
| CNT1 | CNT2 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | B11 | PRE | PD |

| Bit(s) Name | Function |
|---|---|
| CNT1, CNT2 | ***Control Bits:*** Directs programming data to PLL1 (high frequency) or PLL2 (low frequency). |
| R1-R15 | ***Reference Counter Setting Bits:*** 15 bits, R = 3 to 32767 (Note 2). |
| FC | ***Phase Sense of the Phase Detector:*** Set to match the VCO polarity, H = + (Positive VCO transfer function). |
| $ID_O$ | ***Charge Pump Setting Bit:*** $ID_O$ high = 4.3mA, $ID_O$ low = 1.25mA. |
| TS | ***Tristate Bit:*** Tristates the $D_O$ output for PLL2 or PLL1 when high. |
| LD | ***Lock Detect:*** Directs the lock detect signal source pin 10. Pin 10 is high when locked with narrow low excursions. When not locked, this pin is low. |
| $F_O$ | ***Frequency Out:*** This bit can be set to read out reference or programmable divider at the LD pin for test purposes. |
| PRE | ***Prescaler:*** Prescaler divide bit, for PLL1 and PLL2 (low = 64/65, high = 128/129). |
| PD | ***Power-down:*** Low = power-up, high = power-down. $F_{IN}$ is at a high impedance state, respective B counter is disabled, forces tristate at $D_O$ outputs and phase comparators are disabled. The reference counter is disabled and the OSC input is high impedance after both PLLs are powered down. Data can be input and latched in the power-down state. |
| A1-A7 | ***Swallow Counter Divide Ratio:*** A = 0 to 127. |
| B1-B11 | ***Programmable Counter Divide Ratio:*** B = 3 to 2047 (Note 2). |

**Notes:** 1. The MSB is loaded in first.

2. Low count ratios may violate frequency limits of the phase detector.

### Table 4 $F_O$/LD Pin Truth Table

| FO (Bit 22) | | LD (Bit 21) | | $F_O$/LD Pin Output State |
|---|---|---|---|---|
| PLL1 | PLL2 | PLL1 | PLL2 | |
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | PLL2 Lock Detect |
| 0 | 0 | 1 | 0 | PLL1 Lock Detect |
| 0 | 0 | 1 | 1 | PLL1/PLL2 Lock Detect |
| 0 | 1 | X | 0 | PLL2 Reference Divider Output |
| 1 | 0 | X | 0 | PLL1 Reference Divider Output |
| 0 | 1 | X | 1 | PLL2 Programmable Divider Output |
| 1 | 0 | X | 1 | PLL1 Programmable Divider Output |
| 1 | 1 | 0 | 1 | PLL2 Counter Reset |
| 1 | 1 | 1 | 0 | PLL1 Counter Reset |
| 1 | 1 | 1 | 1 | PLL1/PLL2 Counter Reset |

**Table 5 7-Bit Swallow Counter (A) Truth Table**

| Divide Ratio A | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|---|
| **PLL1 (High Frequency)** | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: |
| 126 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **PLL2 (Low Frequency)** | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: |
| 126 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note:** B is greater than A.

**Table 6 11-Bit Programmable Counter (B) Truth Table**

| Divide Ratio B | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: |
| 2046 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 2047 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note:** Divide ratio less than 3 is prohibited. (See equation below).

**Table 7 15-Bit Programmable Reference Counter (for PLL1 and PLL2) Truth Table**

| Divide Ratio R | R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: | ::: |
| 32766 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 32767 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note:** Divide ratio less than 3 is prohibited. The divide ratio can be calculated using the following equation:

$fvco = \{(P * B) + A\} * fosc / R$ where $(A < B)$

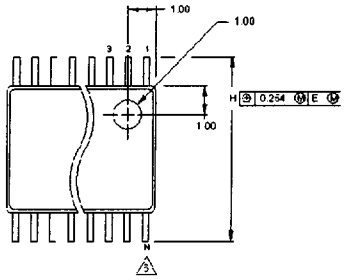
fvco: Output frequency of the external VCO.
fosc: The crystal reference oscillator frequency.
A: Preset divide ratio of the 7-bit swallow counter (0 to 127).
B: Preset ratio of the 11-bit programmable counter (3 to 2047).
P: Preset divide ratio of the dual modulus prescaler (64/65 or 128/129).
R: Preset ratio of the 15-bit programmable reference counter (3 to 32767).

The divide ratio $N = (P * B) + A$.

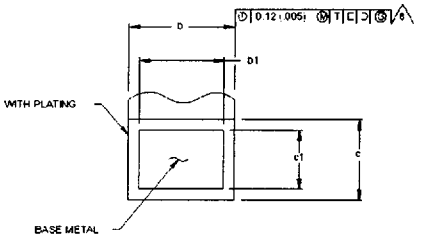
IC WORKS

# Mechanical Package Outline

## Figure 7 TSSOP (0.173" Wide)

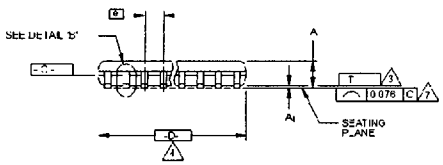



TOP VIEW

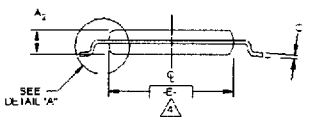



DETAIL "C"
SCALE: 20/1

(SEE NOTE 9)

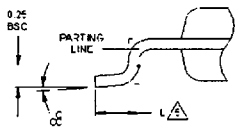



SIDE VIEW

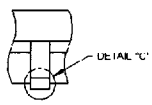



END VIEW

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.273±0.0127 (.01 0±.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS 'B' AND 'C'.
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.




DETAIL 'A'
SCALE: 30/1




DETAIL "B"
SCALE: 30/1
DAMBAR PROTRUSION

**Physical Dimensions in Millimeters**
**20 Lead (0.173" Wide) TSSOP Package Order Number X**
**20" clear antistatic tubes, 76 units/tube**
**JEDEC Outline MO-153**

### THIS TABLE IN MILLIMETERS

| SYMBOL | COMMON DIMENSIONS MIN. | NOM. | MAX. | NOTE | NOTE VARIATIONS | 4 D MIN. | NOM. | MAX. | 6 N |
|---|---|---|---|---|---|---|---|---|---|
| A | | | 1.10 | | AA | 2.90 | 3.00 | 3.10 | 8 |
| $A_1$ | 0.05 | 0.10 | 0.15 | | AB | 4.90 | 5.00 | 5.10 | 14 |
| $A_2$ | 0.85 | 0.90 | 0.95 | | AC | 4.90 | 5.00 | 5.10 | 16 |
| b | 0.19 | - | 0.30 | 8 | AD | 6.40 | 6.50 | 6.60 | 20 |
| b1 | 0.19 | 0.22 | 0.25 | | AE | 7.70 | 7.80 | 7.90 | 24 |
| c | 0.090 | - | 0.20 | | AF | 9.60 | 9.70 | 9.80 | 28 |
| c1 | 0.090 | 0.127 | 0.135 | | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | | |
| E | 4.30 | 4.40 | 4.50 | 4 | | | | | |
| e | 0.65 BSC | | | | | | | | |
| H | 6.25 | 6.40 | 6.50 | | | | | | |
| L | 0.50 | 0.60 | 0.70 | 5 | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | | |
| α | 0° | 4° | 8° | | | | | | |

### THIS TABLE IN INCHES

| SYMBOL | COMMON DIMENSIONS MIN. | NOM. | MAX. | NOTE | NOTE VARIATIONS | 4 D MIN. | NOM. | MAX. | 6 N |
|---|---|---|---|---|---|---|---|---|---|
| A | | | .0433 | | AA | .114 | .118 | .122 | 8 |
| $A_1$ | .002 | .004 | .006 | | AB | .193 | .197 | .201 | 14 |
| $A_2$ | .0335 | .0354 | .0374 | | AC | .193 | .197 | .201 | 16 |
| b | .0075 | - | .0118 | 8 | AD | .252 | .256 | .260 | 20 |
| b1 | .0075 | .0087 | .0098 | | AE | .303 | .307 | .311 | 24 |
| c | .0035 | - | .0079 | | AF | .378 | .382 | .386 | 28 |
| c1 | .0035 | .0050 | .0053 | | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | | |
| E | .169 | .173 | .177 | 4 | | | | | |
| e | .0256 BSC | | | | | | | | |
| H | .246 | .252 | .256 | | | | | | |
| L | .020 | .024 | .028 | 5 | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | | |
| α | 0° | 4° | 8° | | | | | | |

*VARIATION AF IS DESIGNED BUT NOT TOOLED*