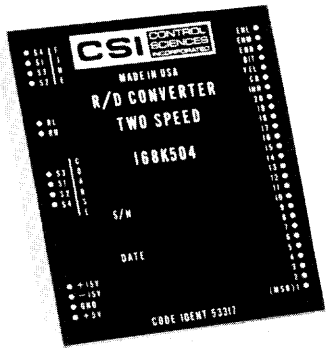
synchro resolver-to-digital converter
single module 2-speed 20-bit
series 168K500



FEATURES
- 1:16, 1:32 or 1:36 speed ratios
- 4-second accuracy
- 20-bit byte/parallel output with 3-state output latches
- 2-speed inputs, multiple pole or geared types
- Insensitive to rotor-to-stator phase shifts up to 70°
- Single module

APPLICATIONS
Radar Tracking — Satellite Tracking — Robotics — Precise Angle Measurements

GENERAL DATA

The Series 168K500 is the first 20-bit two speed, high performance, synchro (or resolver) - to - digital converter specifically designed to operate with multiple pole synchros or resolvers. The converter employs a synthesized reference which corrects for rotor-to-stator phase shifts up to 70° which is common to multipole synchros or resolvers. The module also includes the 2-speed combining, crossover network and stickoff circuits necessary for 2-speed conversion. The binary angle output is 3-state addressable as either three-bytes or one 20-bit word.

THEORY OF OPERATION

The theory of operation for single-speed tracking synchro-to-digital (S/D) converter is explained first. The same principles apply for a resolver-to-digital converter.

Single-Speed Converter (See Figure 1)

The S/D converter determines the value of the input angle Φ by comparing a digital feedback angle Θ with the synchro input angle. When the difference between the input angle and the feedback angle is zero, the output angle contained in the up-down counter is equal to the synchro input angle.

The Function Generator performs the trigonometric computation:

$$\sin(\Phi-\Theta) = (\sin\Phi\cos\Theta - \cos\Phi\sin\Theta)$$

Note that for small angles, $\sin(\Phi-\Theta) \cong (\Phi-\Theta)$. The equality given by the above equation is true only in the first quadrant, i.e., 0° to 90°. The analog inputs to the Function Generator have different values depending on the quadrant in which the input angle lies.

The $\Phi-\Theta$ is an analog representation of the error between Φ the input angle, and Θ the output angle. This analog error is first demodulated then fed to an analog integrator whose output controls the frequency of a Voltage-Controlled Oscillator (VCO). The VCO clocks the up-down counter. The up-down counter is functionally an integrator, therefore the tracking converter in itself is a closed-loop servomechanism with two lags, making it a "Type II" servo loop. The "Type II" servo loop tracking converter exhibits no velocity errors and only minor acceleration errors.

ELECTRICAL SPECIFICATIONS

Parameter	Value			
Resolution	20-bits (0.00034°)			
Accuracy[1]	4 seconds (1:32 or 1:36)			
	8 seconds (1:16)			
Speed Ratios	1:16, 1:32 or 1:36			
Allowable Synchro Misalignment[2]	±2°			
Allowable Rotor to Stator Phase Shift				
Coarse Input	±20°			
Fine Input	±70°			
Synchro Input Rates	**47-70 Hz**	**350-450 Hz**	**800-1200 Hz**	**2200-2800 Hz**
Maximum Tracking Rate	112°/sec	112°/sec	112°/sec	112°/sec
Acceleration Constant (K_a)	3,600 sec^{-2}	37,000 sec^{-2}	150,000 sec^{-2}	326,000 sec^{-2}
Power Supplies[3]				
+15V	50 mA max (45 mA typ)			
−15V	50 mA max (45 mA typ)			
+ 5V	50 mA max (45 mA typ)			
Digital Inputs/Outputs				
Parallel Binary Angle	3-state, 2 TTL loads max.			
Converter Busy (CB)	0.5 to 1.0 μs positive pulse, 2 TTL loads max.			
Built-In-Test (BIT)	Logic '0' = tracking, logic '1' = error 2 TTL loads max.			
Inhibit (INH)[4]	Logic '0' latches output angle			
Enable H (ENH)[5]	Logic '0' enables bits 1-4 Logic '1' disables			
Enable M (ENM)[5]	Logic '0' enables bits 5-12 Logic '1' disables			
Enable L (ENL)[5]	Logic '0' enables bits 13-20 Logic '1' disables			
Velocity Output				
Scale Factor	±1.0V ±0.2V for 12°/sec			
Range	±10V min.			
Loading	10 kohms max.			
Synchro/Resolver Input[6]				
11.8V L-L	75 kohms min.			
90V L-L	600 kohms min.			
Reference Input[6]				
23 to 29 Vrms	180 kohms min.			
103 to 127 Vrms	800 kohms min.			
Input Type[7]	Solid-state differential			
Temperature Ranges				
Operating	0° to 70°			
Storage	−55°C to 125°C			
Dimensions	3.125″ × 2.625″ × 0.8″			
Weight	7.5 oz			

NOTES:

1. Accuracy applies for:
   (a) ±10% signal amplitude variation
   (b) 10% harmonic distortion in the reference
   (c) over power supply range
   (d) over operating temperature range

NOTES: (Continued)

2. With two-speed synchro converters, it is important to understand that the output of the fine synchro dominates in the determination of the coarse (1X) shaft angle. No ambiguities will exist unless the allowable misalignment is exceeded.
3. All units can operate on voltages between ±11.5V to ±16.5V. The tolerance on the +5V supply is ±0.25V.
4. The Inhibit is a CMOS input with a 50 kohm pull-up to +5V.
5. Enable H, M and L are CMOS inputs with 50 kohm pull-downs to ground.
6. Other voltages available, consult factory.
7. Any one stator and/or rotor line may be grounded. Common mode voltages up to specified L-L voltage have no effect on operation.

Two-Speed Converter (See Figure 2)

The operation of a 2-speed S/D converter is essentially the same as the single speed except there are two Solid State Control Transformers (SSCT) generating two error voltages. Assuming an off-null condition (the input angle does not equal the output angle), the crossover detector feeds the coarse SSCT error signal to the demodulator which is driven by the rotor excitation. As the output angle Θ approaches the input angle Φ the coarse SSCT output approaches a null. When the coarse SSCT output drops below a preset threshold, approximately equivalent to 2.8°, the crossover detector switches the fine SSCT error signal into the demodulator. Simultaneously the source of the demodulator drive voltage is switched to the synthesized reference which is derived from fine stators therefore negating the fine rotor to stator phase shift. The feedback angle Θ to the fine SSCT is multiplied by the speed ratio therefore increasing the voltage gradient of the fine SSCT by the same factor. The servo loop then is able to seek an even finer null. The converter will continue to use the fine error signal for continuous tracking. In order to eliminate false stable nulls of 180°, an angle offset produced by the Digital Adder and the Scaler, which produces the Stick-Off Voltage (SO), is introduced into the coarse SSCT.

The 20-bit parallel binary angle is outputted through 3-state transparent latches which can be enabled as one 20-bit word or three bytes (one 4-bit and two 8-bit). By use of the Inhibit input, the 20-bit angle data can be latched without affecting the operation of the converter servo loop.

DIGITAL INPUTS/OUTPUTS

Digital outputs consist of 20 parallel data bits, a Converter Busy (CB) and a BIT logic output.

The parallel digital outputs are addressable either as one 20-bit word or three bytes (one 4-bit and two 8-bit). When Enable H, M and L are at logic '0' the outputs are at normal logic '1' or '0'. When Enable H, M and L are at logic '1' the outputs are in the high impedance state. Outputs are valid 0.5 microseconds after an Enable is driven to logic '0'.

The CB output is a positive 0.5 to 1.0 microsecond pulse, and data changes during the CB pulse. Data is valid at the trailing edge of the CB pulse.

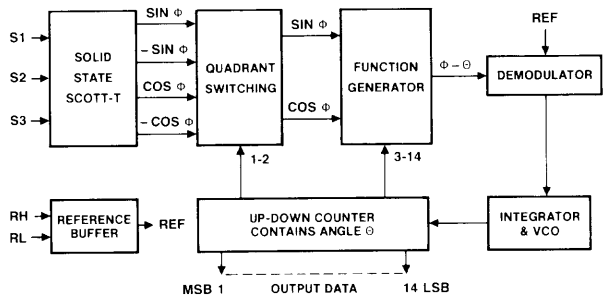
The BIT logic output is a built-in-test derived from the crossover detector. Whenever the digital output is not tracking the synchro or resolver input within the fine speed range the BIT output goes to logic '1'.

The Inhibit (INH) input locks the 20-bit transparent latch so that the data bits will remain stable while data is being transferred. The output is stable 0.5 microseconds after INH is driven to logic '0'. If a CB pulse occurs after an INH has been applied, logic '0', the 20-bit latch will remain locked and its data cannot change until INH is driven back to logic '1' and CB returns to logic '0'. If an INH is applied during a CB pluse, the 20-bit latch will not lock until the CB pulse is over. Inhibit commands do not affect the updating of the converter no matter how long they are applied.

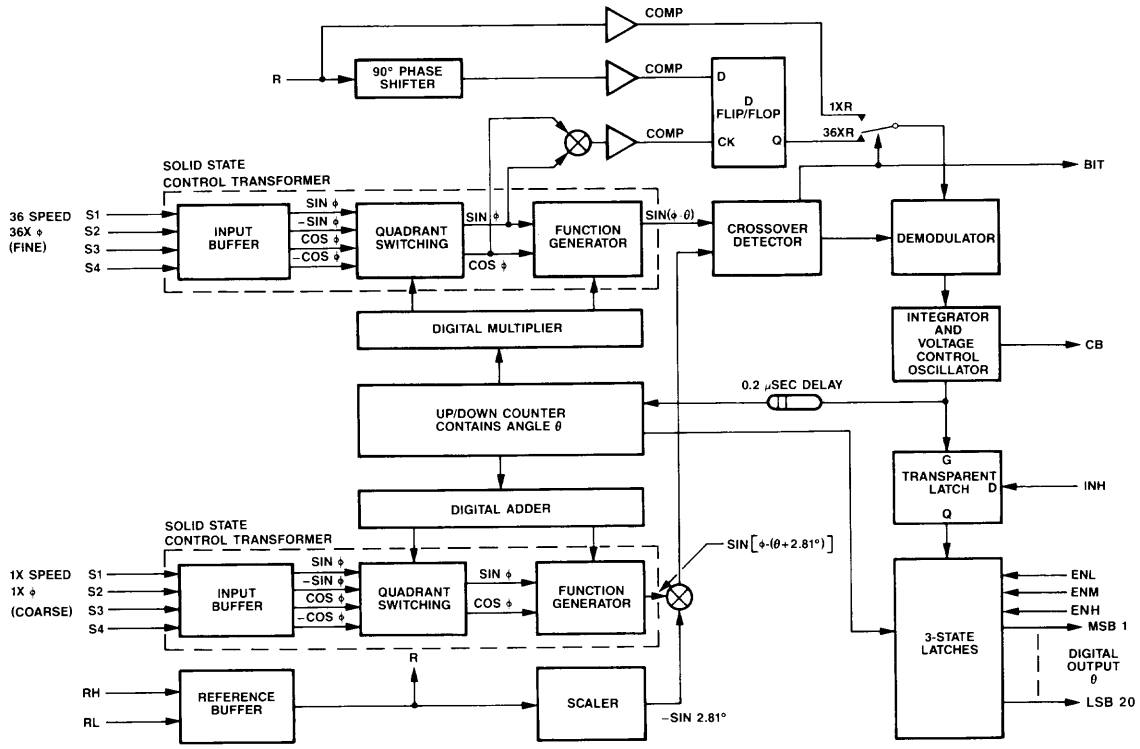
TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB and generates a CB pulse. During the 0.5 to 1.0 microsecond CB time, the output data is changing and should not be transferred. The converter will ignore an INH command applied during a CB interval until that interval is over. There are two methods of interfacing with a computer: (1) synchronous, and (2) asynchronous. A simple method of synchronous loading is to: (a) apply the Inhibit, (b) wait

SINGLE-SPEED CONVERTER BLOCK DIAGRAM
Figure 1



TWO-SPEED CONVERTER BLOCK DIAGRAM
Figure 2



seconds, (c) transfer the data, and (d) release the Inhibit. Asynchronous loading is accomplished by transferring data on the trailing edge of the CB pulse.

ANALOG VELOCITY OUTPUT

Velocity (VEL) is a DC voltage proportional to the angular velocity of the synchro or resolver shaft. Voltage polarity is positive for an increasing digital angle and negative for a decreasing digital angle. Other characteristics are listed in the specifications table.

DYNAMIC PERFORMANCE

The 168K500 series employs a "Type II" servo loop ($K_v - \infty$) and very high acceleration constants (K_a). The loop dynamics are completely independent of power supply variations over their specific ranges. As long as the maximum tracking rate is not exceeded there will be no velocity lag and only minor acceleration lags in the converter output. Acceleration lag can be computed from the following equation:

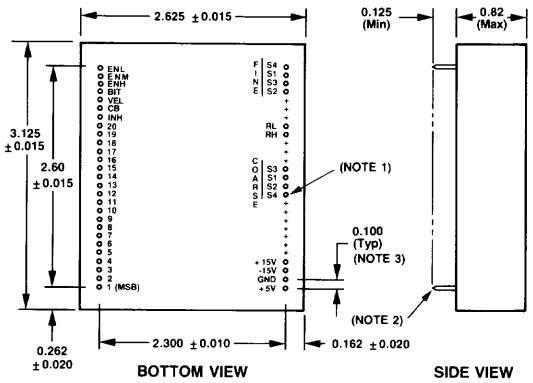
$$E_a = \frac{\text{acceleration } (°/\text{sec}^2)}{K_a}$$

The open loop transfer functions for all frequency options are given below:

$$G_{60} = \frac{58^2\left(\frac{S}{43}+1\right)}{S^2\left(\frac{S}{164}+1\right)} \qquad G_{400} = \frac{183^2\left(\frac{S}{132}+1\right)}{S^2\left(\frac{S}{526}+1\right)}$$

$$G_{1000} = \frac{378^2\left(\frac{S}{278}+1\right)}{S^2\left(\frac{S}{1041}+1\right)} \qquad G_{2600} = \frac{577^2\left(\frac{S}{370}+1\right)}{S^2\left(\frac{S}{1493}+1\right)}$$

MECHANICAL OUTLINE



NOTES:

1. S4 pin appears on resolver input model only.
2. Rigid 0.025 diameter pins for solder-in or plug-in applications.
3. Noncumulative.
4. Dimensions are in inches unless otherwise specified.

ORDERING INFORMATION

168K SUFFIX	INPUT TYPE	STATOR VOLTAGE	REFERENCE VOLTAGE	FREQ.	SPEED RATIO
500	SYNCHRO	11.8V	26V	400 Hz	1:36
501	SYNCHRO	90V	115V	400 Hz	1:36
502	SYNCHRO	90V	115V	60 Hz	1:36
503	RESOLVER	11.8V	26V	400 Hz	1:36
504	RESOLVER	11.8V	26V	1000 Hz	1:36
505	RESOLVER	11.8V	26V	2600 Hz	1:36

NOTES:

1. Standard temperature range 0° to 70°C
2. Standard speed ratio is 1:36; for 1:16 or 1:32, add suffix −16 or −32 to part number.

The standard part numbers listed do not cover the variety of multipole synchros or resolvers that are available.

In order for CSI to specify the right converter for a specific multipole synchro or resolver our applications engineering department must have the following information:

(a) Rotor voltage and frequency
(b) Coarse (1X) transformation ratio and phase shift
(c) Fine (NX) transformation ratio and phase shift
(d) Z_S (primary shorted)