

T-52-13-07



GigaBit Logic

16G076

LED Driver 1 Gbit/s NRZ Data Rate

FEATURES

- DC to 1 Gbit/s NRZ data rates
- Shunt drive output design provides low output impedance, fast rise/fall times, low output jitter
- $T_r = 300$ ps, $T_f = 500$ ps (typ.)
- 500 mW power dissipation (typ.)
- 1-150 mA output current
- DC-blocked ECL, GaAs PicoLogic™ compatible Input
- Available in 18 pin leadless chip carrier, die, or as an assembled and tested evaluation board

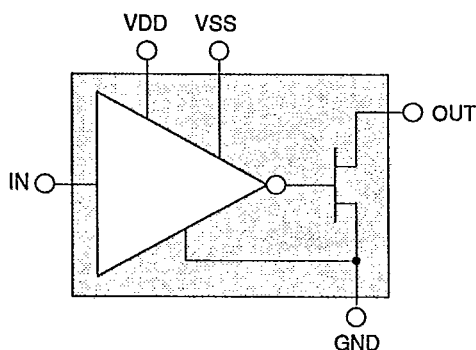
FUNCTIONAL DESCRIPTION

The 16G076 is a unique, high performance GaAs IC LED driver capable of operation up to 1 Gbit/s NRZ. Its shunt-drive output circuit design (the output switch transistor is connected to the LED in parallel) provides fundamental advantages in high speed optical systems, compared with series connected drivers. The 16G076 has a low output impedance regardless of its operation state: current source or sink. As a result, it achieves high speed driving without resorting

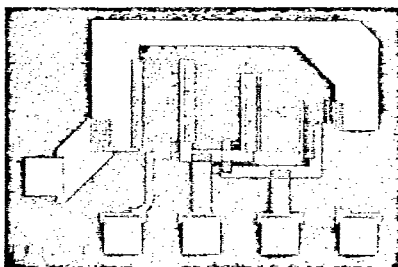
to external speed-up networks (which can result in overshoot and undershoot of the optical output) and data pattern-induced output jitter is very low.

The 16G076's input is compatible with DC-blocked ECL or GaAs PicoLogic™ signals (1 Vp-p, zero centered). Output current is switchable between 1 and 150 mA max.

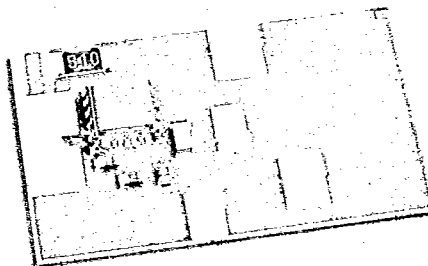
CIRCUIT DIAGRAM



CHIP PHOTOMICROGRAPH



EVALUATION BOARD



ORDERING INFORMATION

Package Type	Part No.
18 pin Leadless Chip Carrier	16G076-L1
Unpackaged Die	16G076-X
Evaluation Board (Assembled & Tested)	16G076-L1E

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
VDD	Supply Voltage	0 to +5V
VSS	Supply Voltage	0 to -5V
PD	Power Dissipation	2W
VIN	Input Voltage	-2 to +0.7V
VOUT	DC Output Voltage	0 to +5V
IOUT	DC Output Current	300 mA
TSTOR	Storage Temperature	-55 to +150°C
TA	Ambient Operating Temperature	-55 to +120°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS
VDD	Supply Voltage	+2.5	+3.5	+4.5	V
VSS	Supply Voltage	-3.5	-2.0	-1.5	V

ELECTRICAL CHARACTERISTICS

VDD = +3.5V, VSS = -2.0V, TA = 25°C

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Supply Current	IDD			100	140	mA
	ISS			-80	-120	mA
Input Voltage	VIH		+0.5			V
	VIL				-0.8	V
Input Current	IIN	VIN = +0.5V			50	μA
Output Current * VOUT = 1.0V	IOUT (MIN)	VIN = -0.8V*			1	mA
	IOUT (MAX)	VIN = +0.5V*	150			mA
Rise Time	tr	RL = 25Ω		300		ps
Fall Time	tf	RL = 25Ω		500		ps

PRECAUTIONS

Owing to their small dimensions, the GaAs FETs from which the 16G076 is designed can be damaged or destroyed if subjected to large transient voltages.

Such transients can be generated by power supplies when switched on if not properly decoupled. It is also possible to induce spikes from static electricity charged operators or ungrounded equipment. To prevent the damage to devices from transient breakdown:

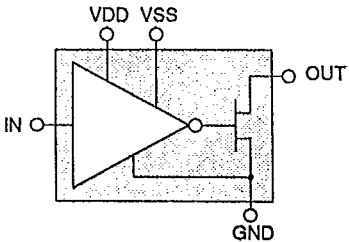
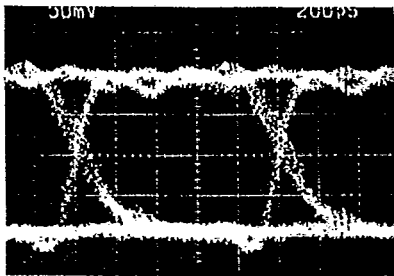
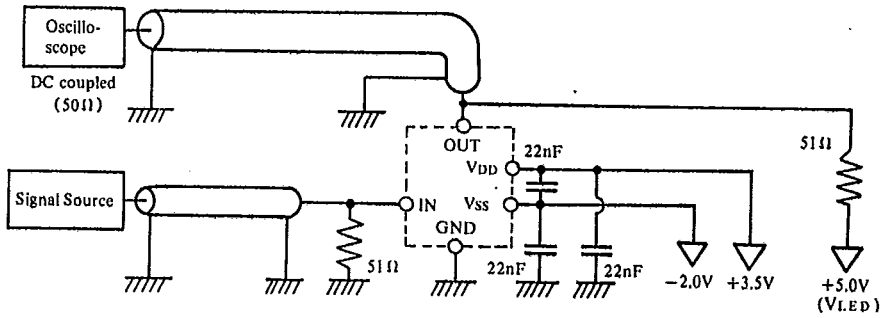
- DC ground all equipment and operators.
- Protect the devices against voltage surges when the power supplies are turned on.

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CIRCUIT DIAGRAM	PIN DESCRIPTIONS
	VDD Supply Voltage VSS Supply Voltage GND Ground IN Input OUT Output
PSEUDO-RANDOM DATA RESPONSE OF ELECTRICAL OUTPUT	
1) Eye Diagram (RL = 25Ω, 1Gbps NRZ)  Horizontal: 200 ps/div. Vertical: 50 mV/div.	
2) Measurement Block Diagram 	

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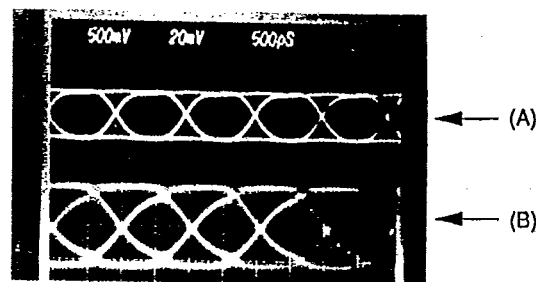


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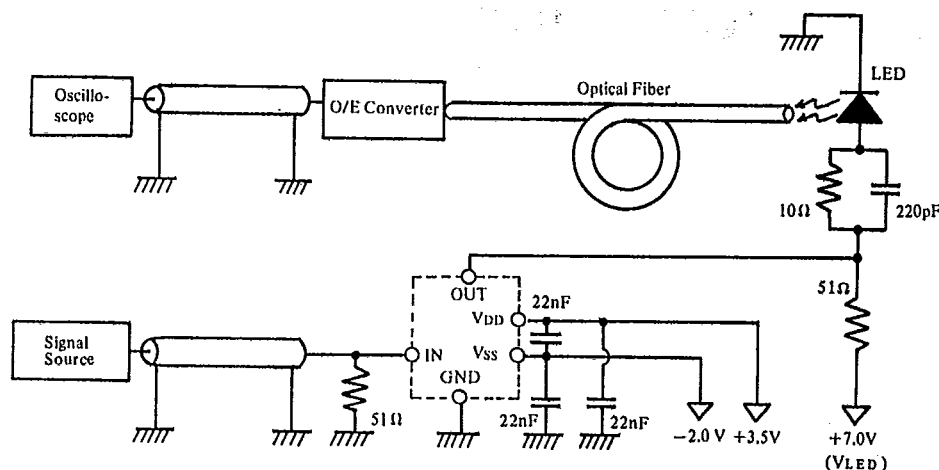
PSEUDO-RANDOM DATA RESPONSE OF OPTICAL OUTPUT

1) Eye Diagram (1 Gbps NRZ)



(A) Driver Input (B) Optical Output
LED: Sumitomo Electric SE-13T2

2) Measurement Block Diagram

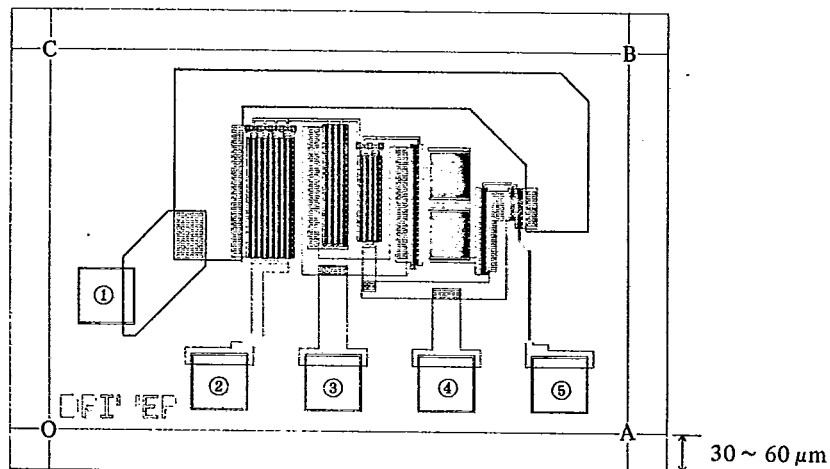




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16G076

DIE PAD ASSIGNMENTS (16G076-X)

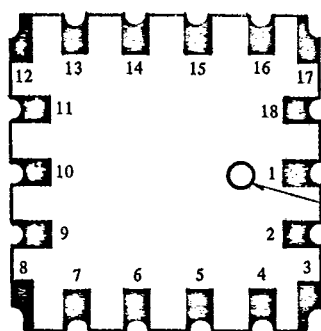


The point O designates the origin of the drawing

Thickness: 450 μm

	Pad	Pad Size	Center Position (μm)
1	GND	100 μm sq.	(100, 305)
2	OUT	100 μm sq.	(300, 155)
3	VSS	100 μm sq.	(500, 155)
4	VDD	100 μm sq.	(700, 155)
5	IN	100 μm sq.	(900, 155)
A			(1020, 0)
B			(1020, 740)
C			(0, 740)

PIN ASSIGNMENTS (BOTTOM VIEW)



Pin	Connection	Pin	Connection
1	NC	10	VDD
2	NC	11	IN
3	NC	12	NC
4	NC	13	NC
5	NC	14	NC
6	GND	15	NC
7	OUT	16	NC
8	NC	17	NC
9	VSS	18	NC



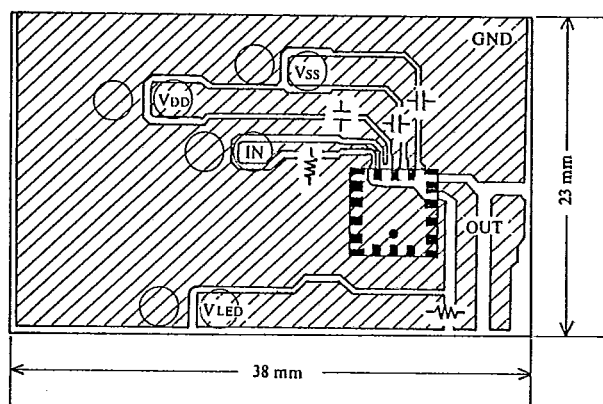
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EVALUATION BOARD USER'S GUIDE

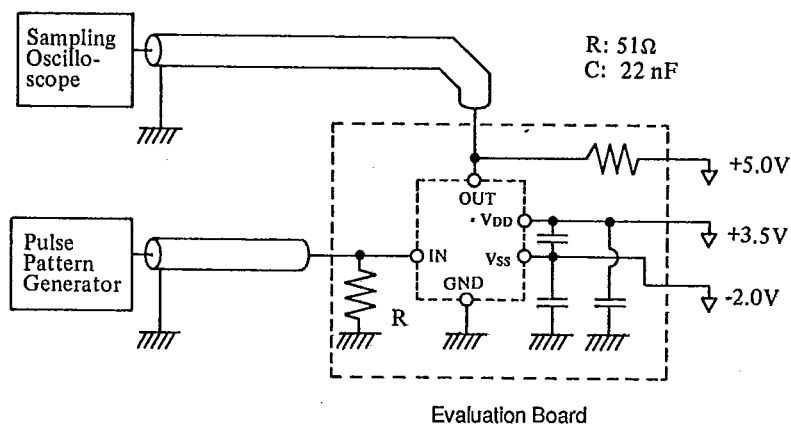
1) Board Layout



The open circles indicate soldering positions for coaxial cables.

2) Measurement Block Diagram

R: 51Ω
C: 22 nF



50Ω coaxial cable is recommended for use with the evaluation board (e.g. Microcoax P/N UT-34-SP - 0.034 dia. semi-rigid coax).

T-90-20

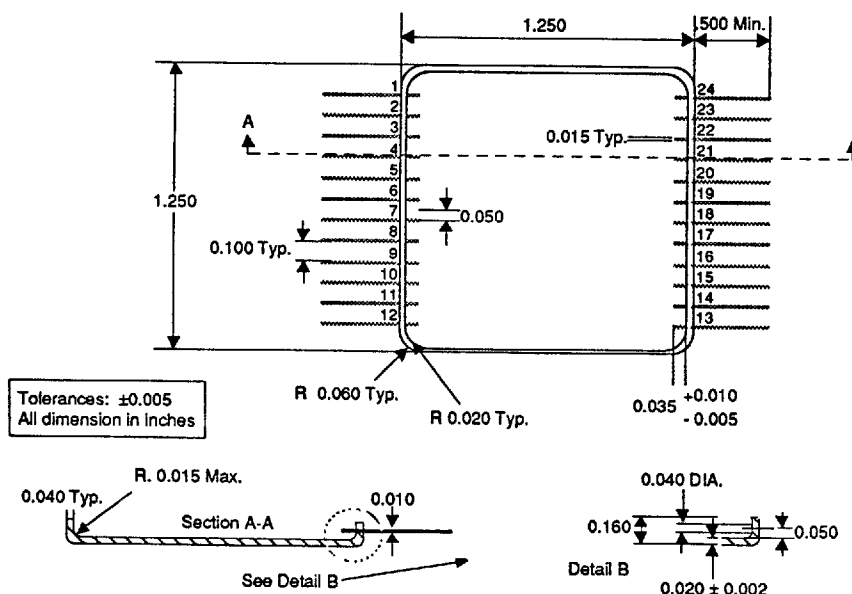


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24 PIN METAL FLATPACK 18 PIN PACKAGE

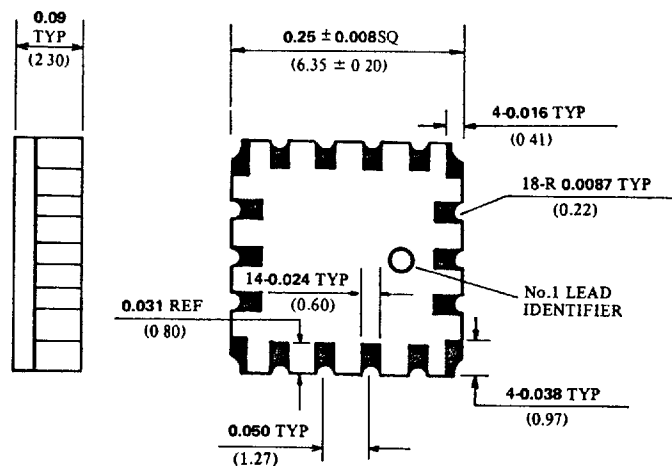
24 PIN METAL FLATPACK

Type H



18 PIN LEADLESS CHIP CARRIER

TYPE L1

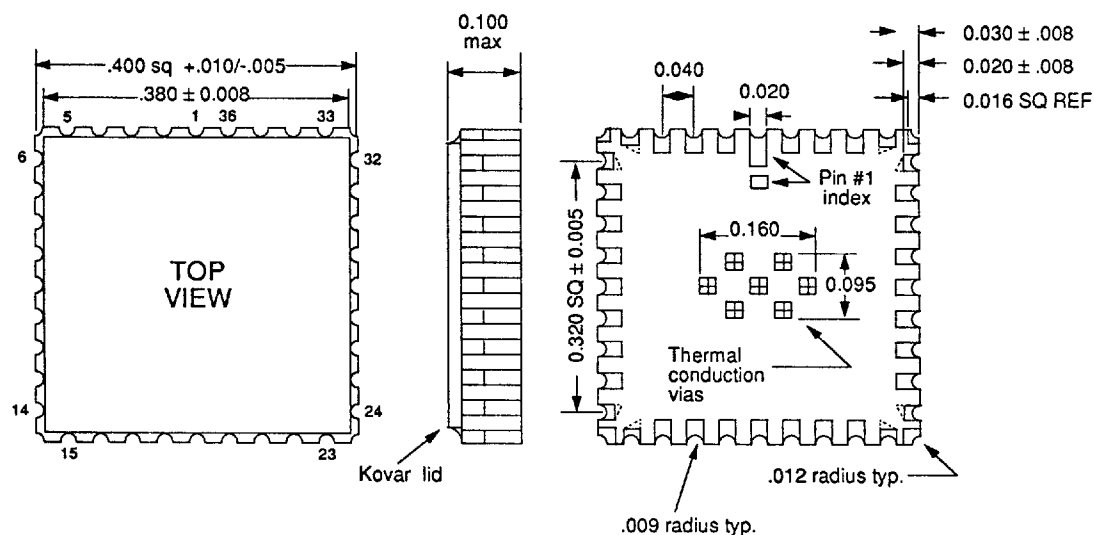




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36 PIN PACKAGES

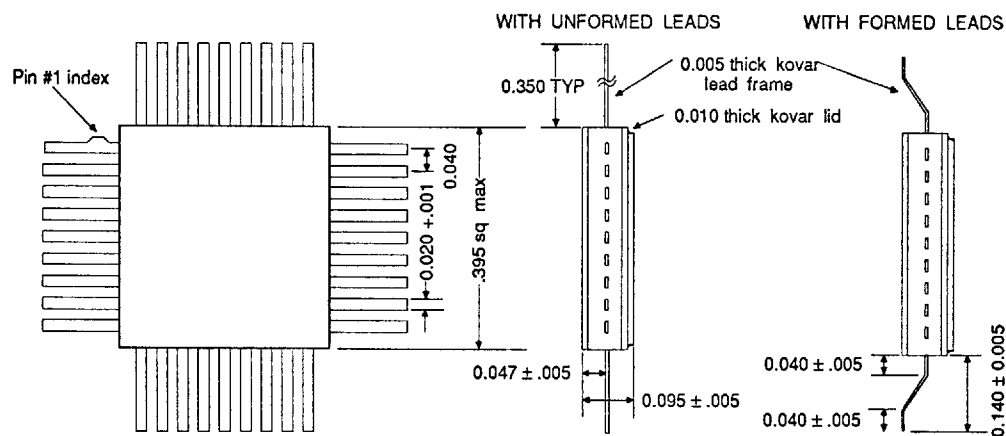
36 PIN LEADLESS CHIP CARRIER TYPE L36



NOTES:

- 1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
- 2) All dimensions in inches.
- 3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK TYPE F

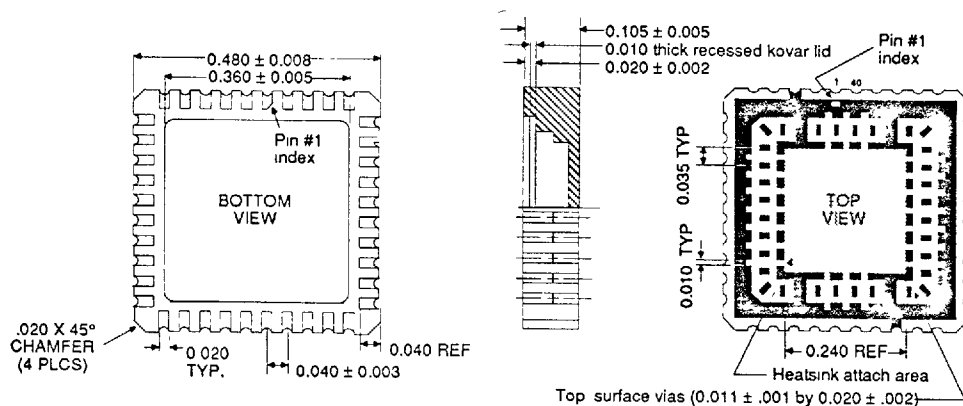




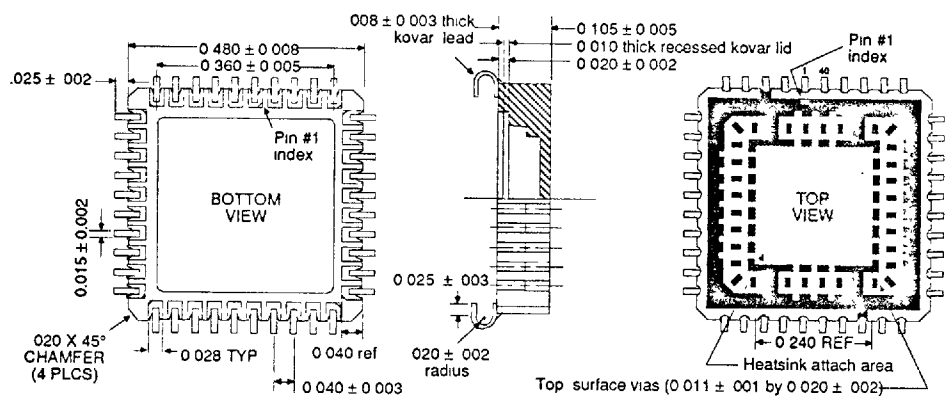
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T-90-20
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER TYPE L



40 PIN LEADED CHIP CARRIER TYPE C

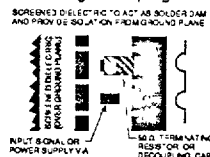


NOTES

- (1) Footprint is JEDEC standard outline
- (2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3, 4, 17, 18, 23, 24, 37, and 38
- (3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential
- (4) Recommended top surface chip resistors are 0.040 long by 0.020 wide by 0.010 thick typ. 100 mw min. nominal power rating (Mini-Systems MSR 21 or equivalent)
- (5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ. 25V VCCW 1000 pf min. (Johnson R09, case or equivalent)
- (6) Recommended heat/sinks are GBL P/Ns 90GHS 40 A and 90GHS 40 B
- (7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent)
- (8) L40 and C40 packages are dimensionally identical except for contact finger width

TOP SURFACE LEGEND	
Metalized Ceramic	
Screened Dielectric	
Bare Ceramic	

Top Surface Terminating/Decoupling Detail

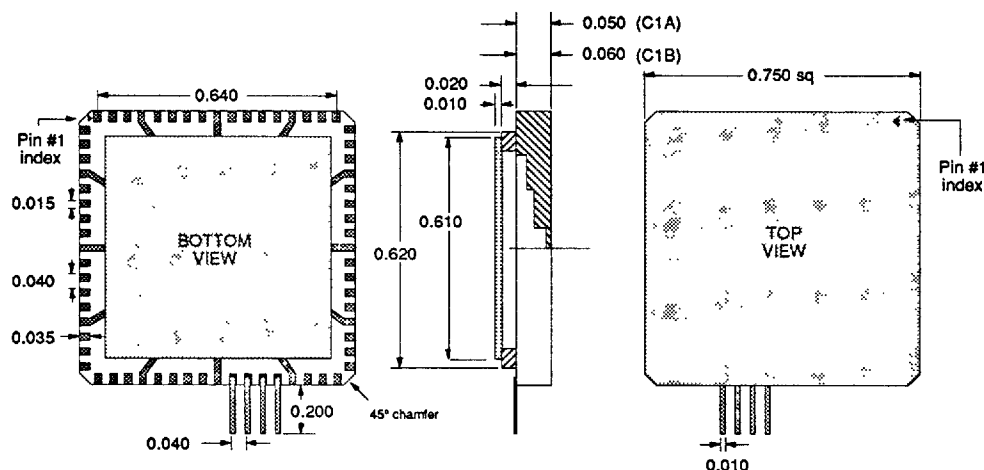




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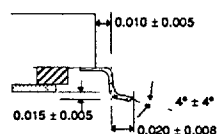
T-90-20
68 & 132 PIN
PACKAGES

68 PIN LEADED CHIP CARRIER TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is $\pm 1\%$ but not larger than ± 0.005 . Tolerance on 0.640 end pad to end pad dimension is ± 0.003 .

GULLWING LEADS



132 PIN LEADED CHIP CARRIER TYPE C3

