CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7B991
CY7B992

Programmable Skew Clock Buffer (PSCB)

Features

- **Output pair skew <100 ps typical (250 max.)**
- **All outputs skew <250 ps typical (500 max.)**
- **3.75- to 80-MHz output operation**
- **User-selectable output functions**
  - **— Selectable skew to 18 ns**
  - **— Inverted and non-inverted**
  - **— Operation at ½ and ¼ input frequency**
  - **— Operation at 2x and 4x input frequency (input as low as 3.75 MHz)**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **32-pin PLCC/LCC package**
- **Jitter < 0.5% peak to peak**
- **Compatible with the Pentium© processor**

Functional Description

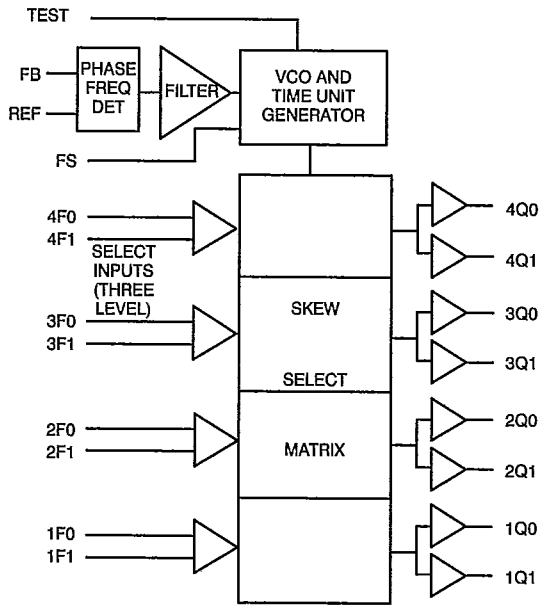
The CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB) offer user-selectable control over system clock functions. These multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B991 TTL or CY7B992 CMOS).

Each output can be hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency with outputs able to skew up to ±6 time units from their nominal "zero" skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. When this "zero delay" capability of the PSCB is combined with the selectable output skew functions, the user can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

6 LOGIC

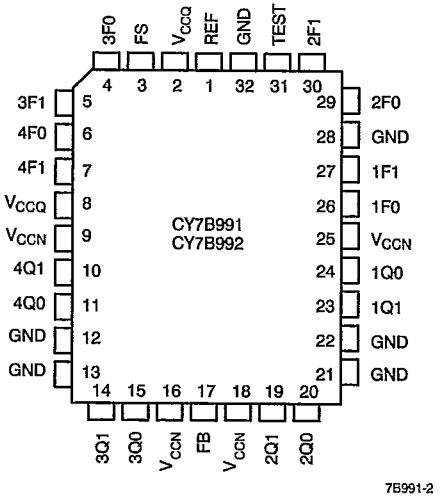
Logic Block Diagram



7B991-1

Pin Configuration

PLCC/LCC



7B991-2

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Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three-level frequency range select. See *Table 1.*
1F0, 1F1	I	Three-level function select inputs for output pair 1 (1Q0, 1Q1). See *Table 2.*
2F0, 2F1	I	Three-level function select inputs for output pair 2 (2Q0, 2Q1). See *Table 2.*
3F0, 3F1	I	Three-level function select inputs for output pair 3 (3Q0, 3Q1). See *Table 2.*
4F0, 4F1	I	Three-level function select inputs for output pair 4 (4Q0, 4Q1). See *Table 2.*
TEST	I	Three-level select. See test mode section under the block diagram descriptions.
1Q0, 1Q1	O	Output pair 1. See *Table 2.*
2Q0, 2Q1	O	Output pair 2. See *Table 2.*
3Q0, 3Q1	O	Output pair 3. See *Table 2.*
4Q0, 4Q1	O	Output pair 4. See *Table 2.*
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in *Table 1.*

Table 1. Frequency Range Select and t_U Calculation[1]

FS[2]	f_{NOM} (MHz) Min.	f_{NOM} (MHz) Max.	$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. *Table 2* below shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 2. Programmable Skew Configurations[1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Note:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see *Table 2*). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.

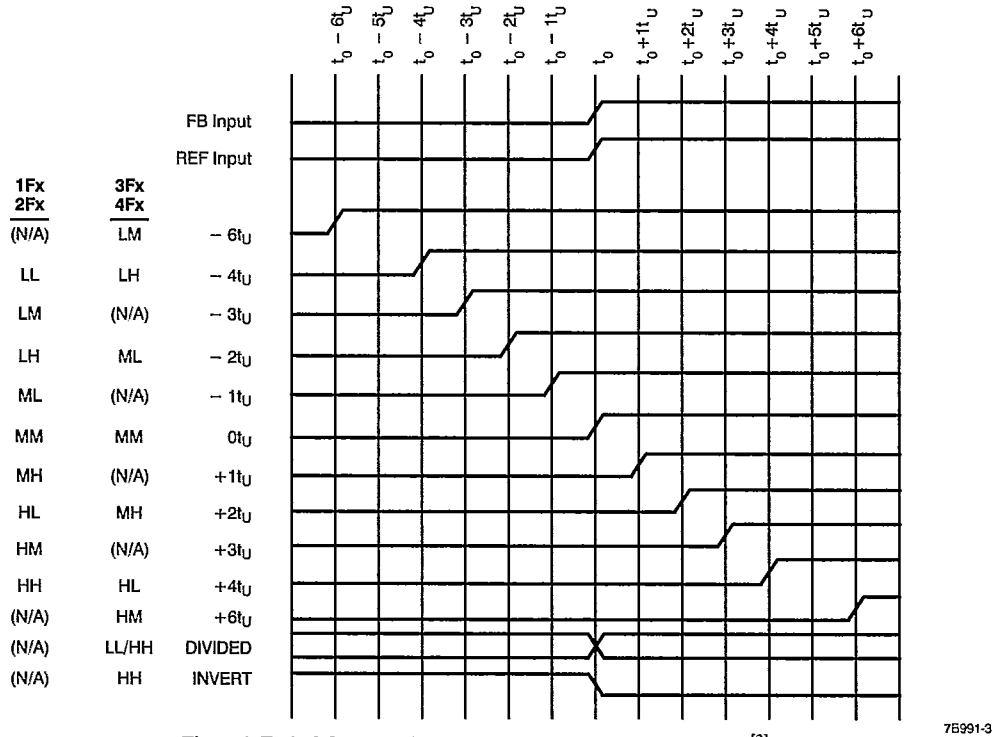


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output[3]

Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B991/CY7B992 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military[4]	− 55°C to +125°C	5V ± 10%

Notes:

3 FB connected to an output selected for "zero" skew (i.e., xF1 = xF0 = MID).

4. Indicates case temperature.

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7B991
CY7B992

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions	CY7B991 Min.	CY7B991 Max.	CY7B992 Min.	CY7B992 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 16 mA	2.4				V
		V_{CC} = Min., I_{OH} = − 40 mA			V_{CC} − 0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} = 46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} − 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		− 0.5	0.8	− 0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS, xFn)[6]	Min. ≤ V_{CC} ≤ Max.	V_{CC} − 1V	V_{CC}	V_{CC} − 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS, xFn)[6]	Min. ≤ V_{CC} ≤ Max.	$V_{CC}/2$ − 500 mV	$V_{CC}/2$ + 500 mV	$V_{CC}/2$ − 500 mV	$V_{CC}/2$ + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS, xFn)[6]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	− 500		− 500		µA
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = $V_{CC}/2$	− 50	50	− 50	50	µA
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		− 200		− 200	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND (25°C only)		− 250			mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open		80		80	mA
I_{CCN}	Output Buffer Current per Output Pair[8]	V_{CCN} = V_{CCQ} = Max., C = 50 pf, Z = 50Ω, Input Selects Open, f_{MAX}		45		57	mA
PD	Power Dissipation per Output Pair[9]	V_{CCN} = V_{CCQ} = Max., C = 50 pf, Z = 50Ω, Input Selects Open, f_{MAX}		171		148[10]	mW

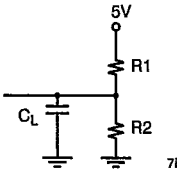
Capacitance[11]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

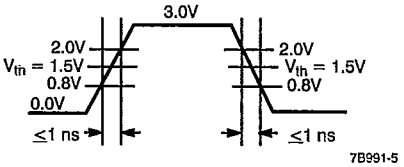
5. See the last page of this specification for Group A subgroup testing information.
6. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
7. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
8. I_{CCN} can be approximated by the following expressions:
   CY7B991:
   I_{CCN} = (2 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N
   CY7B992:
   I_{CCN} = (1.5+ 1.7F) + [((1160 − 2.8F)/Z) + (.0025FC)]N
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F * C
9. Power dissipation can be approximated by the following expressions:
   CY7B991:
   PD = (11 + 0.61F) + [((1550 − 2.7F)/Z) + (.0125FC)]N
   CY7B992:
   PD = (8.25+ 0.94F) + [((700 + 6F)/Z) + (.017FC)]N
   See note 8 for variable definition.
10. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
11. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

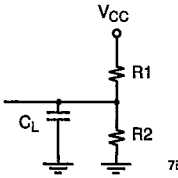


R1 = 130
R2 = 91
C_L = 50 pF (C_L = 30pF for −5 devices)
(Includes fixture and probe capacitance)

TTL AC Test Load (CY7B991)

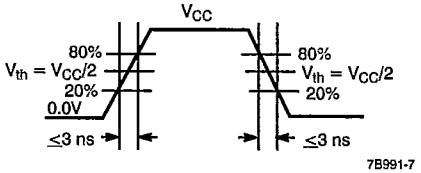


TTL Input Test Waveform (CY7B991)



R1 = 100
R2 = 100
C_L = 50 pF (C_L = 30pF for −5 devices)
(Includes fixture and probe capacitance)

CMOS AC Test Load (CY7B992)



CMOS Input Test Waveform (CY7B992)

Switching Characteristics Over the Operating Range[2, 12]

Parameter	Description		CY7B991−5 Min.	CY7B991−5 Typ.	CY7B991−5 Max.	CY7B992−5 Min.	CY7B992−5 Typ.	CY7B992−5 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2]	40		80	40		80[13]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{UE}	Programmable Skew Unit Error[14]			0.0	±0.5		0.0	±0.5	ns
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[15, 16]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[15, 17]			0.25	0.5		0.25	0.5	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[15, 18]			0.6	0.7		0.6	0.7	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[15, 18]			0.6	1.2		0.6	1.2	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[15, 18]			0.6	1.0		0.6	1.0	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[15, 18]			0.6	1.3		0.6	1.3	ns
t_{SKEW5}	Device-to-Device Skew[19]				0.2			0.2	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.5	0.0	+0.5	− 0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[20]		− 1.0	0.0	+1.0	− 1.0	0.0	+1.0	ns
t_{PWH}	Output HIGH Time Deviation from 50%[21, 24]				2.5			3.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[21, 24]				3			3.5	ns
t_{ORISE}	Output Rise Time[21, 25]		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{OFALL}	Output Fall Time[21, 25]		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{LOCK}	PLL Lock Time[22]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter, Peak to Peak[23]				0.5			0.5	%

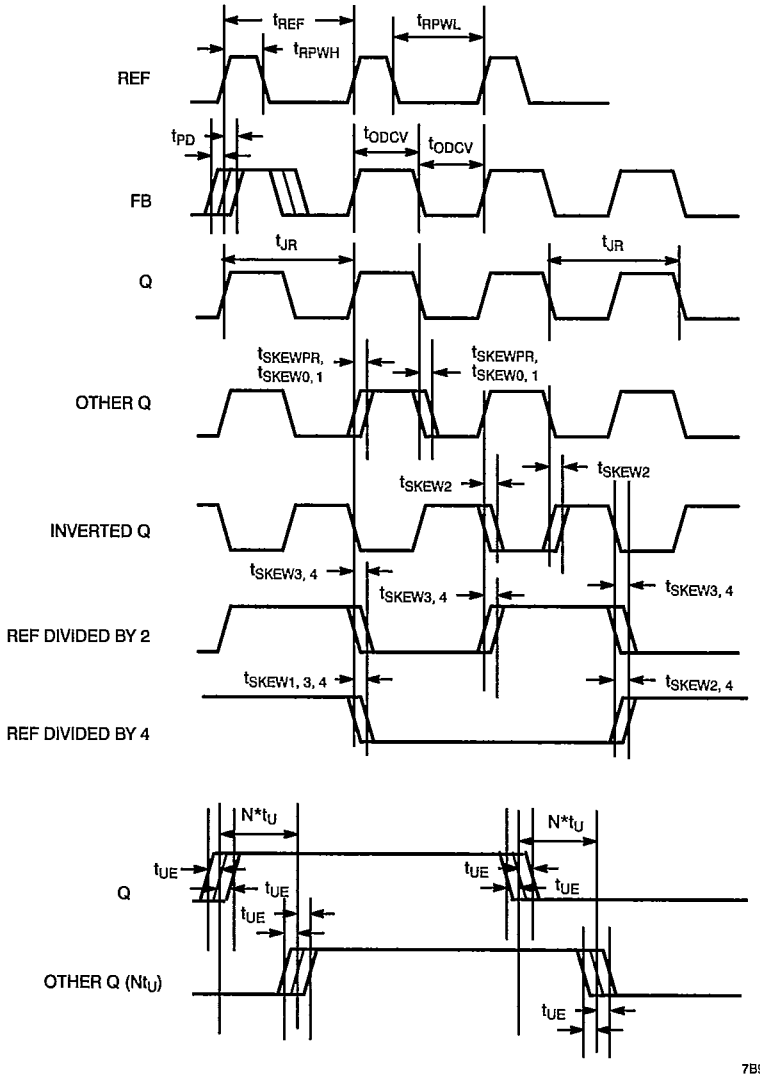
Switching Characteristics Over the Operating Range[2, 12] (continued)

Parameter	Description		CY7B991–7 Min.	CY7B991–7 Typ.	CY7B991–7 Max.	CY7B992–7 Min.	CY7B992–7 Typ.	CY7B992–7 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2]	40		80	40		50	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{UE}	Programmable Skew Unit Error[14]			0.0	±0.7		0.0	±0.7	ns
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[15, 16]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[15, 17]			0.3	0.75		0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[15, 18]			0.6	1.0		0.6	1.0	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[15, 18]			1.0	1.5		1.0	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[15, 18]			0.7	1.2		0.7	1.2	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[15, 18]			1.2	1.7		1.2	1.7	ns
t_{SKEW5}	Device-to-Device Skew[19]				0.2		0.2		ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.7	0.0	+0.7	− 0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[20]		− 1.2	0.0	+1.2	− 1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50%[21, 24]				3			5.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[21, 24]				3.5			5.5	ns
t_{ORISE}	Output Rise Time[21, 25]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[21, 25]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[22]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter, Peak to Peak[23]			0.5			0.5		%

Notes:

12. Test measurement levels for the CY7B991 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B992 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
13. Except as noted, all CY7B992–5 timing parameters are specified to 80-MHz with a 30-pF load.
14. t_{UE} is a measure of the timing error from t_U as calculated in *Table 1*. The major contributors to this error include output edge variations, cross talk, and load-induced variations between package pins and between signal lines external to the chip. t_{UE} is not cumulative across multiple t_U delays.
15. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
16. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
17. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
18. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
19. t_{SKEW5} is the output-to-output skew between the outputs used as the FB input of two or more devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.). The maximum variation between two pins on different parts is t_{SKEW5} plus the skews associated with each part.
20. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
21. Specified with outputs loaded with 30 pF for the CY7B99X–5 devices and 50 pF for the CY7B99X–7 devices. Devices are terminated through 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
22. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
23. Tested initially and after any design or process changes that may affect these parameters.
24. t_{PWH} is measured at 2.0V for the CY7B991 and 0.8 V_{CC} for the CY7B992. t_{PWL} is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
25. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or $0.8V_{CC}$ and $0.2V_{CC}$ for the CY7B992.

AC Timing Diagrams



Operational Mode Descriptions

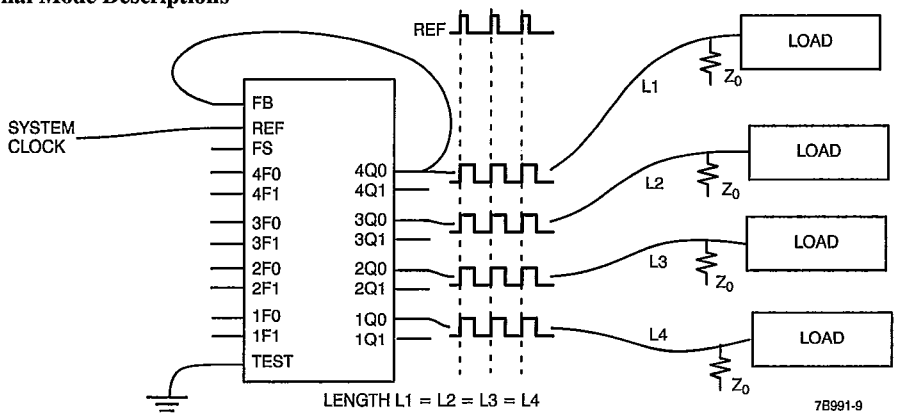


Figure 2. Zero-Skew and/or Zero-Delay Clock Driver

Figure 2 shows the PSCB configured as a zero-skew clock buffer. In this mode the 7B991/992 can be used as the basis for a low-skew clock distribution tree. When all of the function select inputs (xF0, xF1) are left open, the outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

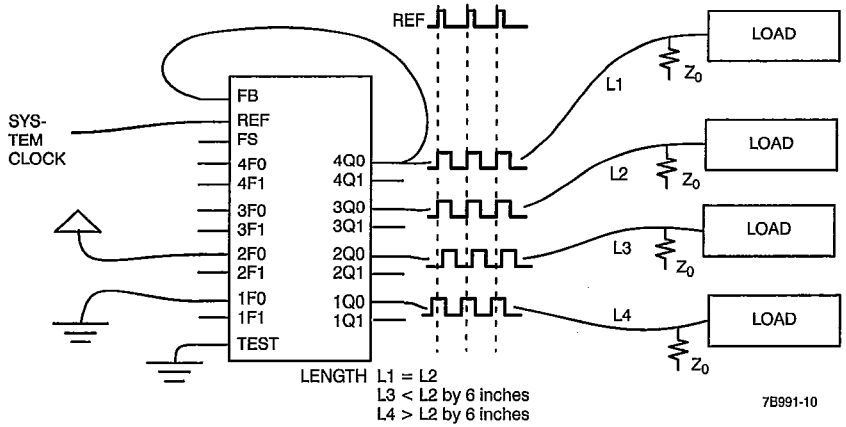


Figure 3. Programmable-Skew Clock Driver

Figure 3 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the PSCB can be programmed to stagger the timing of its outputs. The four groups of output pairs can each be programmed to different output timing. Skew timing can be adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is fed back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads can receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0-ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to insure that all outputs have precise phase alignment.

Clock skews can be advanced by ±6 time units (t_U) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since "Zero Skew", $+t_U$, and $-t_U$ are defined relative to output groups, and since the PLL aligns the rising edges of REF and FB, it is possible to create wider output skews by proper selection of the xFn inputs. For example a $+10\ t_U$ between REF and 3Qx can be achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at $-4\ t_U$ and 3Qx skews to $+6\ t_U$, a total of $+10\ t_U$ skew is realized.) Many other configurations can be realized by skewing both the output used as the FB input and skewing the other outputs.

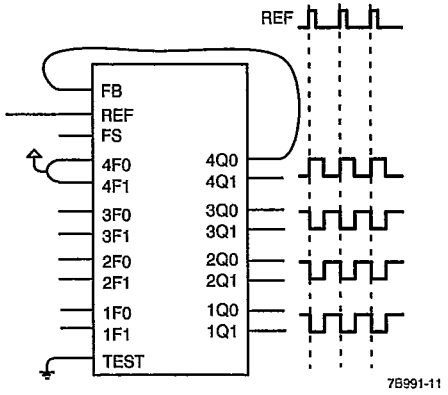


Figure 4. Inverted Output Connections

Figure 4 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the "inverted" outputs with respect to the REF input. By selecting which output is connect to FB, it is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs. The correct configuration would be determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 5 illustrates the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, which results in a 40-MHz waveform at these outputs. Note that the 20- and 40-MHz clocks fall simultaneously and are out of phase on their rising edge. This will allow the designer to use the rising edges of the ½ frequency and ¼ frequency outputs without concern for rising-edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80-MHz operation because that is the frequency of the fastest output.

Figure 6 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This allows use of the rising edges of the ½ frequency and ¼ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15- to 30-MHz range since the highest frequency output is running at 20 MHz.

Figure 7 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function allows the two subsystems to each be clocked 180 degrees out of phase, but still to be aligned within the skew spec.

The divided outputs offer a zero-delay divider for portions of the system that need the clock to be divided by either two or four, and still remain within a narrow skew of the "1X" clock. Without this feature, an external divider would need to be added, and the propagation delay of the divider would add to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the PSCB to multiply the clock rate at the REF input by either two or four. This mode will enable the designer to distribute a low-frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low-skew characteristics of the clock driver. The PSCB can perform all of the functions described above at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

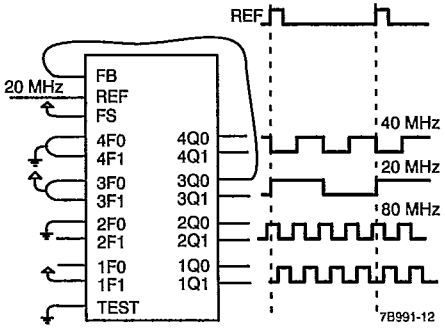


Figure 5. Frequency Multiplier with Skew Connections

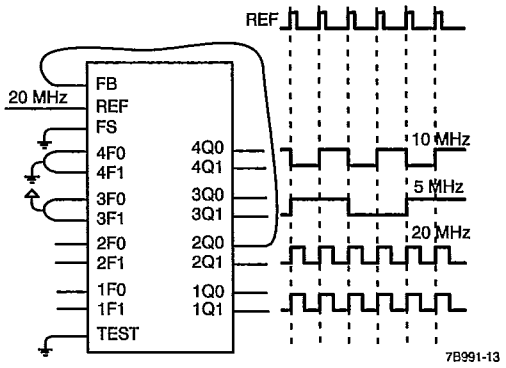


Figure 6. Frequency Divider Connections

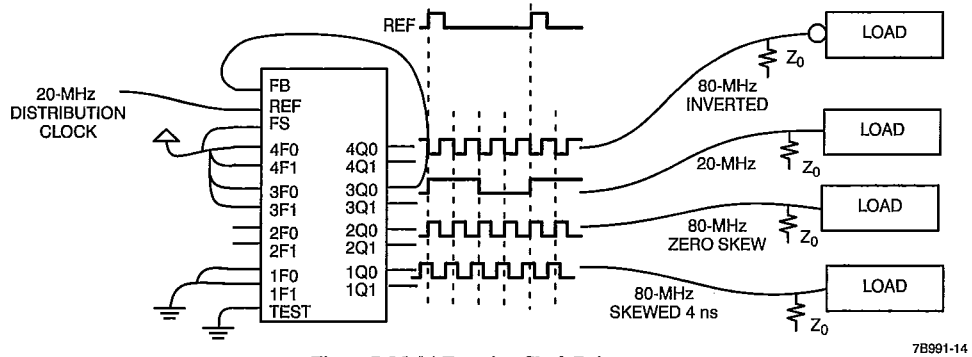


Figure 7. Multi-Function Clock Driver

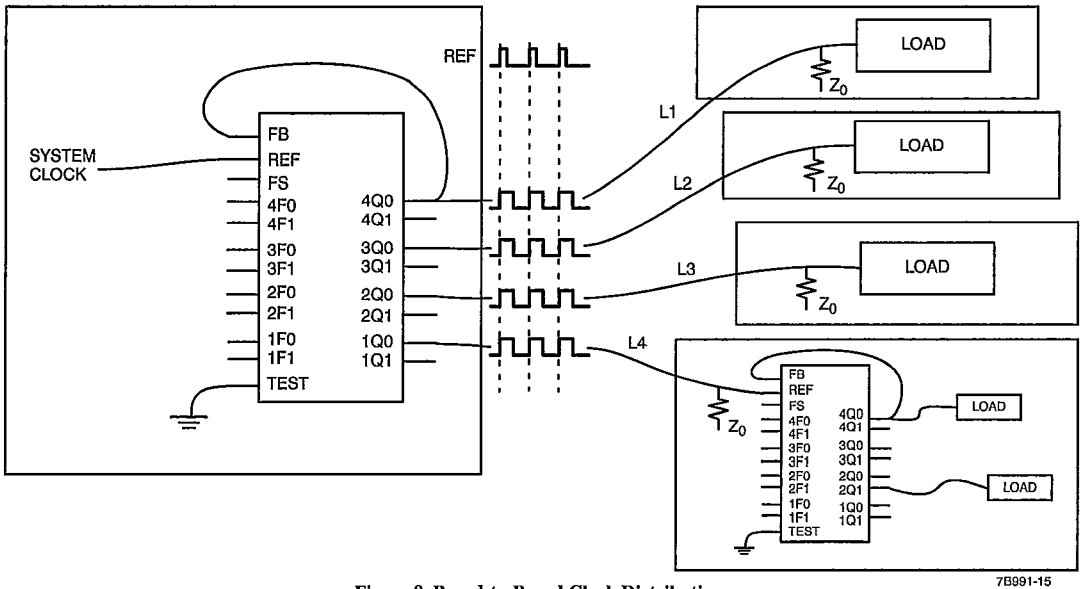


Figure 8. Board-to-Board Clock Distribution

Figure 8 shows the CY7B991/992 connected in series to construct a zero-skew clock distribution tree between boards. Delays of the downstream clock buffers can be programmed to compensate for the wire length (i.e., select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero-delay clock tree. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is not recommended that more than two clock buffers be connected in series.

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B991–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–5LC	L55	32-Pin Rectangular Leadless Chip Carrier	

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
750	CY7B991–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–7LC	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B991–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B991–7LI	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B991–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B992–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–5LC	L55	32-Pin Rectangular Leadless Chip Carrier	

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
750	CY7B992–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–7LC	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B992–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B992–7LI	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B992–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{IHH}	1, 2, 3
V_{IMM}	1, 2, 3
V_{ILL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{IHH}	1, 2, 3
I_{IMM}	1, 2, 3
I_{ILL}	1, 2, 3
I_{OS}	1
I_{CCQ}	1, 2, 3
I_{CCN}	1, 2, 3
PD	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{REF}	9, 10, 11
t_{RPWH}	9, 10, 11
t_{RPWL}	9, 10, 11
t_{U}	9, 10, 11
t_{UE}	9, 10, 11
t_{SKEWPR}	9, 10, 11
t_{SKEW0}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{SKEW3}	9, 10, 11
t_{SKEW4}	9, 10, 11
t_{SKEW5}	9, 10, 11
t_{PD}	9, 10, 11
t_{ODCV}	9, 10, 11
t_{PWH}	9, 10, 11
t_{PWL}	9, 10, 11
t_{QRISE}	9, 10, 11
t_{QFALL}	9, 10, 11
t_{LOCK}	9, 10, 11

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CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

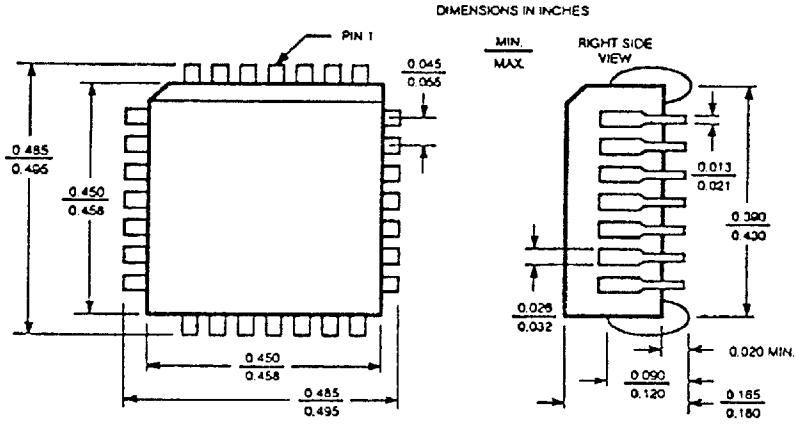
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

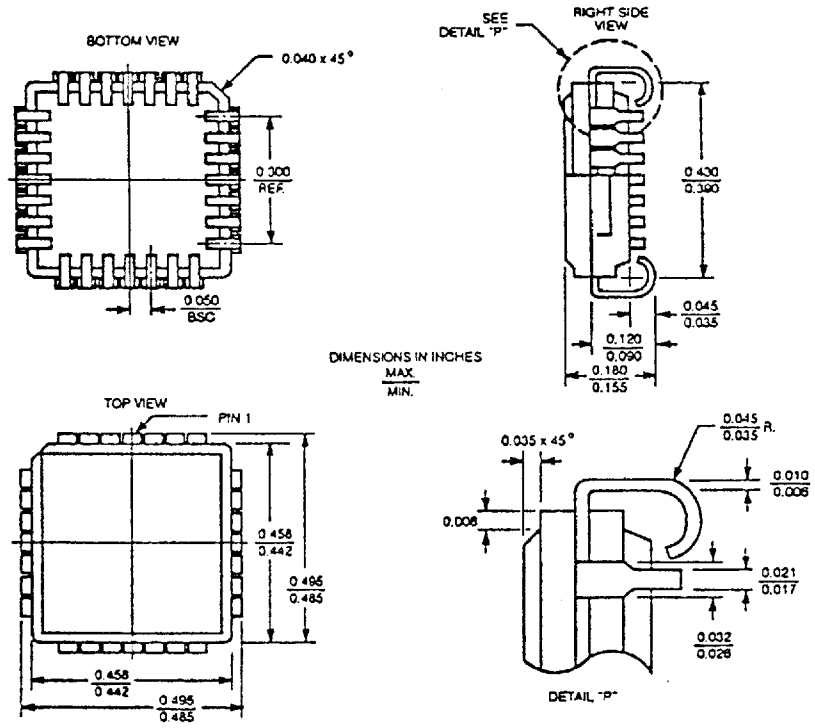


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

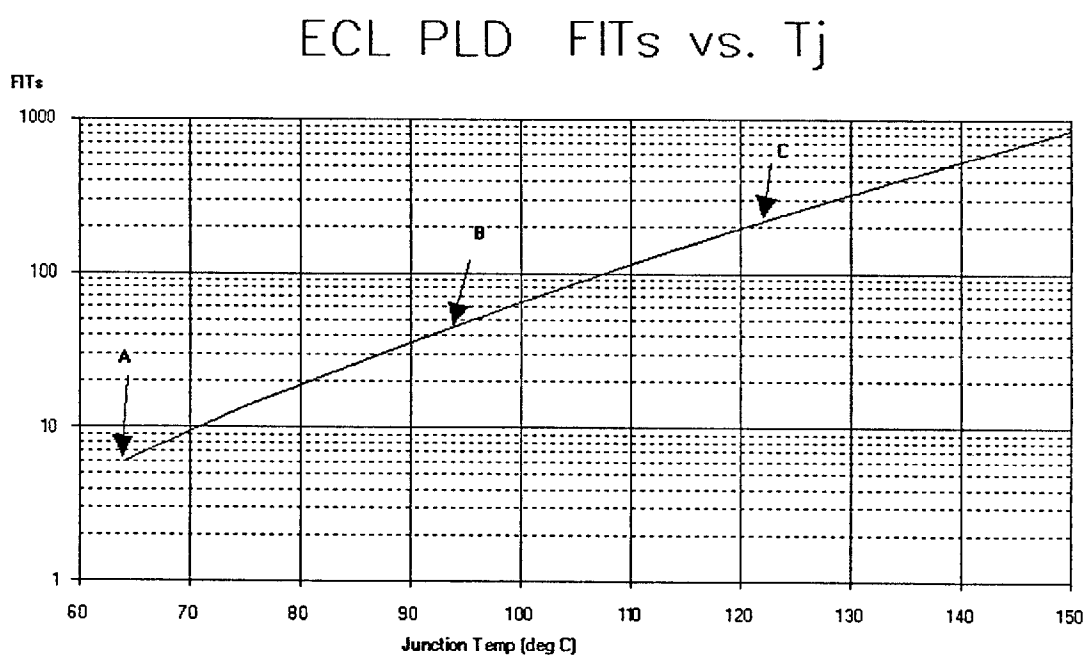


Figure 2. Failures in Time vs Junction Temperature

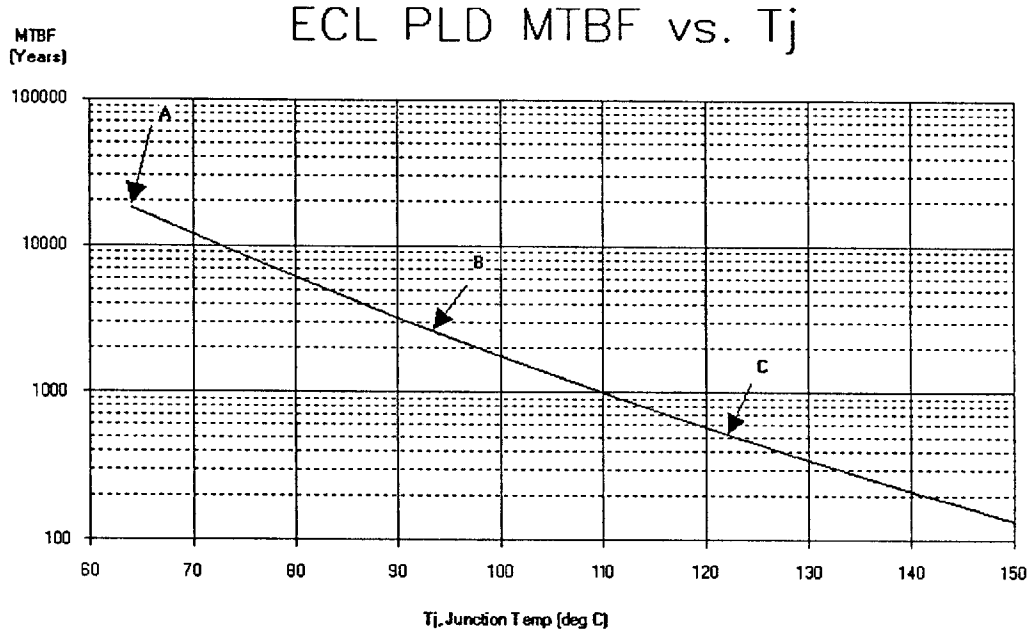


Figure 3. Mean Time Between Failures vs Junction Temp.

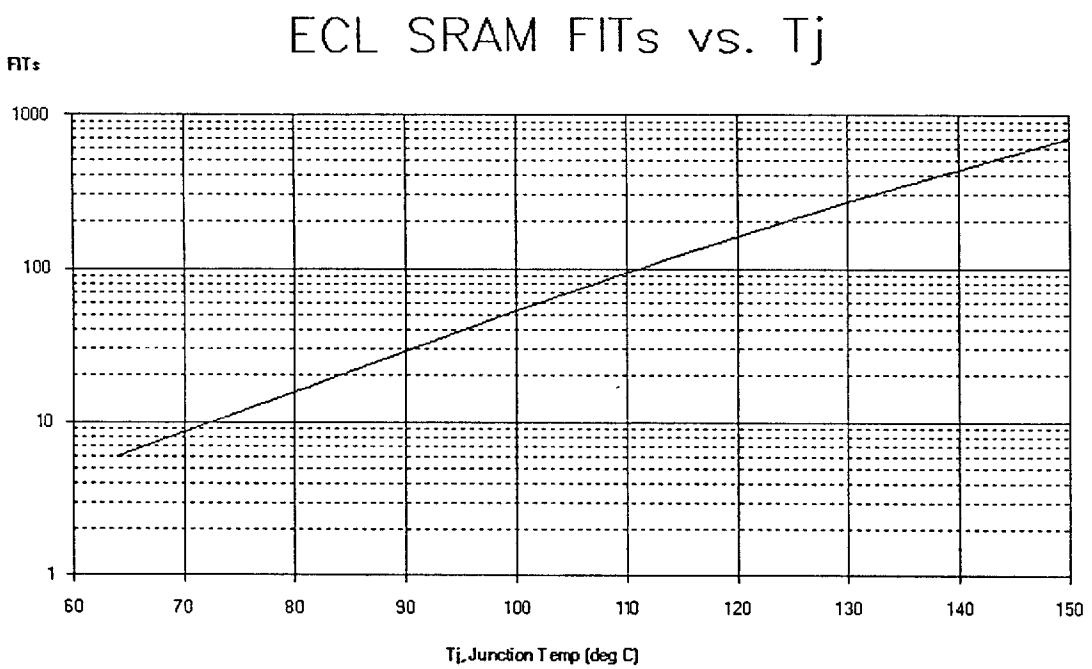


Figure 4. Failures in Time vs Junction Temperature

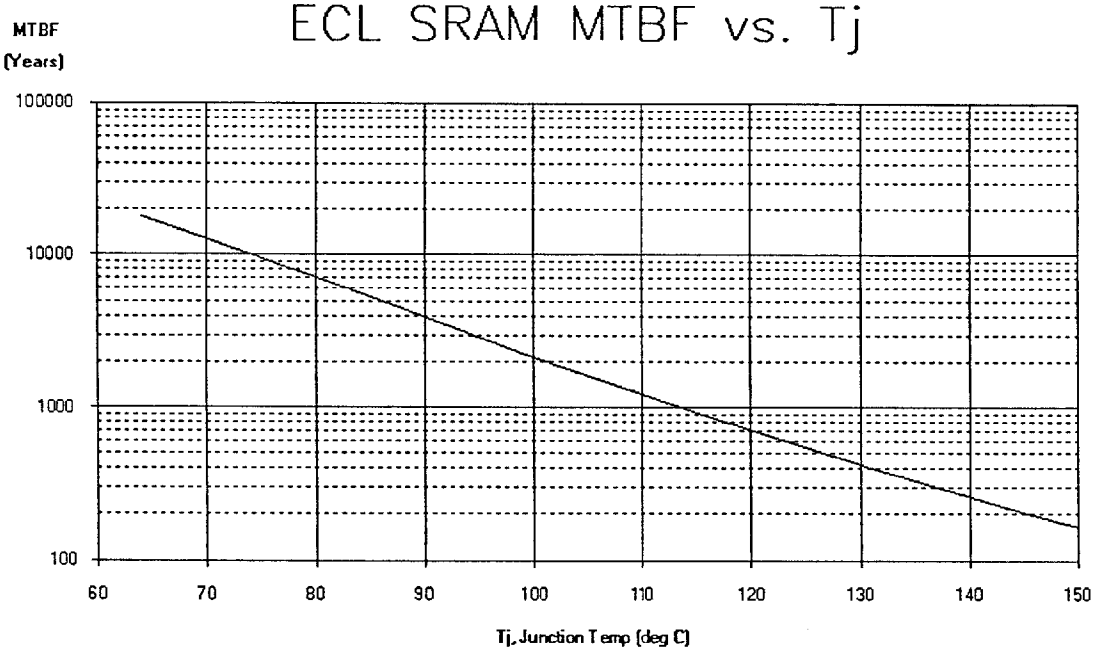


Figure 5. Mean Time Between Failure vs Junction Temp.