DGP303A
Precision Dual SPDT CMOS Analog Switch

FEATURES

- ± 22 Volt Input Range
- 10 Ω Max $\Delta r_{DS(ON)}$ Any Combination Of Switches
- 0.5 nA Max At 25°C, ±15 V
- Tested Δt_{ON} and Δt_{OFF} < 50 ns
- Pin Compatible with DG303A

BENEFITS

- Fully Tested Around ±10.8, ±16.5 And ±22 V Supplies
- Increased Signal Range
- Reduced Switching Errors
- Better Channel-to-Channel Matching
- Simplifies Worst Case Analysis
- Simplifies Upgrades

APPLICATIONS

- Precision Data Acquisition
- Automatic Test Equipment
- Precision Instrumentation
- Radar Systems

DESCRIPTION

The DGP303A is a precision dual single-pole double-throw analog switch designed for critical applications requiring improved performance over that obtainable with the popular DG303A. Produced on an enhanced proprietary high voltage process, the DGP303A has been fully specified with input analog signals to ±22 V, making it an ideal choice for high voltage applications or where the added margin of safety over traditional switches is of importance.

In addition to the low current leakage specifications, $r_{DS(ON)}$, t_{ON} and t_{OFF} have been tested and guaranteed at various input voltages to assure worst-case error analysis. An epitaxial layer prevents latchup.

Packaging for this device includes the 14-pin CerDIP and plastic DIP options. Performance grades include military, A suffix (–55 to 125°C) and industrial, D suffix (–40 to 85°C) temperature ranges. Customers interested in SO packaging should design-in the DG403DY.

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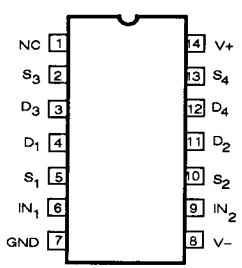
PIN CONFIGURATION

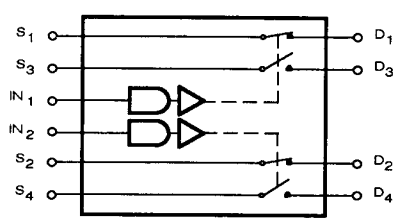
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DGP303AAK
DGP303AAK883
Plastic: DGP303ADJ

FUNCTION BLOCK DIAGRAM



Two SPDT Switches per Package

Truth Table

LOGIC	SWITCH 1,2	SWITCH 3,4
0	OFF	ON
1	ON	OFF

Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 4.0 V

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs V_S, V_D[1] ..... (V-) -2V to (V+) +2V
..... or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
14-Pin Plastic DIP** ..... 450 mW
14-Pin CerDIP*** ..... 900 mW

* All leads welded or soldered to PC board.
** Derate 6 mW /°C above 75°C.
*** Derate 12 mW /°C above 75°C.

1 Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

THE DGP FAMILY OF ANALOG SWITCHES AND MULTIPLEXERS

Siliconix has improved its high-voltage metal-gate CMOS process to allow for lower leakage, higher voltage and lower variation performance. Additionally, through dramatic improvements in automated testing technology, specifications and limits that were previously untestable are now 100% tested and specified on the DGP303A data sheet.

The data sheet specification tables are in a new format as well. The format is that of a military drawing, where all specifications are 100% tested, eliminating any uncertainty about what is actually tested. Many parameters that were previously listed as "typical" or "guaranteed by design" are now 100% tested with minimum and maximum values, so that a worst case design can be realized.

The DGP303A also specified certain parameters that have never been seen on a DG303A standard product data sheet in min/max or typical form. An important example of this is the variation of the switching time over all channels, which is specified with a maximum of 50 ns. The variation of "ON" resistance is similarly specified and 100% tested to be less than 10 Ω over six different drain voltage and source current conditions, over all four channels tested, resulting in 24 different readings. This specification is necessary for determining the worst-case distortion and signal level variation due to differences in channel resistance and "ON" resistance modulation effects. Also note that $r_{DS(ON)}$ is measured at the lower extreme of the voltage operating level, (e.g. ±13.5 V instead of ±15 V) where $r_{DS(ON)}$ is highest.

Leakage currents are specified and tested to new lower limits at both room temperature and over the full temperature range. For example, the industrial range devices' leakages have been reduced from 100 nA (over temp) on the DG303A to 5 nA (over temp) on the DGP version. Additionally, the leakages are specified at the extremes of the operating ranges (e.g. ±16.5 V instead of ±15 V), where the leakages tend to be the highest. This is essential for designs where worst-case leakage must be well known, such as precision instruments and sample-and-hold amplifiers.

The operating range of the DGP303A, up to ±22 V and down to ±10.8 V. This allows the switches to have guaranteed performance limits with power supplies as low as ±12 V (±10%), ±15 V (±10%), and up to ±20 V (±10%).

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]		LIMITS 1=25°C 2=125,85°C 3=−55,−40°C TEMP		A SUFFIX −55 to 125°C MIN [b]	A SUFFIX −55 to 125°C MAX [b]	D SUFFIX −40 to 85°C MIN [b]	D SUFFIX −40 to 85°C MAX [b]	UNIT
SWITCH										
Analog Signal Range [c]	V_{ANALOG}			1,2,3		−15	15	−15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V− = −13.5 V; I_S = 1 mA, V_D = ±10.0 V		1,3 2	30		50 75		50 75	Ω
		V+ = 10.8 V, V− = 10.8 V; I_S = 1 mA, V_D = ±7.5 V; V_{IN} = 0.4 V		1,3 2	40		75 100		75 100	
		V+ = 22 V, V− = −22 V; I_S = 1 mA, V_D = ±15 V		1,3 2	25		40 60		40 60	
Delta Drain-Source ON Resistance	$\Delta r_{DS(ON)}$	V_D = +5, 0, −5 V, I_S = ±1 mA; V_{IN} = 0.8 V Worst Combination		1,3 2	3		10 15		10 15	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V− = −16.5 V	V_S = V_D = 15.5 V	1 2	0.1	−0.5 −60	0.5 60	−0.5 −6	0.5 6	nA
			V_S = V_D = −15.5 V	1 2	0.1	−0.5 −60	0.5 60	−0.5 −6	0.5 6	
		V+ = 22 V, V− = −22 V	V_D = V_S = 21 V	1 2	0.4	−2 −200	2 200	−2 −20	2 20	
			V_D = V_S = −21 V	1 2	0.4	−2 −200	2 200	−2 −20	2 20	
Source OFF Leakage Current	$I_{S(OFF)}$	V+ = 13.5 V, V− = −13.5 V	V_D = −12.5 V, V_S = +12.5 V	1 2	0.1	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
			V_D = +12.5 V, V_S = −12.5 V	1 2	−0.1	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
		V+ = 16.5 V, V− = −16.5 V	V_D = −15.5 V, V_S = +15.5 V	1 2	0.15	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
			V_D = +15.5 V, V_S = −15.5 V	1 2	−0.15	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
		V+ = 22 V, V− = −22 V	V_D = −21 V, V_S = +21 V	1 2	0.2	−2 −100	2 100	−2	2	
			V_D = +21 V, V_S = −21 V	1 2	−0.2	−2 −100	2 100	−2 −10	2 10	
Drain OFF Leakage Current	$I_{D(OFF)}$	V+ = 13.5 V, V− = −13.5 V	V_D = −12.5 V, V_S = +12.5 V	1 2	0.1	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
			V_D = +12.5 V, V_S = −12.5 V	1 2	−0.1	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
		V+ = 16.5 V, V− = −16.5 V	V_D = −15.5 V, V_S = +15.5 V	1 2	0.15	−0.5 −50	0.5 50	−0.5 −5	0.5 5	
			V_D = +15.5 V, V_S = −15.5 V	1 2	−0.15	−0.5 −50	0.5 50	−0.5 −5	0.5 5	

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ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]		LIMITS 1=25°C 2=125,85°C 3=−55,−40°C TEMP	TYP [d]	A SUFFIX −55 to 125°C MIN [b]	A SUFFIX −55 to 125°C MAX [b]	D SUFFIX −40 to 85°C MIN [b]	D SUFFIX −40 to 85°C MAX [b]	UNIT
SWITCH (Cont'd)										
Drain OFF Leakage Current	$I_{D(OFF)}$	V+ = 22 V, V− = −22 V	V_D = −21 V, V_S = +21 V	1	0.2	−2	2	−2	2	nA
				2		−100	100	−10	10	
			V_D = +21 V, V_S = −21 V	1	−0.2	−2	2	−2	2	
				2		−100	100	−10	10	
INPUT										
Input current with V_{IN} HIGH	I_{IH}	V+ = 22 V, V− = −22 V, V_{IN} under test = 5 V		1	0.005	−0.5	0.5	−0.5	0.5	µA
				2		−5	5	−5	5	
		V+ = 22 V, V− = −22 V, V_{IN} under test = 22 V		1	0.005	−0.5	0.5	−0.5	0.5	
				2		−5	5	−5	5	
Input current with V_{IN} LOW	I_{IL}	V+ = 22 V, V− = −22 V, V_{IN} under test = 0 V		1	0.005	−0.5	0.5	−0.5	0.5	
				2		−5	5	−5	5	
DYNAMIC										
Turn-ON Time	t_{ON}	See Switching Time Test Circuits		1,3	150		300		300	ns
				2			400		400	
Turn-OFF Time	t_{OFF}			1,3	130		250		250	
				2			350		350	
Delta t_{ON}	Δt_{ON}	Worst Combination among channels of the t_{ON} measurements		1,3	30		50		50	
				2			100		100	
Delta t_{OFF}	Δt_{OFF}	Worst Combination among channels of the t_{OFF} measurements		1,3	30		50		50	
				2			100		100	
Charge Injection	Q	R_{gen} = 0Ω, C_L = 10 nF	V_{gen} = 0 V	1	35					pC
			V_{gen} = ±10 V	1	45					
Source OFF Capacitance [d]	$C_{S(OFF)}$	f = 1 MHz, V_S = 0 V		1	14					pF
Drain OFF Capacitance [d]	$C_{D(OFF)}$	f = 1 MHz, V_S = 0 V		1	14					pF
Channel ON Capacitance [d]	$C_{D+S(ON)}$			1	40					
Crosstalk (Channel-to-Channel)		R_L = 75Ω, C_L = 5 pF, f = 1 MHz		1	64					dB
OFF Isolation		R_L = 75Ω, C_L = 5 pF, f = 1 MHz		1	56					

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SUPPLY									
Positive Supply Current	I+	V_{IN} (One Input) = 4V, All Others = 0 V, $V\pm$ = ±16.5 V	1 2	0.45		0.6 1		0.6 1	mA
		V_{IN} = 0.8 V, All Inputs, $V\pm$ = ±16.5 V	1 2	0.001		10 100		10 100	µA
Negative Supply Current	I-	V_{IN} (One Input) = 4 V, All Others = 0 V, $V\pm$ = ±16.5 V	1 2	-0.001	-10 -100		-10 -100		µA
		V_{IN} = 0.8 V, All Inputs, $V\pm$ = ±16.5 V	1 2	-0.001	-10 -100		-10 -100		µA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.

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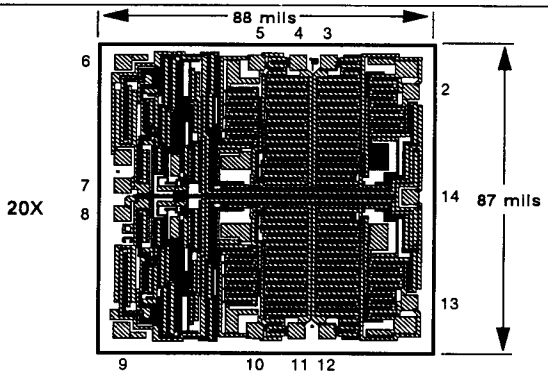
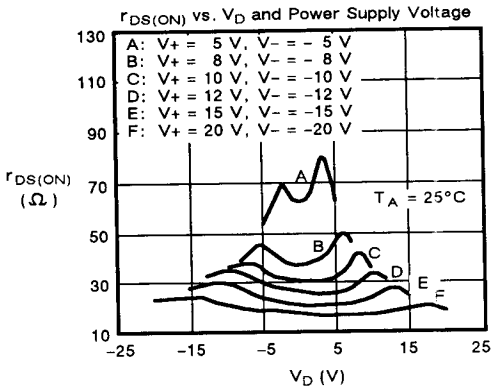
DIE TOPOGRAPHY

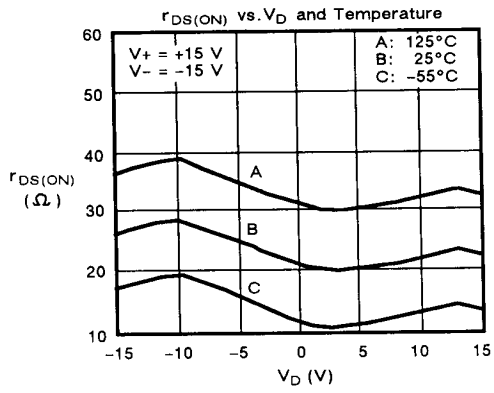


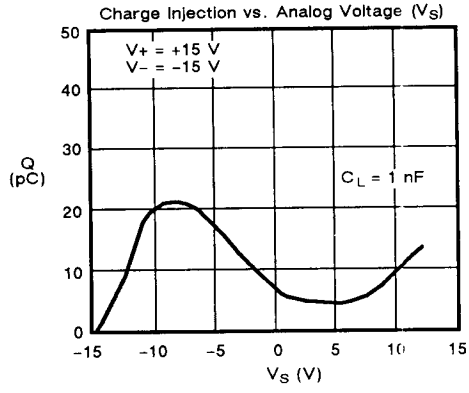
ICMJC
8 Capacitors
2 Resistors
22 P-channel depletion MOSFETs
30 N-channel depletion MOSFETs
4 Diodes

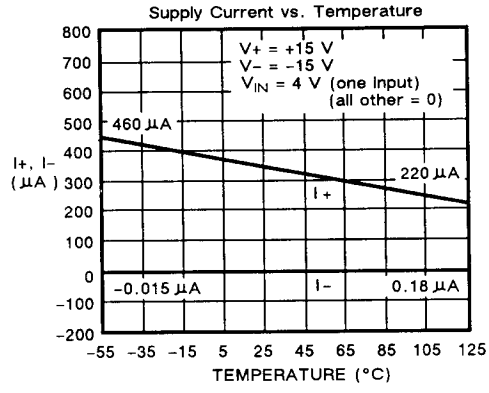
Pad No.	Function
2	Source 3
3	Drain 3
4	Drain 1
5	Source 1
6	Input 1
7	Ground
8	V-
9	Input 2
10	Source 2
11	Drain 2
12	Drain 4
13	Source 4
14	V+ (Substrate)

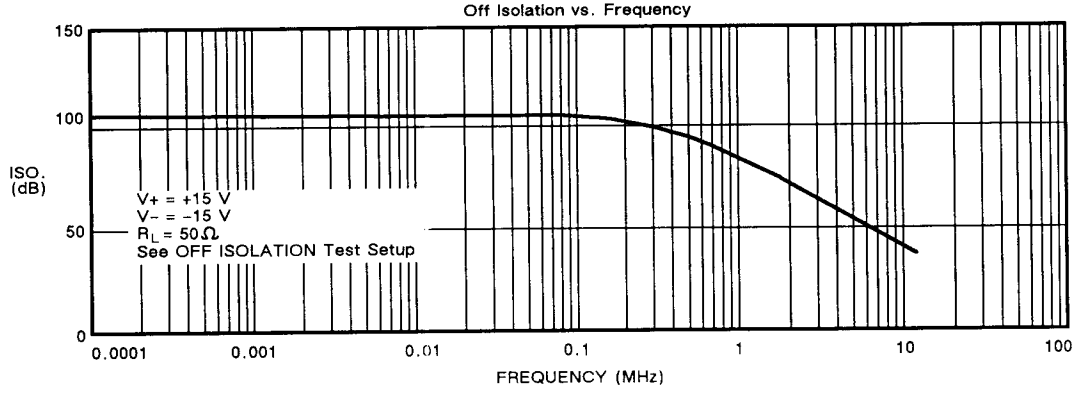
TYPICAL CHARACTERSITICS





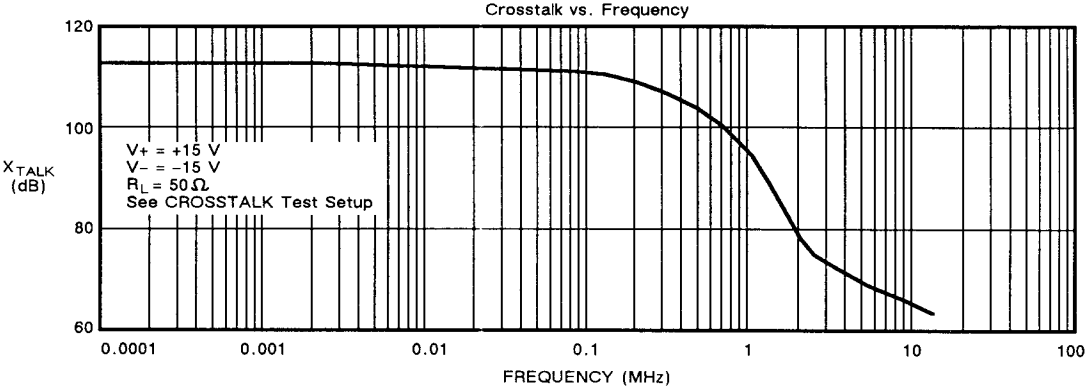




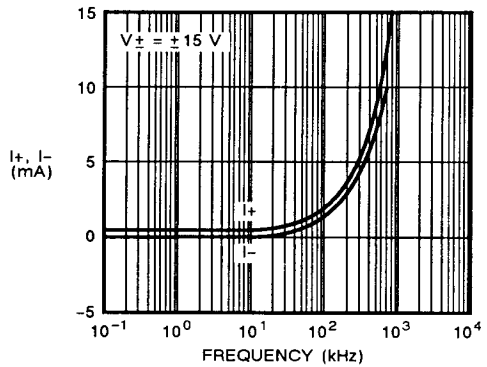


TYPICAL CHARACTERSITICS

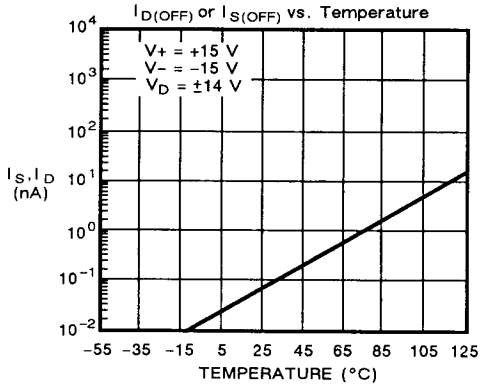
Crosstalk vs. Frequency



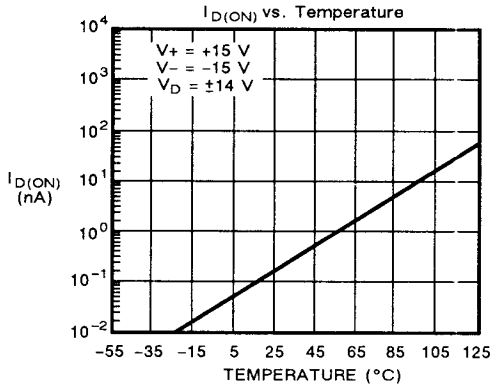
Supply Currents vs. Switching Frequency



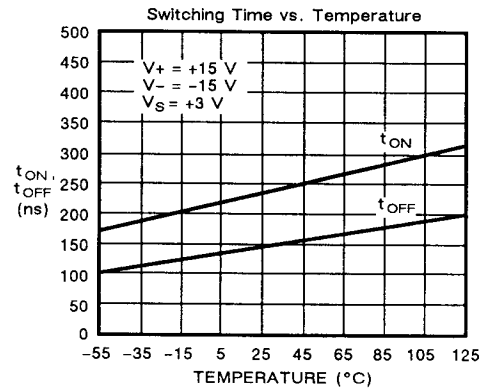
$I_{D(OFF)}$ or $I_{S(OFF)}$ vs. Temperature



$I_{D(ON)}$ vs. Temperature



Switching Time vs. Temperature



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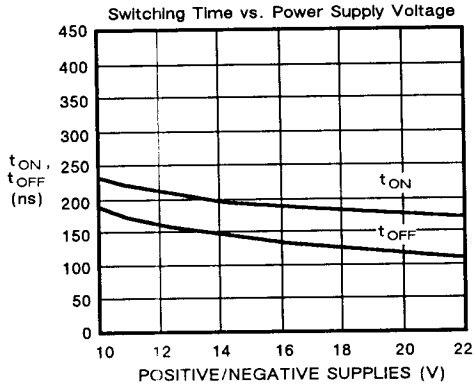
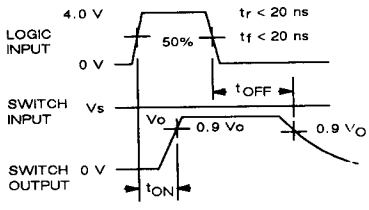
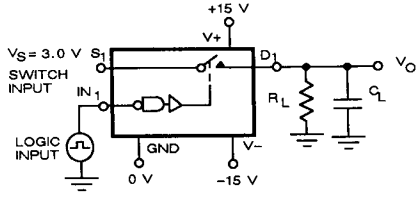
TYPICAL CHARACTERSITICS



SWITCHING TIME TEST CIRCUITS

V_O is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

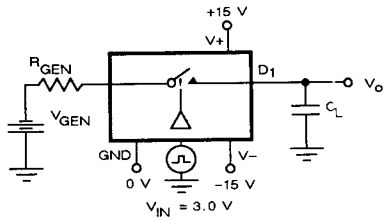


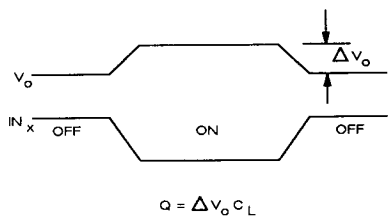


For load conditions, See Electrical Characteristics
C_L (includes fixture and stray capacitance)

$$V_o = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

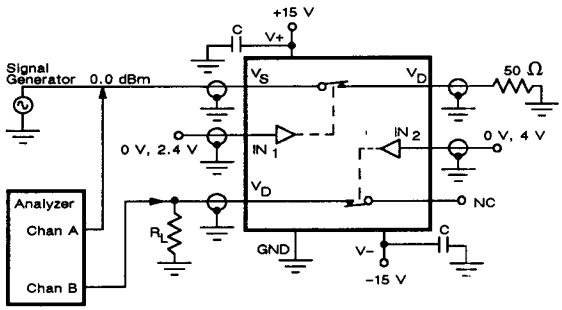
CHARGE INJECTION TEST CIRCUIT





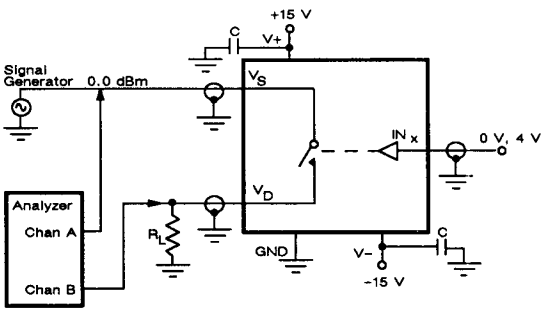
$Q = \Delta V_o C_L$

CROSSTALK TEST CIRCUIT



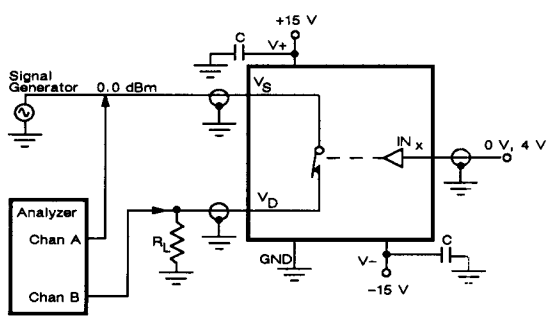
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

OFF ISOLATION TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

INSERTION LOSS TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

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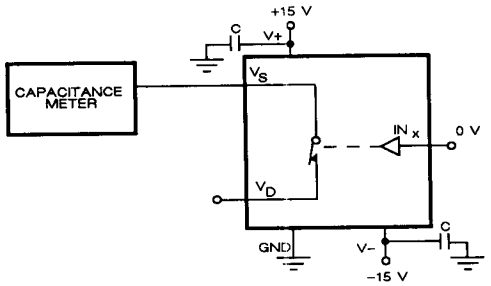
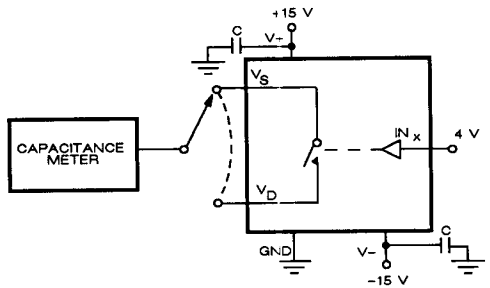
SOURCE/DRAIN ON CAPACITANCE



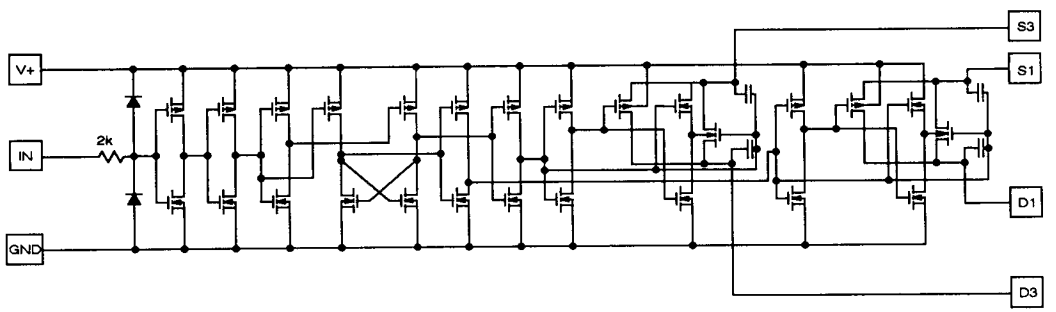
METER
BOONTON 72BD Capacitance Meter or equivalent

SOURCE/DRAIN OFF CAPACITANCE

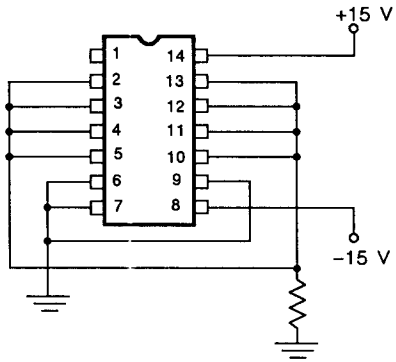


METER
BOONTON 72BD Capacitance Meter or equivalent

SCHEMATIC DIAGRAM (Typical Channel)



BURN-IN CIRCUIT

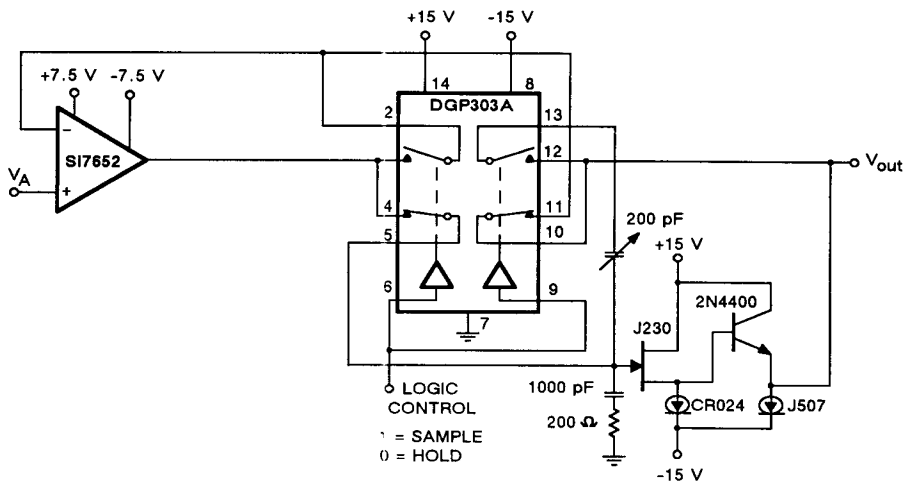


Note: All Resistors are 10 kΩ unless otherwise specified

APPLICATION HINTS

The figure below shows a precision sample-and-hold amplifier using the DGP303A. The errors contributed by the analog switch are mostly attributed to charge injection and leakage. Charge injection causes a dc offset to appear on the holding capacitor.

The low leakage of the DGP303A reduces the droop rate of the sample and hold.



Precision Sample & Hold