DGP508A
Precision 8-Channel CMOS Multiplexer/Demultiplexer

Siliconix incorporated

T-51-11

FEATURES

- Fully Tested Around ±10.8, ±16.5 and ± 20 V Supplies
- 10% (Max.) delta $r_{DS(ON)}$
- 2.0 nA (Max.) Leakage at 25°C, ±16.5 V
- Low Charge Injection (Q < 15 pC)
- Pin-Compatible with DG508A

BENEFITS

- Simplifies Worst-Case Analysis
- Reduces Channel-to-Channel Variations
- Reduces Switching Errors
- Reduces Switching Noise
- Simplifies Upgrading

APPLICATIONS

- Automatic Test Equipment
- Communication Systems
- Precision Data Acquisition
- Precision Instrumentation
- Upgrading Old Designs

DESCRIPTION

The DGP508A is a precision 8-channel CMOS analog multiplexer/demultiplexer which is specified with improved static and dynamic performance limits. The DGP508A features tighter leakage and delta $r_{DS(ON)}$ limits and wider analog signal ranges than the industry-standard DG508A, yet maintains 100% pin and functional compatibility. This allows for precision system performance upgrading without redesign or layout of circuit boards. In addition, the specification limits and associated test conditions are in a military drawing format, simplifying source-control documentation and ensuring performance based upon a worst-case analysis. Refer to the "Detailed Description" for more information on the "DGP" family.

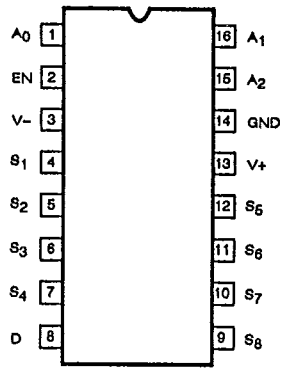
Produced on a proprietary high-voltage CMOS process, the DGP508A has been fully specified for signals up to ±20 V, making it an ideal choice for extended range operation, or in systems with additional headroom requirements. An epitaxial layer prevents latchup.

The DGP508A is available in a 16-pin plastic DIP for the industrial, D suffix (–40 to 85°C) temperature range and the CerDIP for military (available with /883 processing), A suffix (–55 to 125°C) temperature operation.

For more information on the DGP508A, please refer to Siliconix Technical Article TA87-1.

PIN CONFIGURATION

Dual-In-Line Package



Top View

Order Numbers:
CerDIP:
DGP508AAK
DGP508AAK/883
Plastic:
DGP508ADJ

TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{AL} < 0.8 V
Logic "1" = V_{AH} > 2.4 V

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FUNCTIONAL BLOCK DIAGRAM

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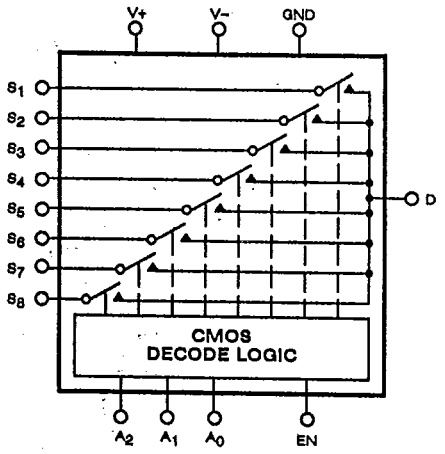

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs V_S, V_D[1] ..... (V-) -2 V to (V+) +2 V

..... or 30 mA, whichever occurs first

Current (Any Terminal) Continuous ..... 30 mA

Current (S or D) Pulsed 1 ms 10% duty ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin CerDIP*** ..... 900 mW
16-Pin Small Outline**** ..... 900 mW

* All leads welded or soldered to PC board.
** Derate 6 mW/°C above 75°C.
*** Derate 12 mW/°C above 75°C.
**** Derate 7.7 mW/°C above 75°C.

1 Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V, V_{EN} = 2.4 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH									
Drain-Source[e] ON Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V- = -13.5 V, I_S = 1 mA, V_D = ±10.0 V	1,3	265		400		400	Ω
			2			500		500	
		V+ = 10.8 V, V- = 10.8 V, I_S = 1 mA, V_D = ±7.5 V, V_{IN} = 0.4 V	1,3	300		450		450	
			2			550		550	
		V+ = 20 V, V- = -20 V, I_S = 1 mA, V_D = ±15 V	1,3	200		350		350	
			2			450		450	
Delta Drain-Source[e] ON Resistance	$\Delta r_{DS(ON)}$	V_D = +5, 0, -5 V, I_S = ±1 mA, V_{IN} = 0.8 V, Worst Combination	1	20		40		40	
			2,3			50		50	

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ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V, V_{EN} = 2.4 V		LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
				TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH (Cont'd)										
Source OFF Leakage Current	$I_{S(OFF)}$	V+ = 13.5 V, V- = -13.5 V	V_D = -12.5 V, V_S = +12.5 V	1	0.01	-0.25	0.25	-0.25	0.25	nA
				2		-10	10	-2	2	
			V_D = +12.5 V, V_S = -12.5 V	1	-0.01	-0.25	0.25	-0.25	0.25	
				2		-10	10	-2	2	
		V+ = 16.5 V, V- = -16.5 V	V_D = -15.5 V, V_S = +15.5 V	1	0.01	-0.25	0.25	-0.25	0.25	
				2		-10	10	-2	2	
			V_D = +15.5 V, V_S = -15.5 V	1	-0.01	-0.25	0.25	-0.25	0.25	
				2		-10	10	-2	2	
		V+ = 20 V, V- = -20 V	V_D = -19 V, V_S = +19 V	1	0.03	-1	1	-1	1	
				2		-50	50	-10	10	
			V_D = +19 V, V_S = -19 V	1	-0.03	-1	1	-1	1	
				2		-50	50	-10	10	
		V_D = -5 V, V_S = +5 V		2		-5	5	-2	2	
		V_D = +5 V, V_S = -5 V		2		-5	5	-2	2	
Drain OFF Leakage Current	$I_{D(OFF)}$	V+ = 13.5 V, V- = -13.5 V	V_D = -12.5 V, V_S = +12.5 V	1	0.08	-2	2	-2	2	
				2		-100	100	-20	20	
			V_D = +12.5 V, V_S = -12.5 V	1	-0.08	-2	2	-2	2	
				2		-100	100	-20	20	
		V+ = 16.5 V, V- = -16.5 V	V_D = -15.5 V, V_S = +15.5 V	1	0.10	-2	2	-2	2	
				2		-100	100	-20	20	
			V_D = +15.5 V, V_S = -15.5 V	1	-0.10	-2	2	-2	2	
				2		-100	100	-20	20	
		V+ = 20 V, V- = -20 V	V_D = -19 V, V_S = +19 V	1	0.25	-5	5	-5	5	
				2		-200	200	-50	50	
			V_D = +19 V, V_S = -19 V	1	-0.25	-5	5	-5	5	
				2		-200	200	-50	50	
		V_D = -5 V, V_S = +5 V		2		-50	50	-20	20	
		V_D = +5 V, V_S = -5 V		2		-50	50	-20	20	
Channel ON[e] Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V- = -16.5 V	V_D = +15.5 V, V_S = +15.5 V	1	0.10	-2	2	-2	2	
				2		-100	100	-20	20	
			V_D = -15.5 V, V_S = -15.5 V	1	-0.10	-2	2	-2	2	
				2		-100	100	-20	20	
		V+ = 20 V, V- = -20 V	V_D = +19 V, V_S = +19 V	1	0.25	-5	5	-5	5	
				2		-200	200	-50	50	
			V_D = -19 V, V_S = -19 V	1	-0.25	-5	5	-5	5	
				2		-200	200	-50	50	

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ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V, V_{EN} = 2.4 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SWITCH (Cont'd)									
Channel ON [e] Leakage Current (Continued)	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = +5 V, V_S = +5 V	2		-50	50	-20	20	nA
		V_D = -5 V, V_S = -5 V	2		-50	50	-20	20	
SUPPLY									
Positive Supply Current	I_+	V_{IN} = 2.4 V, V_A = 0 or 2.4 V, V± = ±16.5 V	1,2,3	1.3		2.4 3		2.4 3	mA
	$I_{+\,STANDBY}$		1,2,3	1.3		2.4 3		2.4 3	
Negative Supply Current	I_-		1,2,3	-0.65	-1.5 -2		-1.5 -2		
	$I_{-\,STANDBY}$		1,2,3	-0.65	-1.5 -2		-1.5 -2		
INPUT									
Input Current With V_{IN} High	I_{AH}	V+ = 20 V, V- = -20 V, V_{IN} under test = 2.4 V	1,2	-0.001	-0.5	0.5	-0.5	0.5	µA
		V+ = 20 V, V- = -20 V, V_{IN} under test = 20 V	1,2	0.004	-0.5	0.5	-0.5	0.5	
Input Current With V_{IN} Low	I_{AL}	V+ = 20 V, V- = -20 V, V_{IN} under test = 0 V	1,2	0.01	-0.5	0.5	-0.5	0.5	
DYNAMIC									
Enable Turn-ON Time	$t_{ON(EN)}$	See Switching Time Test Circuits	1,3 2	750		1000 1500		1000 1500	ns
Enable Turn-OFF Time	$t_{OFF(EN)}$		1,3 2	350		1000 1500		1000 1500	
Multiplexer Switching Time	t_{TRANS}		1,3 2	700		1000 1500		1000 1500	
Break-Before-Make Interval	t_{OPEN}		1	450	50		50		
Charge Injection	Q	R_{gen} = 0Ω, C_L = 10 nF, V_{gen} = 0 V	1	5.5		15		15	pC
		V_{gen} = ±10 V	1	7		20		20	

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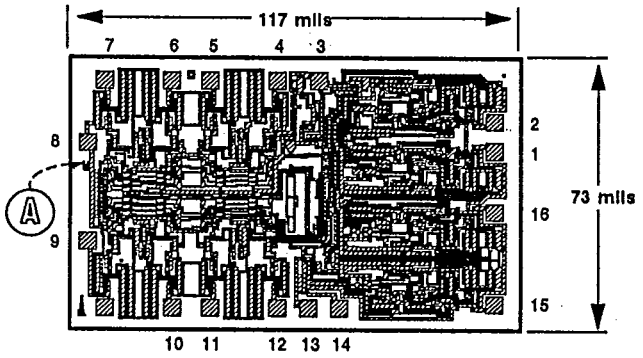
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V, V_{EN} = 2.4 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC (Cont'd)									
Source OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	1	5					pF
Drain OFF Capacitance	$C_{D(OFF)}$		1	25					
Drain and Source ON Capacitance	$C_{S(ON)} + C_{D(ON)}$		1	30					
Crosstalk		f = 100 kHz	1	-60					dB
OFF Isolation			1	-60					
Insertion Loss			1	-1.6					

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.

DIE TOPOGRAPHY



ICMGA
4 Capacitors
7 Resistors
12 Diodes
85 P-channel enhancement MOSFETs
89 N-channel enhancement MOSFETs

Pad No.	Function
1	Address 0
2	Enable
3	V-
4	Source 1
5	Source 2
6	Source 3
7	Source 4
8	Drain
9	Source 8
10	Source 7
11	Source 6
12	Source 5
13	V+ (Substrate)
14	Ground
15	Address 2
16	Address 1

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$t_{ON(EN)}$ AND $t_{OFF(EN)}$ TEST CIRCUIT

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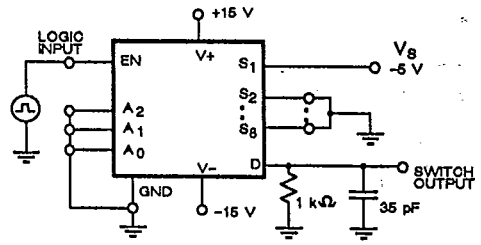
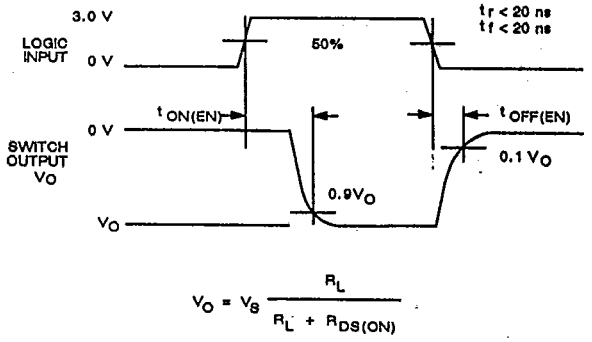
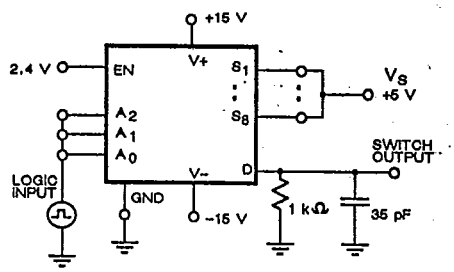
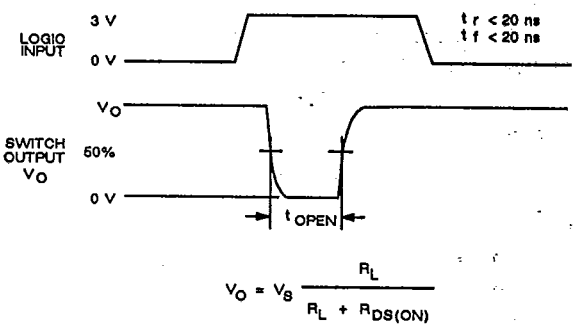


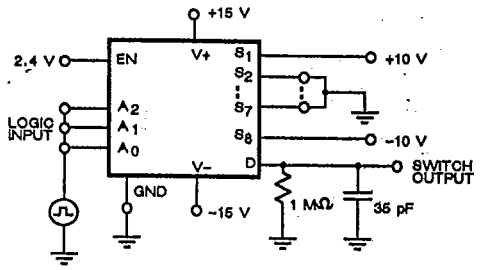


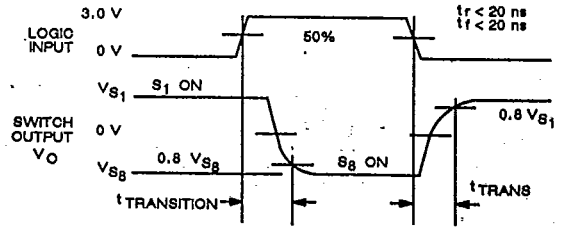
t_{OPEN} TEST CIRCUIT





$t_{TRANSITION}$ TEST CIRCUIT





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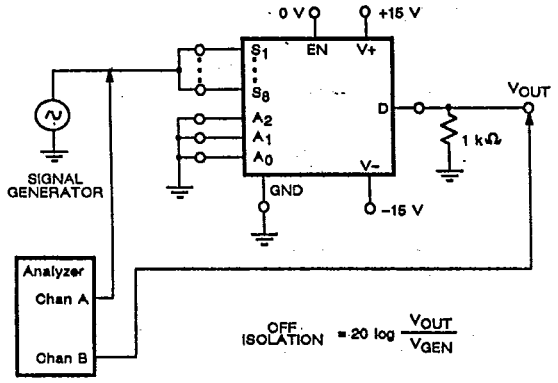
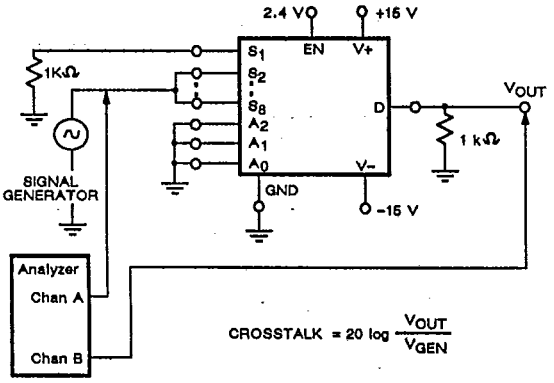
OFF ISOLATION TEST CIRCUIT



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_{GEN}}$$

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

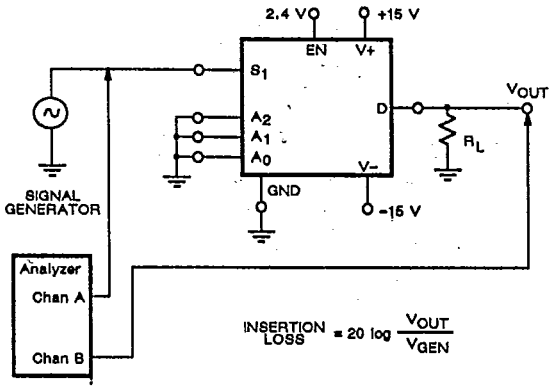
CROSSTALK TEST CIRCUIT



$$\text{CROSSTALK} = 20 \log \frac{V_{OUT}}{V_{GEN}}$$

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

INSERTION LOSS TEST CIRCUIT



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT}}{V_{GEN}}$$

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

DRAIN ON CAPACITANCE

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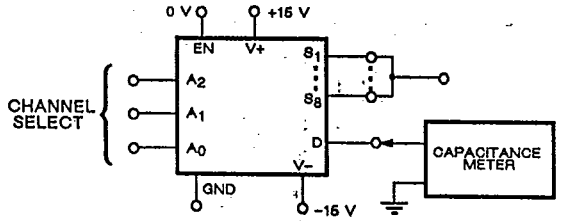
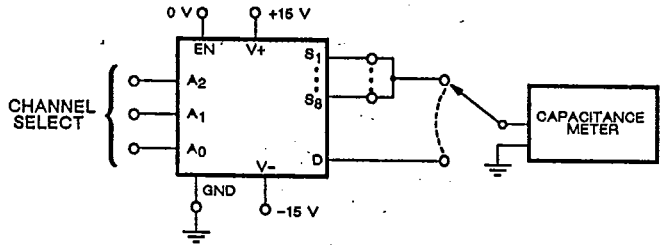


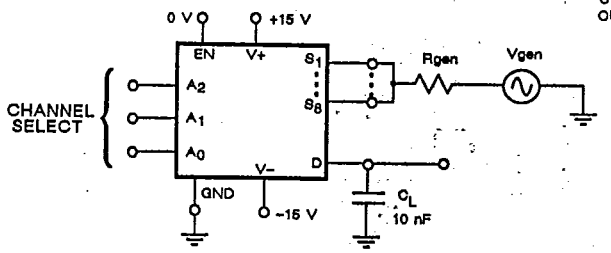
METER
BOONTON 72BD Capacitance Meter or equivalent

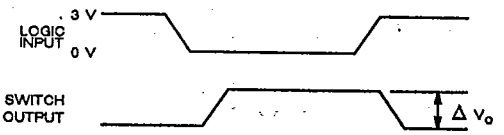
SOURCE/DRAIN OFF CAPACITANCE



METER
BOONTON 72BD Capacitance Meter or equivalent

CHARGE TRANSFER ERROR





Δ Vo is the measured voltage due to charge transfer error, Q

$$Q = C_L \times \Delta V_o$$

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SCHEMATIC DIAGRAM

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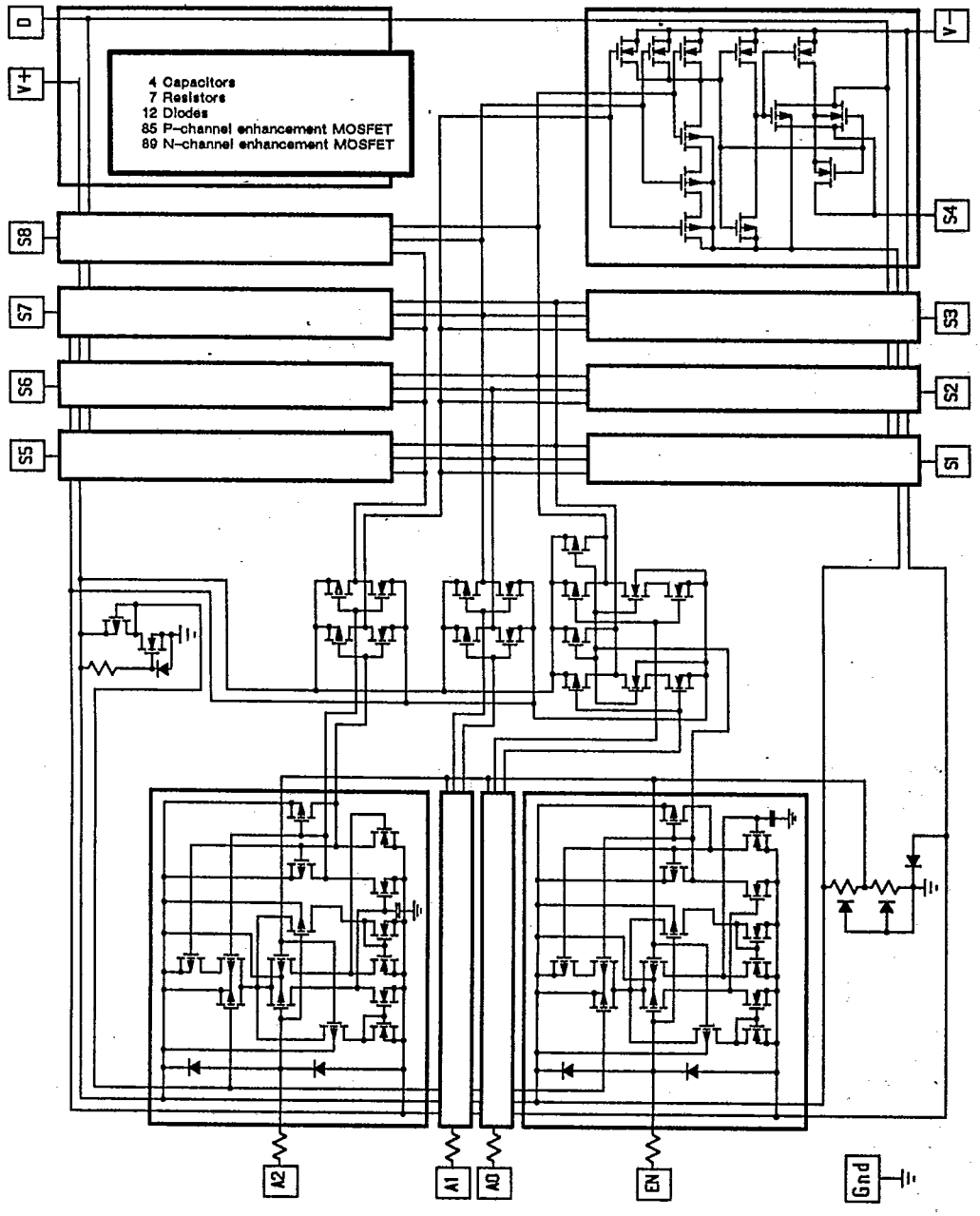

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TYPICAL CHARACTERISTICS

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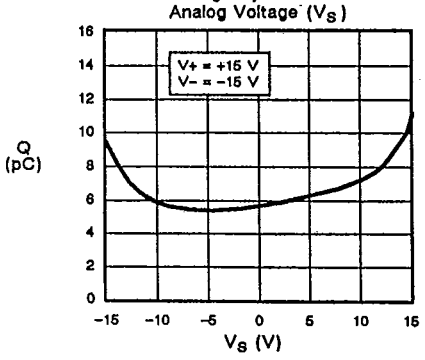
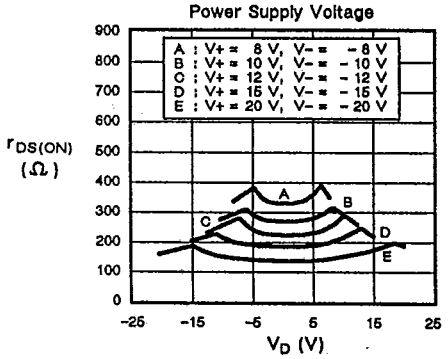
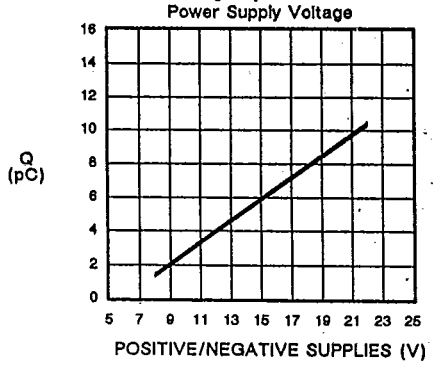
Charge Injection vs. Analog Voltage (V_S)



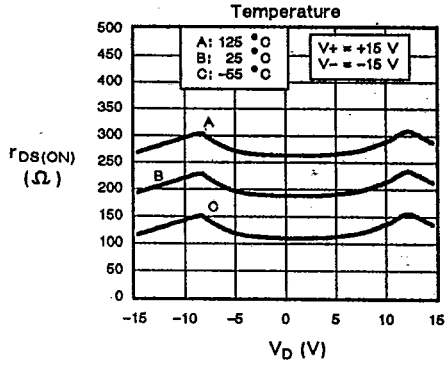
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



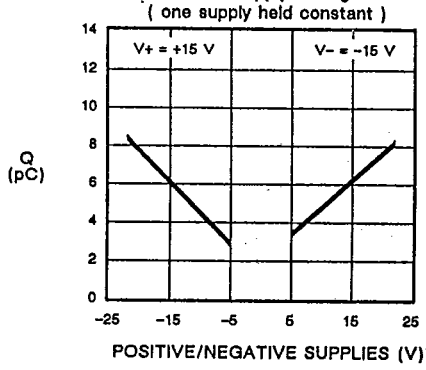
Charge Injection vs. Power Supply Voltage



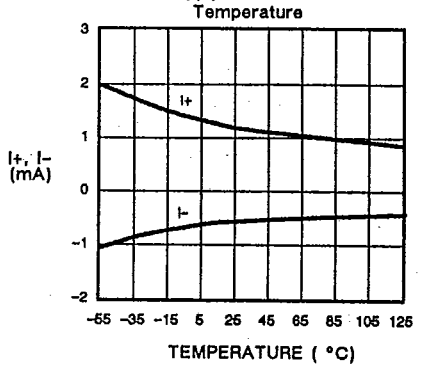
$r_{DS(ON)}$ vs. V_D and Temperature



Charge Injection vs. Power Supply Voltage (one supply held constant)



Supply Current vs. Temperature



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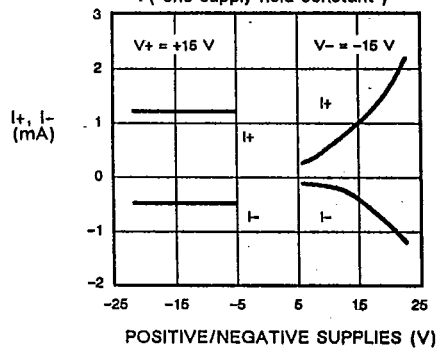
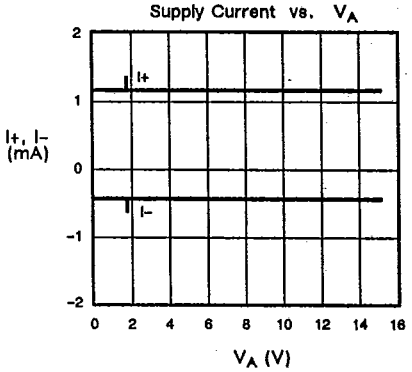
TYPICAL CHARACTERISTICS (Cont'd)

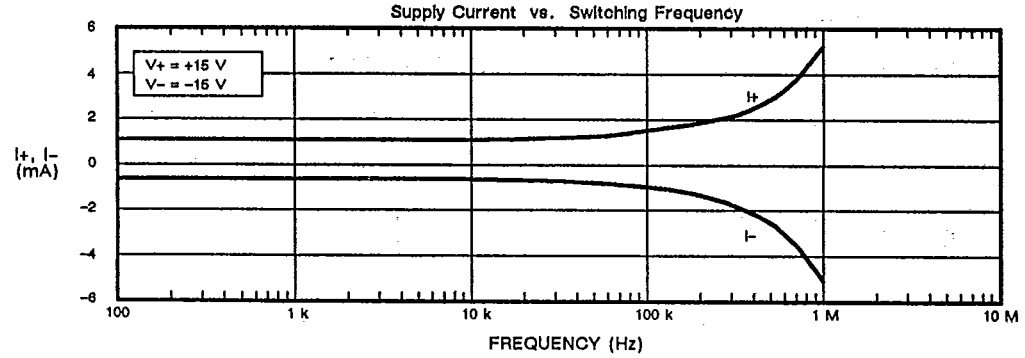
Supply Current vs. Supply Voltage
(one supply held constant)



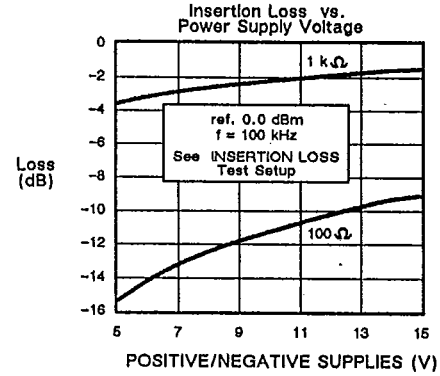
Supply Current vs. V_A



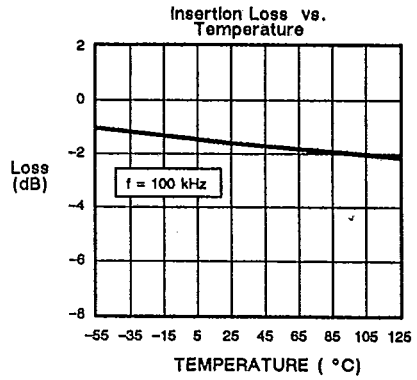
Supply Current vs. Switching Frequency



Insertion Loss vs. Power Supply Voltage

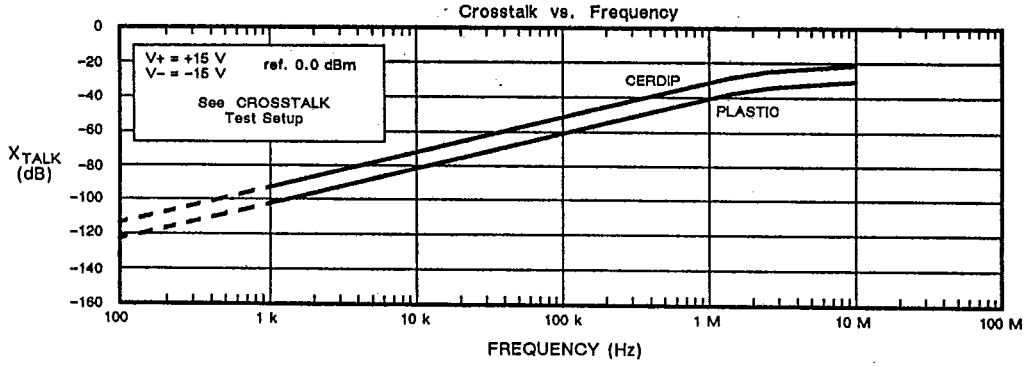


Insertion Loss vs. Temperature

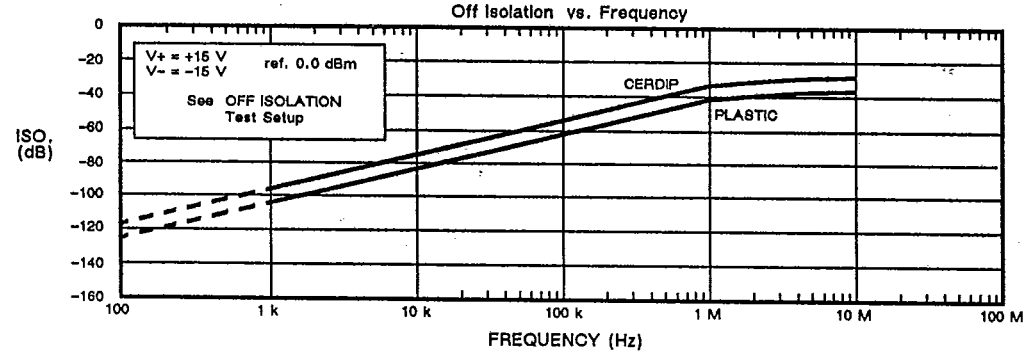


TYPICAL CHARACTERISTICS (Cont'd)

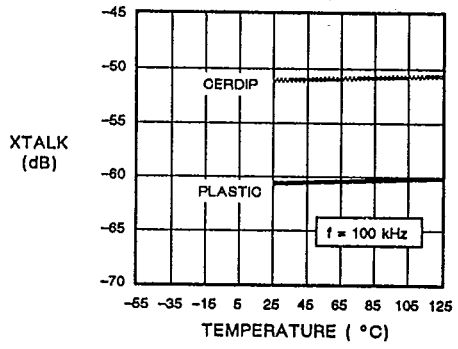
Crosstalk vs. Frequency



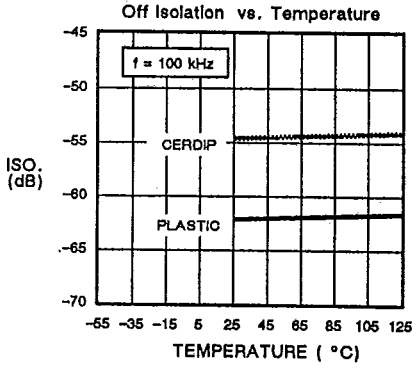
Off Isolation vs. Frequency



Crosstalk vs. Temperature



Off Isolation vs. Temperature



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DGP508A

Siliconix incorporated

TYPICAL CHARACTERISTICS (Cont'd)

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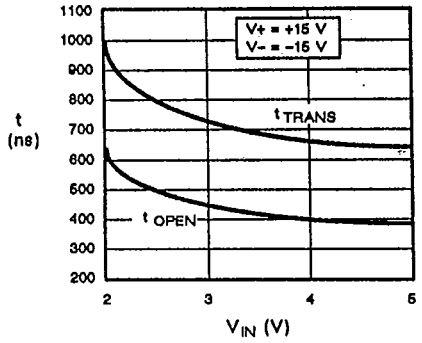
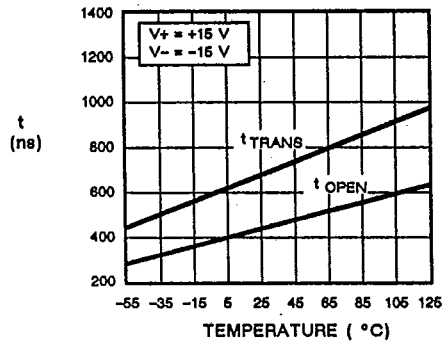
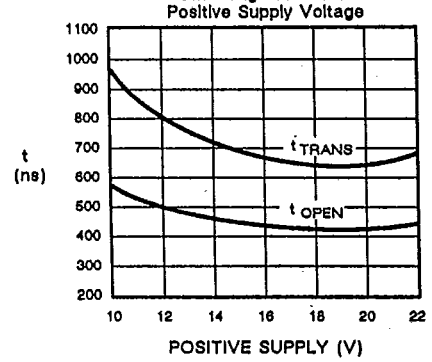
Switching Time vs. Input Logic Voltage (V_A)



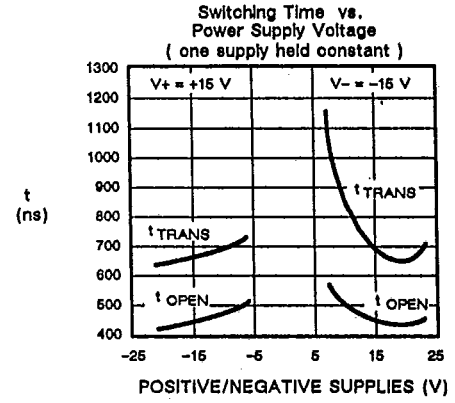
Switching Time vs. Temperature



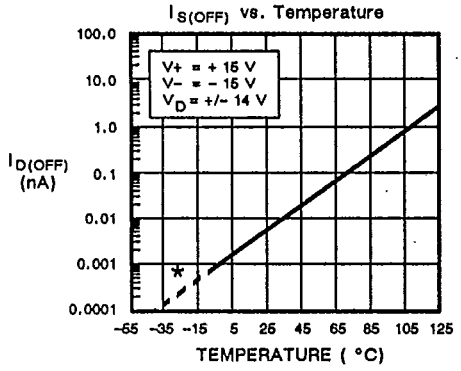
Switching Time vs. Positive Supply Voltage



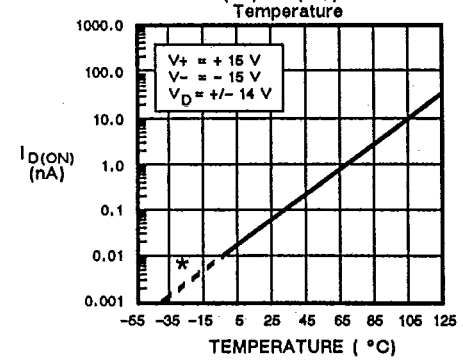
Switching Time vs. Power Supply Voltage (one supply held constant)



$I_{S(OFF)}$ vs. Temperature



$I_{D(ON)}$, $I_{D(OFF)}$ vs. Temperature

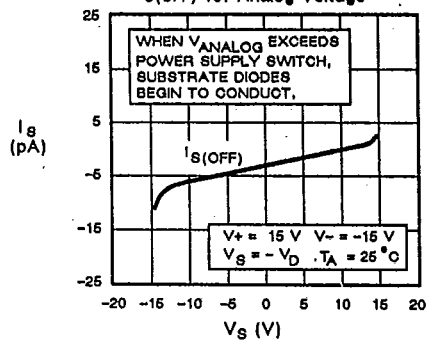


* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

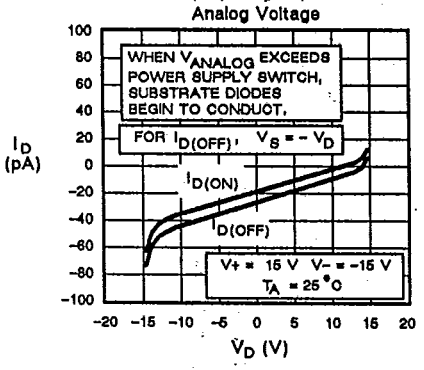
TYPICAL CHARACTERISTICS (Cont'd)

T-51-11

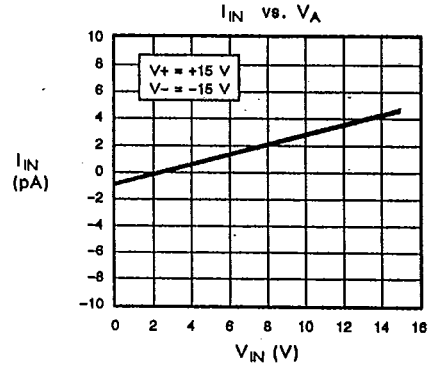
$I_{S(OFF)}$ vs. Analog Voltage



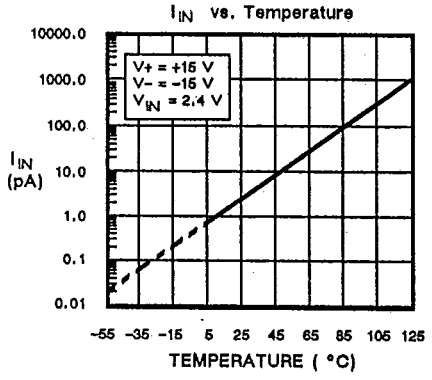
$I_{D(ON)}$, $I_{D(OFF)}$ vs. Analog Voltage



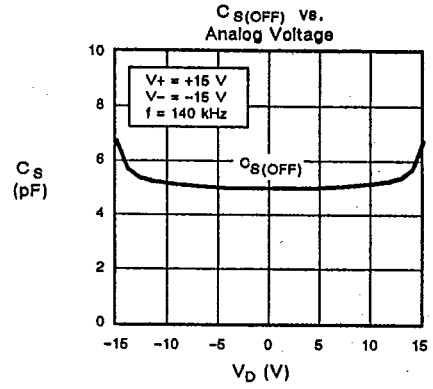
I_{IN} vs. V_A



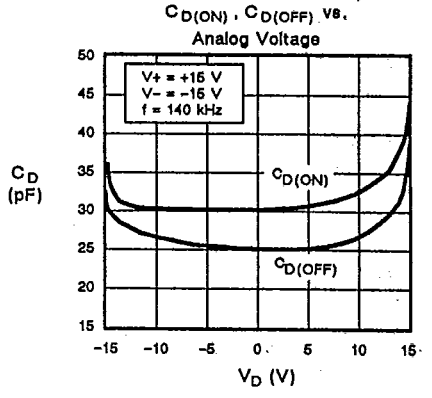
I_{IN} vs. Temperature



$C_{S(OFF)}$ vs. Analog Voltage



$C_{D(ON)}$, $C_{D(OFF)}$ vs. Analog Voltage



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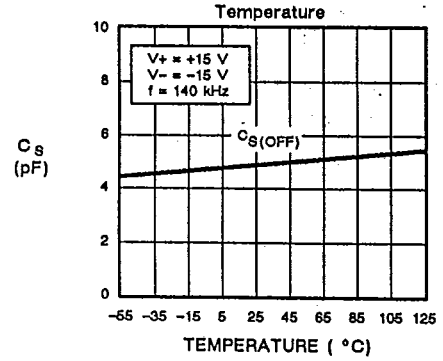
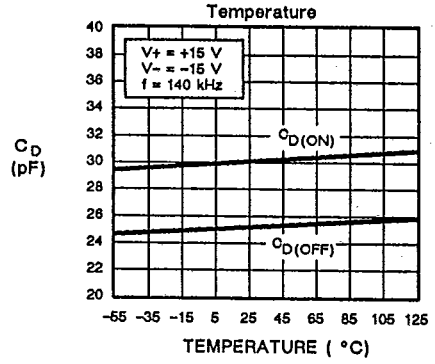
TYPICAL CHARACTERISTICS (Cont'd)

T-51-11

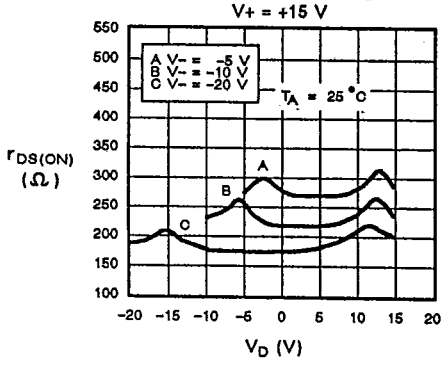
$C_{S(OFF)}$ vs. Temperature



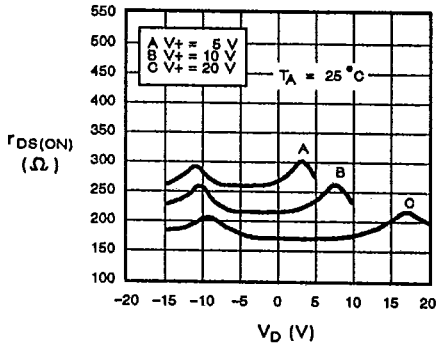
$C_{D(ON)}$, $C_{D(OFF)}$ vs. Temperature



$r_{DS(ON)}$ vs. V_D and Negative Supply Voltage V+ = +15 V



$r_{DS(ON)}$ vs. V_D and Positive Supply Voltage V- = -15 V



DETAILED DESCRIPTION

The DGP Family Of Analog Switches And Multiplexers

Siliconix has improved its high voltage metal-gate CMOS process to allow for lower leakage, higher voltage and lower variation performance. Additionally, through dramatic improvements in automated testing technology, specifications and limits that were previously untestable are now 100% tested and specified on the DGP508A data sheet.

The data sheet specification tables are in a new format as well. The format is that of a military drawing, where all min/max specifications are 100% tested, eliminating any uncertainty about what is actually tested. Many parameters that were previously listed as "typical" or "guaranteed by design" are now 100% tested with minimum and maximum values, so that a worst-case design can be realized.

For example, charge transfer error (or charge injection) was listed only as a typical value in the standard DG508/509A data sheet, and no maximum value was guaranteed. A maximum limit of 20 pC has been established on the data sheet, and this value is 100% tested. This allows the design engineer to design precision switching circuits, such as sample-and-hold amplifiers, with fixed limits for the charge compensation circuit.

DETAILED DESCRIPTION (Cont'd)

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The DGP508A data sheet also specifies parameters that previously have never been specified. An example is the variation in switching time over all channels, specified to a 50 ns maximum. The variation of ON resistance is similarly specified and 100% tested to be less than 40 Ω over six different drain voltage and source current conditions, over all four channels tested, resulting in 48 different readings. This specification is necessary for determining the worst-case distortion and signal level variation due to differences in channel resistance and ON resistance modulation effects. Also note that $r_{DS(ON)}$ is measured at the lower extreme of the voltage operating level, (e.g. ±13.5 V instead of ±15 V) where $r_{DS(ON)}$ is highest.

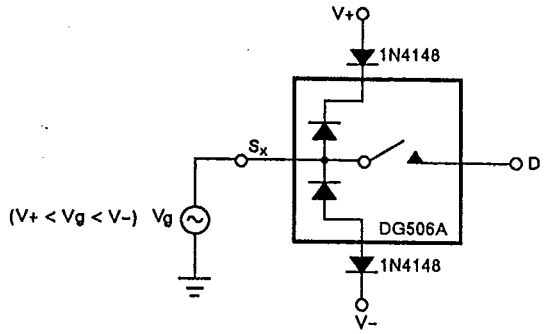
Leakage currents are specified and tested to new lower limits at both room temperature and over the full temperature range. For example, the industrial range devices' leakages have been reduced from 200 nA (over temp) on the DG508A to 50 nA (over temp) on the DGP version. Additionally, the leakages are specified at the extremes of the operating ranges (e.g. ±16.5 V instead of ±15 V), where the leakages tend to be the highest. This is essential for designs where worst-case leakage must be well known, such as precision instruments and sample-and-hold amplifiers.

The tested supply range of the DGP508A is increased beyond that of the DG508A, up to ±20 V and down to ±10.8 V. This allows the switches to have guaranteed performance limits with power supplies as low as ±12 V (±10%), ±15 V (±10%), and up to ±20 V.

APPLICATIONS

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V– value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S – (V–) doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V–, but it preserves the low channel resistance and low leakage characteristics of the device.



Overvoltage Protection Using Blocking Diodes

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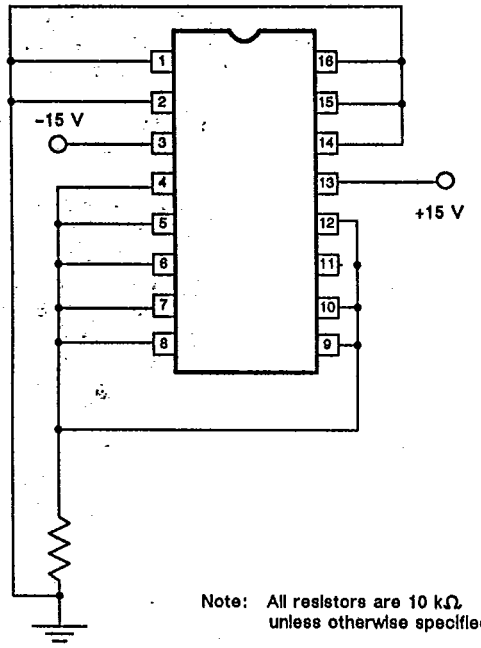
DGP508A

Siliconix incorporated

BURN-IN DIAGRAM

T-51-11



Note: All resistors are 10 kΩ unless otherwise specified