NATEL

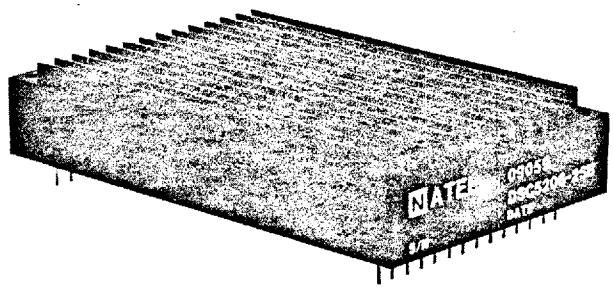
# DSC5206

# Reference Powered, 12 VA Output 16-bit, 4 Arc-minute Accuracy Digital-to-Synchro Converter

T-71-35-03

## Features

- **Fully Protected 12 VA Output**
  (current limiting)
  (short circuit proof)
  (thermal cut-off)
  (over-voltage transient protected)
- **No DC Power Supplies Needed**
  (reference powered)
- **Microprocessor Compatible**
  (8- and 16-Bit)
- **Double-Buffered Digital Inputs**
- **4 Arc-minute Accuracy**
- **Low Power Dissipation**
  (1.25 watts per VA delivered to load)
- **Built-in "KICK" Circuit**
  (prevents synchro "hang-ups")
- **Fully Isolated Operation**
  (inputs/outputs/reference)
- **BIT** (built-in test) **Output**
- **Compact PCB Mounting**
  (5.2 X 3.2 X 1.0 inches)



DSC5206

## Applications

Training Simulators
Remote Indicators
Gun Fire Control
Navy Re-transmission Systems
Test Equipment

## Description

The Model **DSC5206** is the first 4 arc-minute 12 VA synchro driver with Built-in 16-bit Digital-to-Synchro capability. The 12 VA output power is delivered efficiently through a reference-powered design that develops an internal "dynamic power supply" which reduces power dissipation by a factor of 2 over conventional designs. The **5206** has an extremely low (0.05%) scale factor variation which further helps reduce power when driving TR loads. Being reference powered, it also eliminates the need for all external DC power supplies. Packaged in a single, PCB mountable module with integral heat dissipating fins, the **5206** offers excellent thermal transfer and high reliability.

The high output drive power of 12 VA makes the **5206** the ideal choice when driving single and multiple active Torque Receiver (TR) Synchro loads, Control Differential Transmitters (CDXs) and Control Transformers (CTs). Included also is a built-in "KICK" circuit which senses when a TR load may be "hung-up" and automatically shifts the output angle by 120° to free-up the synchro. In addition, the output stage is fully protected and includes fast-acting active current limiting, thermal cutoff, and output stage transient suppression to make the **5206** virtually indestructible.

A built-in-test circuit continuously monitors the output currents in all three output drivers along with other internal test points. An open collector logic output referenced to the logic ground immediately indicates if a fault condition is present.

The logic interface is easy, having the flexibility designed in to make interfacing possible with a minimum number of components. This includes the double-buffering of all input logic data bits. All data bits (1-16) are true binary coded and are actively pulled down to ground, so if the application requires less than 16-bits any unused bits may be left unconnected. Control bits LBE, HBE, and LDC control the operation of the data input buffers. All digital inputs are TTL and 5-V CMOS compatible, using internally derived logic thresholds that guarantee 0.8-V as a logic "0" and 2.4-V as a logic "1."

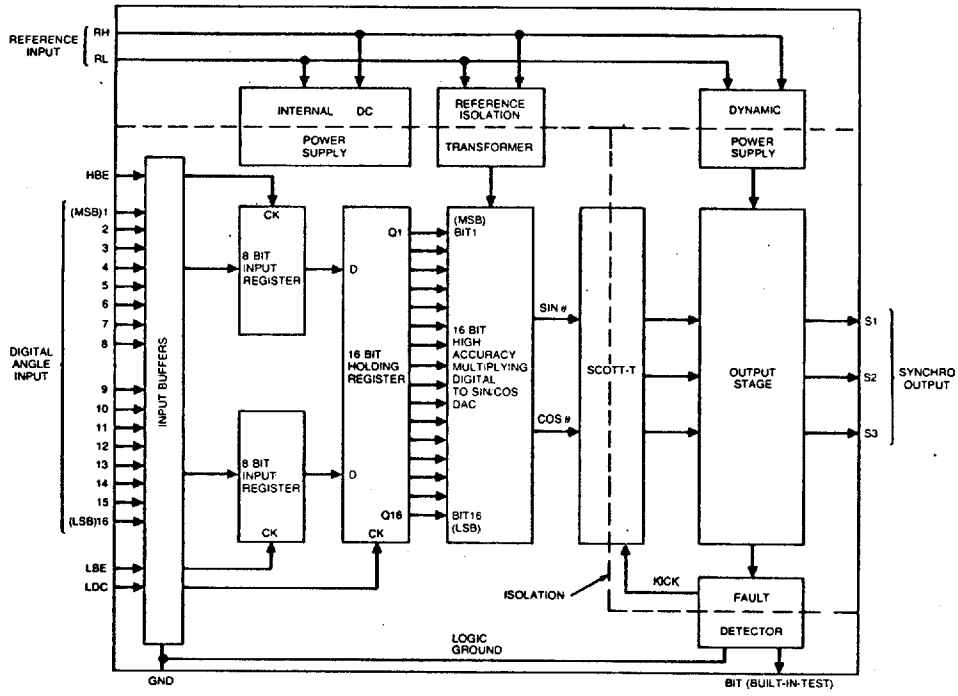



**FIGURE 1 5206 Functional Block Diagram**

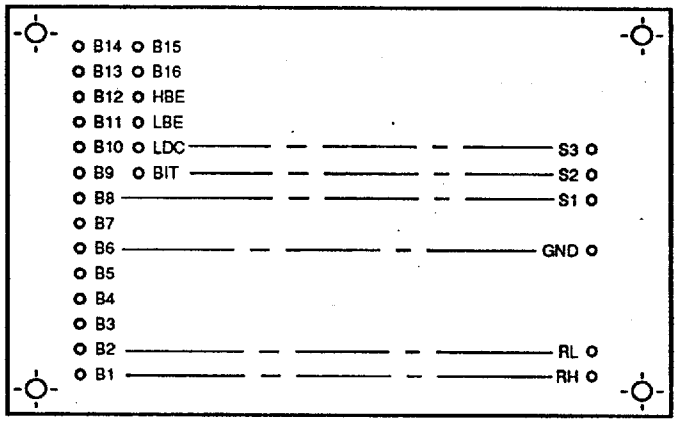
The operation of **Model 5206** is illustrated in the functional block diagram of Figure 1. The reference voltage (RH-RL) is received by both a power transformer and an isolation transformer. The power transformer has separate secondary windings. One set of windings provides bias and dynamic power supply voltages to the output stage; while another set provides power to the input circuitry, and is therefore referenced to the incoming "logic ground" line. The reference isolation transformer provides a scaled-down representation of the input reference to the Multiplying digital-to-analog sine/cosine converter (DAC).

The digital word representing the input angle is applied to the input buffer registers, which are configured as two independently enabled bytes of 8 bits each. These bytes are controlled by the HBE (high byte enable) and LBE (low byte enable) input logic controls. When interfacing the **5206** to an 8-bit microprocessor, these registers are normally addressed sequentially over common data lines. When interfacing to a 16-bit data bus, both input registers are enabled simultaneously to accept a single 16-bit word. The second 16-bit "Holding Register" allows the input registers to be presented to the Sine/Cosine DAC simultaneously as a single 16-bit word. this holding register is controlled by the LDC (load converter) input. This double-buffering is especially important in 8-bit microcomputer-based systems where false codes and servo "hunting" would otherwise occur. The presence of these two registers in series allows the systems and circuit designers maximum flexibility in controlling the updating of the converter with digital data in systems with and without microprocessors. All three registers pass data from input to output whenever their respective enable signals are at logic "1," and latch data when the enable signals are at logic "0." The output of the holding register is applied to the digital input of the Multiplying Sine/Cosine DAC. This DAC accepts the ac reference as a second input and multiplies the two together while following Sine and Cosine laws. The result are signals at the ac reference frequency and phase which precisely reflect the Sine and Cosine of the input digital angle. The operation of the Multiplying Sine/Cosine DAC is very similar to a pair of conventional four-quadrant multiplying DACs, with the exception that the transfer function is controlled by resistor ladders that follow Sine and Cosine laws instead of linear transfer functions. The format of these signals is changed from Sine/Cosine to Synchro format through an isolation scott-tee type transformer. The resultant 3 signals are then applied to the output stage.

The output stage consists of three precision power amplifiers in push-pull class AB configurations, powered from a dynamic power supply. This dynamic supply reduces the dissipation in the output section by allowing the output transistors to operate with less average voltage across them as compared to operation from a fixed DC power source. To assure stable operation over temperature and load variations, precision operational amplifiers are used as the primary amplifier gain element. In addition to providing short circuit protection, current limiting, and voltage transient protection; the power amplifiers are designed to shut down in a high impedance output state when the amplifier temperature reaches 125 degrees centigrade, thereby making them virtually indestructible.

An internal "KICK" circuit is used in the **5206** to prevent the possibility that the torque receiver may become locked at 180° from the true angle. It does this by shifting the electrical angle by 120° if the output is in current limit for more than four seconds.

The internal BIT circuit provides a fault indication if there is a loss of reference, output short circuit or overload, internal thermal shutdown, or internal circuit failure. The "open collector" logic output allows maximum flexibility in interfacing to system fault logic.




BOTTOM VIEW

**FIGURE 2 DSC5206 Pin Assignments**

GND — Digital Ground -

To be connected to the input logic ground. This is also the ground reference for the BIT output.

B1-B16* — Parallel Input Data Bits -

B1 is MSB. Bit weight = 180 degrees
B16 is LSB. Bit weight = 0.0055 degrees

RH, RL — Input Reference Voltage -

RH stands for reference high.
RL stands for reference low.

S1, S2, S3 — Analog Synchro Output Signals -

These outputs are the synchro equivalent of the digital input angle. They are isolated from both the reference input and the logic input ground.

HBE* — High Byte Enable -

Data bits 1-8 enter the input buffer register when HBE is set to a logic "1." When HBE is at logic "0," input data bits 1-8 are ignored.

LBE* — Low Byte Enable -

Data bits 9-16 enter the input buffer register when LBE is set to a logic "1." When LBE is at logic "0," the input data bits are ignored.

LDC* — Load Converter -

When LDC is set to logic "1," the converter will transfer the contents of the two input buffer registers to the input holding register. This presents data to the converter and results in a corresponding analog output. When LDC is set to logic "0," data is held in the holding register and the outputs of the two input buffer registers are ignored.

BIT — Built-in Test -

Open collector logic output signal referenced to the logic ground.
Logic "0" = no fault condition present.
Logic "1" (open circuit) = fault condition.

*Note: Unused pins may be left unconnected.

## Specifications

| PARAMETER | VALUE | REMARKS | TEST LEVEL |
|---|---|---|---|
| **Digital Angular Resolution** | | | |
| | 16-bits (0.33 arc-minutes) | | Note 2 |
| **Accuracy** | | | |
| | ± 4.0 arc-minutes (option S)<br>± 8.0 arc-minutes (option P) | Accuracy applies over the full operating temperature, frequency, power supply, and load ranges | Note 1 |
| **Reference/Power Input** | | | |
| Voltage | 115 V-rms, ±10% | For 90 V-rms nominal output | Note 2 |
| Frequency | 360 to 440 Hz | | Note 3 |
| Input Current | 35 mA-rms maximum<br>230 mA-rms maximum | Vref = 115 V-rms, No Load<br>Vref = 115 V-rms, 12.5 VA Load | Note 1 |
| Breakdown Voltage | 500 V-dc minimum | To logic ground or any output | Note 3 |
| Harmonic Distortion | Up to 10 percent | Without degradation in accuracy | Note 3 |
| **Digital Inputs** | | Transient-protected CMOS | |
| Logic "0" level<br>Logic "1" level | – 0.3 to 0.8 V-dc<br>2.4 to 5.5 V-dc | | Note 2<br>Note 2 |
| Input Current<br>Data bits 1-16<br>Input Current<br>HBE, LBE, LDC | 15 µA typical (30 µA max.), active pull down to ground<br>– 15 µA typical (–30 µA max.), active pull up to internal 5 V-dc | Unused pins may be left unconnected<br>Unused pins may be left unconnected | Note 3<br>Note 3 |
| Data Bit Coding | Positive logic, natural binary angle | B1 is MSB, B16 is LSB | Note 3 |
| **Register Controls** | | Active-high transparent latches | |
| HBE | Logic "1"<br>Logic "0" | Data bits 1-8 enter high-byte input register<br>High-byte input register holds data | Note 1 |
| LBE | Logic "1"<br>Logic "0" | Data bits 9-16 enter low-byte input register<br>Low-byte input register holds data | Note 1 |
| LDC | Logic "1"<br>Logic "0" | Data from input register enters holding register<br>Holding register holds data | Note 1 |
| Pulse Width<br>HBE, LBE, and LDC | 600 ns minimum | For guaranteed data transfer | Note 3 |
| Data Set-up Time | 200 ns minimum | Data stable before HBE or LBE low-to-high transition | Note 3 |
| Data Hold Time | 200 ns minimum | Data stable after HBE or LBE high-to-low transition | Note 3 |
| **BIT Output** | | Referenced to Digital Ground | |
| Output Current<br>Sink<br>Source (Leakage) | 1 mA minimum @ 0.8 V-dc<br>10 nA typ. @ 25°C, (20 V-dc)<br>100 µA max. over temp. (20 V-dc) | Open collector output | Note 1 |
| Logic "0"<br>Logic "1" | – 0.3 to 0.8 V-dc @ 1 mA load<br>Open collector, V max = 20 V-dc | For no Fault Detected<br>Fault Detected | Note 1<br>Note 1 |

| PARAMETER | VALUE | REMARKS | TEST LEVEL |
|---|---|---|---|
| **Synchro Analog Outputs** | | | |
| Voltages (Line-to-Line) | 90 V-rms nominal | For nominal reference voltages. The outputs vary in direct proportion to the reference amplitude | |
| Gain | 0.783 ±1% | 115 V-rms reference input / 90 V-rms output | Note 1 |
| Radius Accuracy | 0.05% maximum | Scale factor variation with angle | Note 2 |
| Drive Capability | 12.5 VA minimum | | Note 1 |
| Output Current Drive | 225 mA peak minimum | Between S1, S2, and S3 outputs | Note 3 |
| Output Impedance (dc to 440 Hz) | less than 2.5 ohms | | Note 3 |
| Load Regulation | 0.25% maximum | From no load to full load | Note 2 |
| Synchro Load Impedance | $\|Z_{so}\| > 486\ \Omega$ | 12.5 VA limit | Note 1 |
| Output Setting Time | 250 µs maximum | To specified converter accuracy (179° step) | Note 2 |
| Phase Shift | less than 2 degrees | Reference to output | Note 3 |
| Quadrature Output | 0.25% maximum | | Note 2 |
| Output dc Offset (Line-to-Line) | ± 10 mV typical, ±50 mV maximum | | Note 2 |
| Thermal Cut-off | 85°C top-plate temperature min. | | Note 2 |
| Output Short Circuit Duration | Indefinite | All outputs together simultaneously | Note 3 |
| **Power Dissipation** | | Internal | |
| No Load<br>12.5 VA Load | 4.0 watts maximum<br>15.0 watts maximum | For Resistive loads. Does not include power dissipated in the load | Note 3 |
| **Thermal Resistance** | | Based on internal module dissipation | |
| Case (Top Plate) to Ambient | 3 degrees C per watt typical | Actual value depends upon cooling configuration | Note 3 |
| Junction to Case Top | 3 degrees C per watt maximum | For the worst case device junction vs. output load | Note 3 |
| **Physical Characteristics** | | | |
| Size | 5.20 X 3.17 X 1.04 inches (132 X 81 X 26 mm) | | Note 3 |
| Weight | 17 oz. (482g) typical<br>24 oz. (680g) maximum | | Note 3 |

NOTE 1. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

## Absolute Maximum Ratings

Reference Input ..... 138 V-rms
Digital Inputs ..... – 0.3 V-dc to +6.5 V-dc
Storage Temperature ..... – 65°C to +135°C

Although the digital inputs have integral transient protection, this protection is not a substitute for proper electrostatic handling procedures. This part is ELECTROSTATIC SENSITIVE and must be treated as such.

## Output Protection

The **Model 5206** incorporates several protection methods that together make the **5206** virtually indestructible. These methods are:

1. Active current limiting
2. Thermal cut-off
3. Overvoltage transient protection

The active current limiting circuitry in the **5206** continuously monitors the instantaneous current in each of the three output drivers. When an overcurrent or output short circuit condition exists, the peak current that can be supplied to the load is instantly limited to a value that is safe for the components used within the **5206**.

The thermal cut-off circuit of the **5206** uses a solid-state temperature-sensing element attached to the top plate. The voltage from this temperature sensor provides an indication when the power amplifiers temperature reaches 125°C. If this occurs, a disable signal is applied to each of the output power amplifiers, which removes all output current drive capability. The result is that the outputs go into a high-impedance state and are no longer capable of driving load current. When the internal temperature drops to a safe level, the output stages are automatically restored to their normal state.

The **5206** incorporates overvoltage transient protection on both the reference input and the synchro outputs. These transient protection networks utilize rugged transient suppression diodes that automatically conduct to suppress transient energy whenever the applied voltages reach dangerous levels. The reference-protection diode is connected internally across RH-RL and may begin to conduct if the reference input (RH-RL) reaches 190 volts peak. The output-protection diodes are connected in a "delta" configuration, with one diode between each of the S1-S2, S2-S3, and S1-S3 output pairs. Transient protection is necessary at the output of the **5206** due to the fact that synchros are, by nature, inductive loads and can produce voltage transients many times their nominal voltage due to inductive "kick."

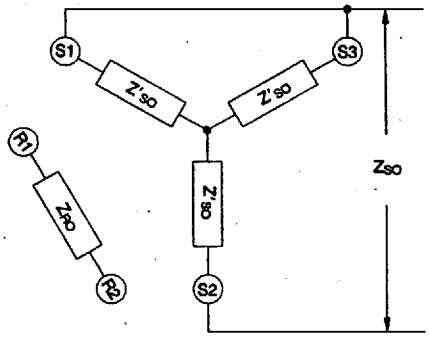



**FIGURE 3 Synchro Load Schematic**

## Synchro Loads

There are several types of synchro loads, including Control Transformers (CTs), Torque Receivers (TRs), and Control Differential Transmitters (CDXs). The 12.5 VA output drive of the **5206** makes it possible to drive all but the heaviest TR loads easily. In many cases, the **5206** can drive multiple loads. The two most common loads driven by the **5206** are CTs and TRs.

CTs are electromechanical synchro devices which provide a null voltage output from the rotor winding whenever the actual shaft angle of the CT matches the angle sent to the CT from the S1, S2, and S3 outputs of the **5206**. The actual transfer function of a CT is as follows:

$$V_{rotor}\ (rms) = K \times V_{L\text{-}L} \times \sin(\theta - \phi)$$

where:

| | | |
|---|---|---|
| K | = | gain of the CT |
| $V_{L\text{-}L}$ | = | line-to-line voltage from **5206** |
| $\theta$ | = | the angle represented by the **5206** output |
| $\phi$ | = | the CT shaft angle |

In systems that use CTs, they are utilized as position sensing elements rather than as torque or motor elements. The force that is used to position the shaft generally is provided by a motor coupled to the common shaft. CT impedances, therefore are relatively high.

A schematic diagram of a typical synchro load is shown in Figure 3. $Z_{so}$ is the impedance measured between one leg (S2, for example) and the other two legs (S1, S3) shorted together, with the rotor open circuit. The relationship between $Z_{so}$ and the individual winding impedances ($Z'_{so}$) is given by:

$$Z_{so} = (3/2) \times Z'_{so}$$

The relationship between the synchro output voltages, output VA, and $Z_{so}$ is as follows:

$$VA = 3/4 \times V^2 / Z_{so}$$

where:

VA is the VA required from the **5206** to drive the load and V is the rms value of the maximum line-to-line **5206** output voltage*.

*The maximum value of an rms voltage refers to the rms voltage level when the voltage is at its maximum value, since the line-to-line output voltages vary with input digital angle. For example, the rms voltage between S3 and S1 is maximum when the input angle is 90°.

**Example:**

From **5206** Data Sheet, page 4, 90 V-rms output can drive $|Z_{so}| = 486$ ohms. To calculate the VA drive:

$$VA = 3/4 \times V^2 / Z_{so} = 3/4 \times (90)^2 / 486$$

$$VA = 12.5$$

**TABLE 1. Typical Control Transformer Parameters**

| CT Type | Frequency | Voltage | $Z_{so}$ | $\lvert Z_{so} \rvert$ | Required VA |
|---|---|---|---|---|---|
| 11 CT4e | 400 | 90 V-rms | 700 + j4900 | 4950 | 1.23 |
| 15 CT4c | 400 | 90 V-rms | 1020 + j8330 | 8392 | 0.72 |
| 18 CT4c | 400 | 90 V-rms | 1360 + j12600 | 12700 | 0.48 |
| 23 CT4c | 400 | 90 V-rms | 1230 + j14300 | 14353 | 0.42 |

The **Model 5206** can be used to drive single or multiple Torque Receiver (TR) loads. TRs are constructed in the same manner as CTs, except that they generally have much lower impedances than CTs and are meant to provide torque to the rotating shaft.

TRs provide torque as a result of the interaction of two magnetic fields within the TR; one field produced by the S1, S2, and S3 stator windings, and one field from a reference source applied to the rotor windings. The TR can be considered an "active" load in that it "acts" against the opposing **5206** output, depending upon shaft angle, to produce a torque at the TR shaft. Torque is produced whenever the TR shaft angle and the **5206** input angle are different, thereby producing a voltage gradient between the **5206** output and the TR stator output. Circulating currents are developed as a result of this voltage gradient to provide the "magnetomotive force" that produces the "opposing" magnetic field against the rotor field. The opposing magnetic fields within the TR apply a torque gradient in attempting to rotate the TR shaft until the shaft angle is equal to the **5206** input angle. When the two angles are equal, the result is a "null" condition where the torque gradient is zero.

Theoretically, the TR represents an infinite load impedance to the **5206** output when the TR shaft angle is exactly equal to the **5206** input angle. In actual practice, however, the effective load impedance at "null" (shaft angle = **5206** input angle) will be reduced by the effects of two variables:

1. Line-to-line voltage differential between the TR stator and **5206** output.
2. Line-to-line phase-shift differential between the TR stator and **5206** output.

Any such line-to-line voltage and/or phase-shift differentials will give rise to an additional VA (voltage-ampere) requirement from the **5206**, resulting in a loss of available VA for producing torque. This additional VA requirement is as follows:

$$VA_{D/S} = [3(V_{L\text{-}L})^2/2Z_{SS}] \times \sqrt{(\Delta E/2V_{L\text{-}L})^2 + [\text{Sin}\ (\Delta\sigma/2)]^2}$$

where:

$V_{L\text{-}L}$ = **5206** maximum L-L voltage (90 V-rms)
$\Delta E$ = (**5206** – TR) L-L voltage differential
$Z_{SS}$ = Stator impedance with rotor shorted
$\Delta\sigma$ = (**5206** – TR) phase shift differential (°)

For example, to find the additional VA required by the 5206 (excluding the VA required to produce torque), consider the following example of driving a type 15TRX4a torque receiver:

$V_{L\text{-}L}$ = 90 V-rms
$\Delta E$ = 2.7 V-rms (3% of 90 V-rms)
$|Z_{SS}|$ = 66 ohms
$\Delta\sigma$ = 5
$VA_{5206}$ = 8.5

As this example demonstrates, VA is easily "stolen" from the **5206** due to line-voltage and phase-shift differentials. This is an important point to consider when designing TR systems.

The torque gradient required from the TR shaft will depend upon the particular application. Some applications, such as driving indicators or other visual readouts will not require much torque. Other applications, where the TR may be driving heavier loads, will require more VA. The torque that can be provided to the shaft will depend upon the type of TR; the "available" VA after the effects outlined above are accounted for and the difference between the shaft angle and the input angle to the **5206**. The VA required by the TR to produce a torque gradient is described by the following equation:

$$VA_{5206} = [3(V_{L\text{-}L})^2/2Z_{SS}] \times \text{Sin}\ [(\theta - \phi)/2]$$

where:

$V_{L\text{-}L}$ = **5206** maximum L-L voltage (90 V-rms)
$Z_{SS}$ = TR stator impedance with rotor shorted
$\theta$ = **5206** input angle
$\phi$ = TR shaft angle
$VA_{5206}$ = Volt-amperes needed from **5206**

Consider an example where a type 15TRX4a torque receiver is required to produce a torque gradient of 4 g-cms at a differential angle ($\theta - \phi$) of 2°. The operating parameters are the same as the previous example. The required VA from the **5206** can be calculated as follows:

$VA = [3 \times (90)^2/(2 \times 66)] \times \text{Sin}\ (2/2)$
$= 3.2$ VA

This calculation should be combined with the previous calculation for the "additional" VA in order to predict the total VA required from **5206**. In order to combine the calculations, the equation below should be used in order to take into account the phase relationship between the various current components supplied by the **5206**.

$$VA_{5206} =$$

$$[3(V_{L\text{-}L})^2/2Z_{SS}] \times \sqrt{[(\Delta E/2V_{L\text{-}L}) + \text{Sin}\{(\theta - \phi)/2\}]^2 + [\text{Sin}\ (\Delta\sigma/2)]^2}$$

The terms for this equation are defined in the previous examples.

*Note: To reduce the VA requirement, stator resistors (in series with S1, S2, S3) can be added to increase the total "$Z_{SS}$" impedance.

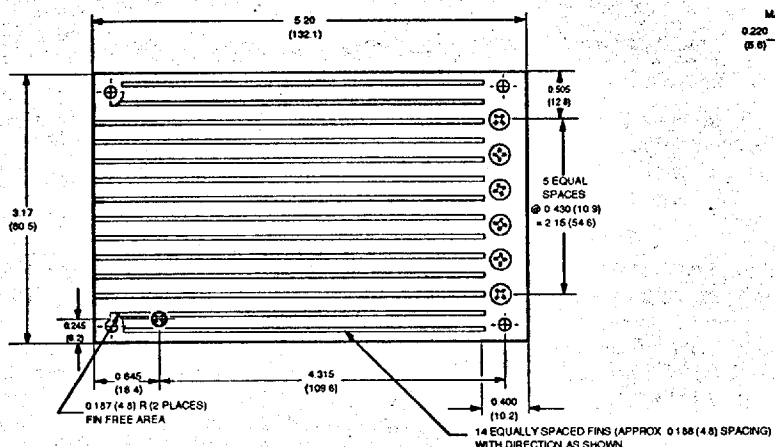
Voltage imbalance ($\Delta E/V_{L\text{-}L}$) used in calculations for Table 2 is ±3%

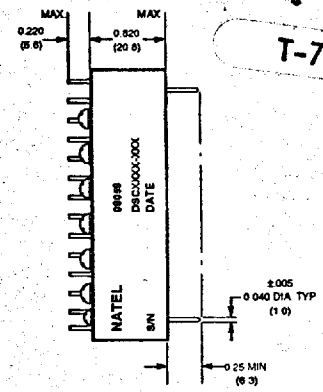
**TABLE 2. VA Load on 5206 with TR at "Null"**

| TR Type | Frequency | Voltage ($V_{L\text{-}L}$) | $\lvert Z_{SS} \rvert$ (Nom) | Phase Shift (Maximum) | *VA "Null" |
|---|---|---|---|---|---|
| 11 TR4c | 400 | 90.0 | 215.0 | 6.0° | 3.1 |
| 15 TRX4a | 400 | 90.0 | 66.0 | 5.0° | 8.5 |
| 18 TRX4a | 400 | 90.0 | 19.0 | 4.0° | *24.3 |
| 23 TRX4a | 400 | 90.0 | 7.3 | 2.0° | *38.3 |

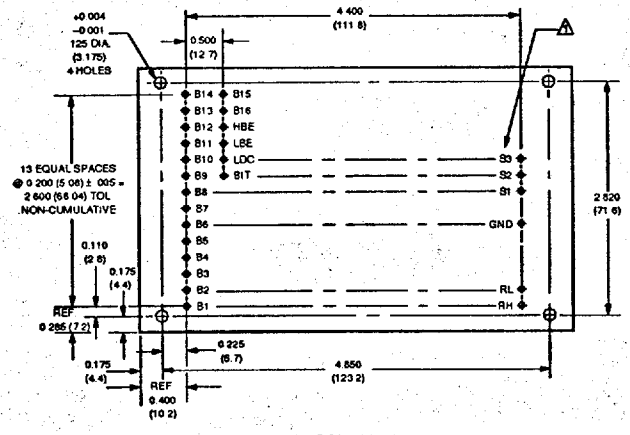
Voltage imbalance ($\Delta E/V_{L\text{-}L}$) used in calculations: ±3%.

TOP VIEW




BOTTOM VIEW




**TOLERANCES:**
.XX = ±.020 (±.51)
.XXX = ±.010 (±.25)

NOTES:
Dimensions shown in inches and (mm).
⚠ Designations are for reference only and do not appear on part as shown.

**MECHANICAL OUTLINE**

## Ordering Information

**DSC5206 - T A M**

**Temperature Range**

1 = 0° C to +70° C
2 = −40° C to +85° C

**Accuracy**

P = ±8.0 arc-minutes
S = ±4.0 arc-minutes

**Mil Specification**

B = MIL-STD-883B
S = Standard

A wide range of applications assistance is available from Natel. Application notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

## Other products available from NATEL

- **3 arc-second accurate,** Programmable Dynamic Angle Simulator that includes 4 Related Instruments and is totally A.T.E. Programmable (L200).
- Hybrid (36-pin DDIP size) Synchro(Resolver)-to-Digital converters that operate from a **single +5V power supply** and offer excellent features such as BIT, AGC, low power dissipation and more (Models 1006, 1056, 1046 and 1044).
- 1.3 arc-minute accuracy, high power, Digital-to-Synchro converters that **do not require any DC power supplies** (Models 5031 and 5131).
- 1-inch square, single +5V powered, 16-bit R/D converter with built-in **Reference Oscillator.**
- **2-channel** Digital-to-Sin/Cos Converter in a single 36-pin hybrid (HDSC2036).
- **2-speed,** 22-Bit Synchro(Resolver)-to-Digital Converter, 0.0004° accuracy in a single 40-pin TDIP (HRD/HSD1626).
- **3-channel** Resolver-to-Digital Converter in a single 40-pin TDIP (HRD1346).
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106).

TEL: (805) 581-3950

NATEL ENGINEERING CO., INC.

4550 RUNWAY STREET • SIMI VALLEY, CA 93063-3493
TWX: (910) 494-1959 FAX: (805) 584-4357