H7211
Four Digit LCD Decoder / Drivers

HUGHES AIRCRAFT COMPANY
MICROELECTRONICS CENTER

T-52-13-07

DESCRIPTION

Hughes 7211 devices are configured to drive conventional 4 digit, 7 segment LCD displays. They feature on-chip oscillator, divider chain, backplane driver, and 28 segment drivers. These devices simplify the task of implementing a cost effective alphanumeric 7 segment display for microprocessor systems since they latch data and perform character encoding.

Two input configurations are available. One provides four data bit inputs and four digit select inputs. This configuration (7211-1, 7211-2) is suitable for interfacing with multiplexed BCD or binary output devices such as counters. The microprocessor oriented interface (7211-3, 7211-4) devices provide data input latches and digit select code latches under control of chip select inputs.

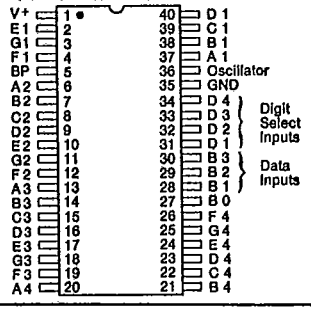
Two different decoder configurations are available. One configuration (7211-1, 7211-3) will decode four bit binary input into a seven segment alphanumeric hexadecimal output. The other (7211-2, 7211-4) versions will provide the output code 0-9, dash, E, H, L, P, blank. Either device will correctly decode BCD to seven segment decimal outputs.

The 7211-1/7211-2/7211-3/7211-4 are available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

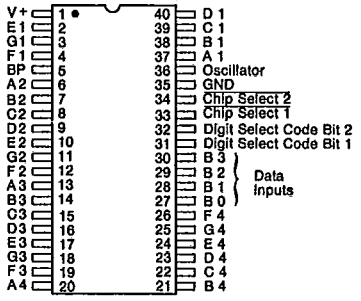
FEATURES

- CMOS Circuitry
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- Four digit non-multiplexed 7 segment LCD display outputs with backplane driver
- Complete onboard RC oscillator to generate backplane frequency
- Backplane input/output allows simple synchronization of slave-device segment outputs to a master backplane signal
- Cascadable
- 7211-1, 7211-2 provide separate digit select inputs to accept multiplexed BCD input
- 7211-3, 7211-4 provide data and digit select code input latches controlled by chip select inputs to provide direct microprocessor interface.
- 7211-1, 7211-3: decode binary to hexadecimal
- 7211-2, 7211-4: decode binary to code B (0-9, dash, E, H, L, P, blank)

7211-1, 7211-2
PIN CONFIGURATION



7211-3, 7211-4
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

V_{DD} ..... −.3 to + 6.5V
Power Dissipation 250mW
Operating Temperature
Plastic Package ..... −40 to +85°C
Ceramic Package ..... −55 to +125°C
Storage Temperature ..... −65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

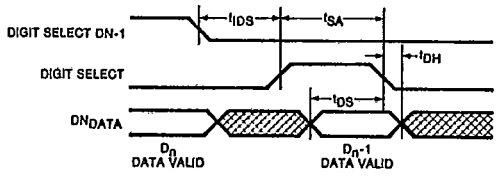
ELECTRICAL CHARACTERISTICS at T_A = −55 to 125°C, V_{DD} nominal, C_L = 50pF

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current [2]	I_{OP}	Test circuit, Display blank		10	50	µA
Oscillator Input Current [2]	I_{OSCI}	Pin 36		± 2	± 10	
Segment Rise/Fall Time	t_{RFS}	C_L = 200 pF		0.5		us
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000 pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		16		KHz
Backplane Frequency	f_{BP}	Pin 36 Floating		125		Hz
Logical "1" Input Voltage	V_{IH}		3			V
Logical "0" Input Voltage	V_{IL}				1	
Input Leakage Current [2]	I_{ILK}	Pins 27-34		± .01	± 1	µA
Input Capacitance [1]	C_{IN}	Pins 27-34		5		pF
BP/Brightness Input Leakage [2]	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		± .01	±5	µA
BP/Brightness Input Capacitance [1]	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{DS}		500			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	Other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			µs

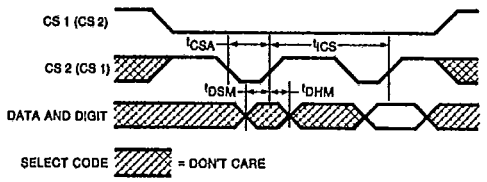
NOTE 1: Design assured but not tested.
NOTE 2: Parameters guaranteed by other tests at −55°C.

TIMING DIAGRAMS

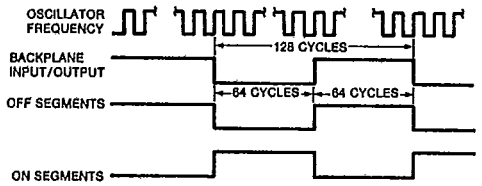
(a) Multiplexed Input Timing



(b) Microprocessor Interface Input Timing



DIGITAL WAVEFORMS



FUNCTIONAL DESCRIPTION

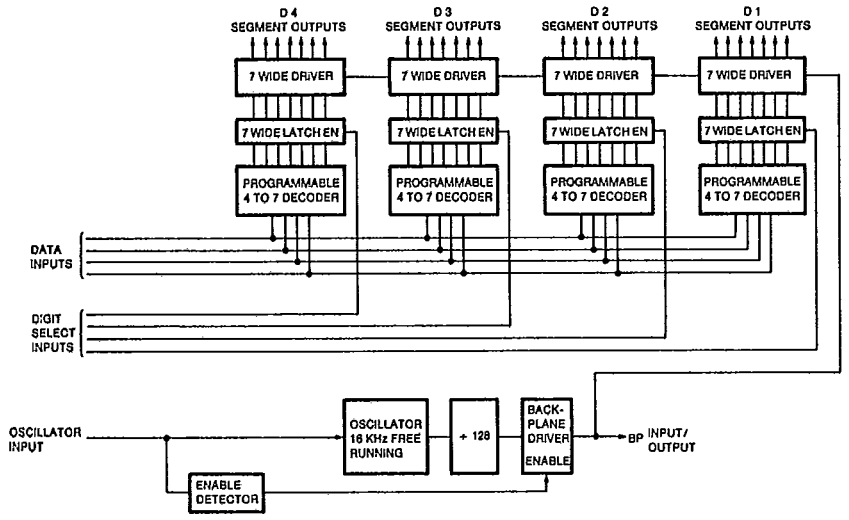
The LCD devices in the 7211-1, 7211-2, 7211-3, 7211-4 family provide outputs suitable for driving conventional four digit by seven segment LCD displays. They include 28 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate backplane frequency.

The segment and backplane drivers consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from different rise and fall times, and ensures maximum display life.

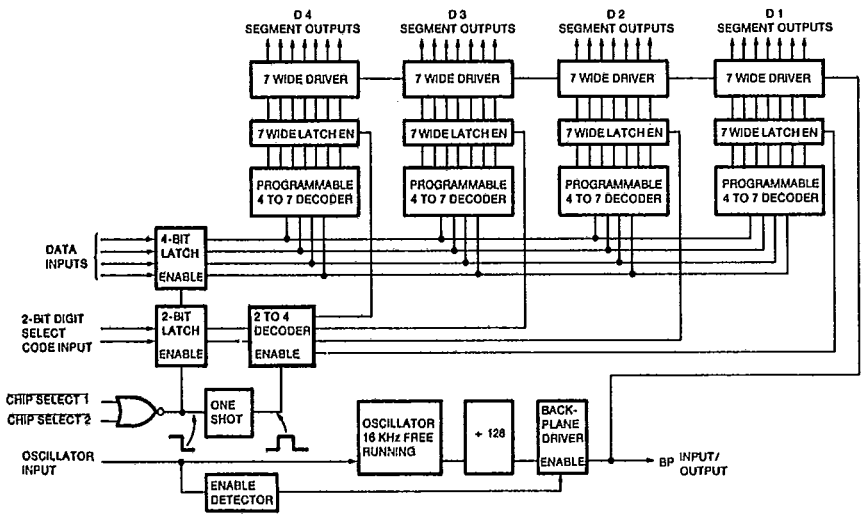
The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the negative supply. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with more than 4 digits and a single backplane. The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5 µs. (i.e. 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the 7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2 µs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

FUNCTIONAL DIAGRAMS

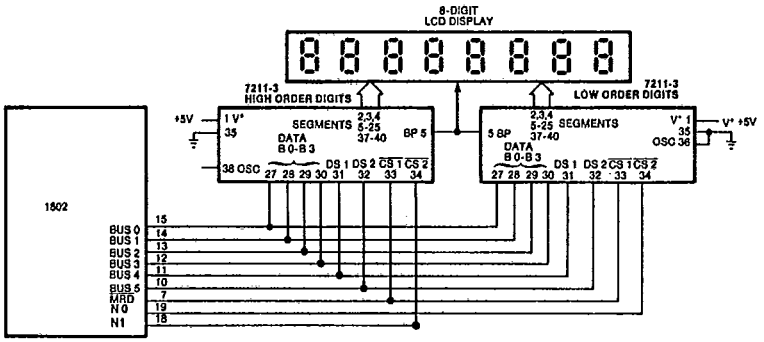
7211-1, 7211-2



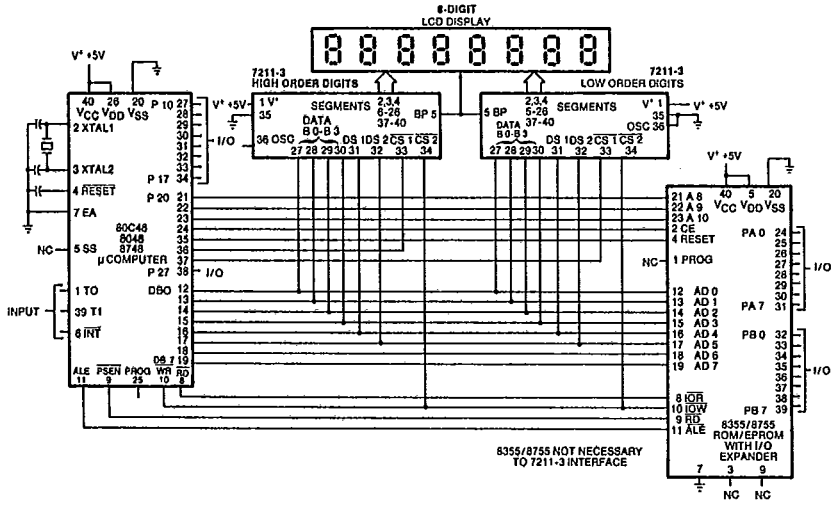
7211-3, 7211-4



(c) 1802 Microprocessor Interface via I/O Instruction Control **H7211**



(d) 80C48/8048/8748 Microcomputer Interface



The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36). The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about 1 microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

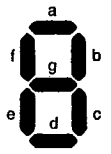
INPUT CONFIGURATION AND OUTPUT CODES

Part Number	Input Configuration	Output Code
7211-1P	Multiplexed 4-bit	Hexadecimal
7211-2P	Multiplexed 4-bit	Code B
7211-3P	Microprocessor Interface	Hexadecimal
7211-4P	Microprocessor Interface	Code B

OUTPUT CODES

BINARY					
B3	B2	B1	B0	HEXADECIMAL	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT



SIGNAL DESCRIPTION: **H7211**

A1, A2, A3, A4 — Outputs directly connected to the "a" segments of LCD
B1, B2, B3, B4 — Outputs directly connected to the "b" segments of LCD
C1, C2, C3, C4 — Outputs directly connected to the "c" segments of LCD
D1, D2, D3, D4 — Outputs directly connected to the "d" segments of LCD
E1, E2, E3, E4 — Outputs directly connected to the "e" segments of LCD
F1, F2, F3, F4 — Outputs directly connected to the "f" segments of LCD
G1, G2, G3, G4 — Outputs directly connected to the "g" segments of LCD

B0, B1, B2, B3 — Data input bits select appropriate output code B0 is the least significant bit
D1, D2, D3, D4 — Digit selects bits (7211-1, 7211-2) D1 is the least significant bit
DS1, DS2 — Two bit digit select code (7211-3, 7211-4) DS 1 is the least significant bit

DS 2	DS 1	
0	0	selects D 4
0	1	selects D 3
1	0	selects D 2
1	1	selects D 1

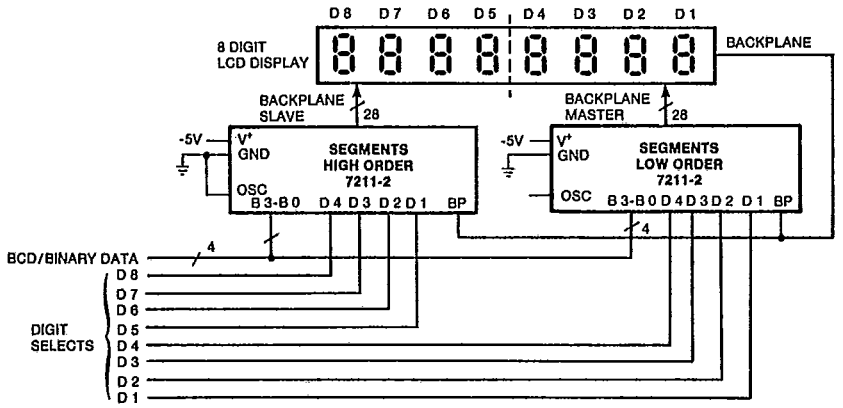
$\overline{CS\,1}$, $\overline{CS\,2}$ — Chip select signals (7211-3, 7211-4): when both $\overline{CS\,1}$, $\overline{CS\,2}$ are low, the data at the Data Inputs (B 0-B 3) and Digit Select Inputs (D 1-D 4) are written into the input latches. On the rising edge of either chip select, the data is decoded and written into the output latches.

OSC — Oscillator input can be floating or tied to external capacitor. When grounded, disables BP output devices, allowing segments to be synched to an external signal input at the BP terminal.

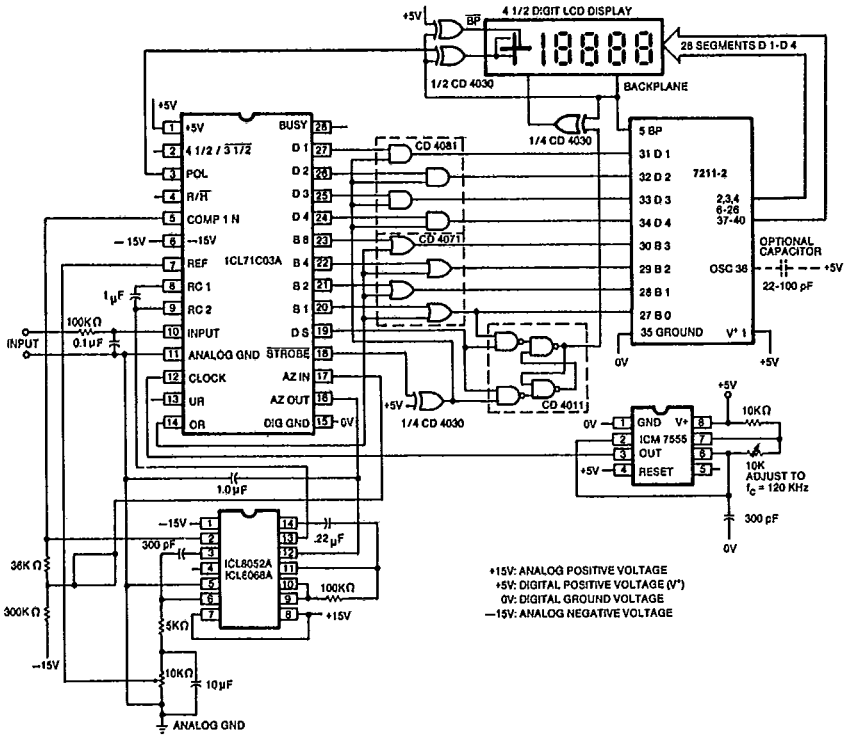
BP — See OSC pin above.

APPLICATIONS:

(a) Cascading and Synchronization:



(b) 4 1/2 Digit LCD DPM With Digit Blanking on Overrange



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