Integrated Device Technology, Inc.

2M x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4059

FEATURES:

- High-density 16 megabit CMOS static RAM module
- Pin-compatible upgrade from IDT7MP4058 (512K x 8) SRAM module
- Fast access time: 55ns (max.)
- Low power consumption
  - — Active: 110mA (max.)
  - — CMOS Standby: 450µA (max.)
  - — Data Retention: 250µA (max.)V_{CC} = 2V
- Surface-mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in a 36-pin SIP (Single In-line Package) for maximum space-saving
- Single 5V (±10%) power supply
- Inputs and outputs TTL-compatible

DESCRIPTION:

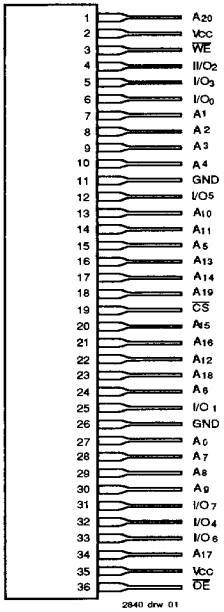
The IDT7MP4059 is a 2M x 8 high-speed CMOS static RAM module constructed on an epoxy laminate substrate (FR-4) using four 512K x 8 static RAMs and a one-of-four decoder in plastic surface mount packages.

The IDT7MP4059 is available with maximum access times as fast as 55ns, with maximum operating power consumption of 605mW.

The IDT7MP4059 is offered in a 36-pin SIP (Single In-line Package). This vertically mounted SIP module is a cost-effective solution allowing for very high packing density.

All inputs and outputs of the IDT7MP4059 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

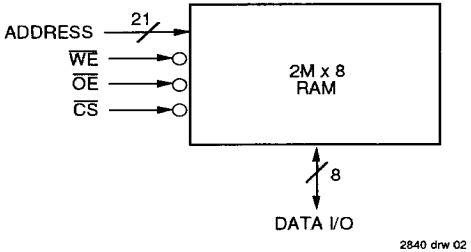
PIN CONFIGURATION



2840 drw 01

SIP
BACK VIEW

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

A_{0-20}	Address Inputs
I/O_{0-7}	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Power
GND	Ground

2840 tbl 01

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

2840 tbl 04

NOTE:
1. V_{IL} = –3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN\ (C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

2840 tbl 03

NOTE:
1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

2840 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
I_{LO}	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ 0.2V, $V_{IN} \geq V_{CC}$ –0.2V or ≤ 0.2V	—	450	µA

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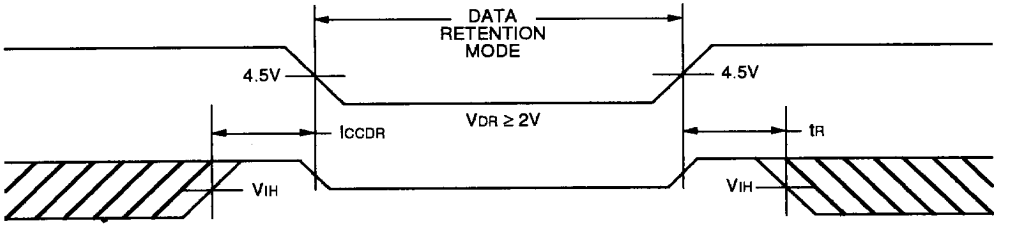
DATA RETENTION CHARACTERISTICS (T_A = 0°C TO +70°C)

Symbol	Parameter	Test Condition	Min.	Vcc @ 2.0V Max.	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}(1)	—	ns

2840 tbl 08

NOTES:
1. t_{RC} = Read Cycle Time
2. This parameter is guaranteed by design, but not tested.

DATA RETENTION WAVEFORM

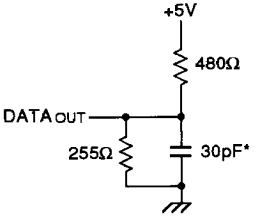


2840 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2840 tbl 09



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*Including scope and jig.

Figure 1. Output Load

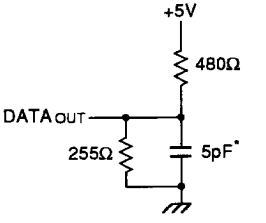

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Figure 2. Output Load
(For t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4059LxxS								Unit
		-55		-70		-85		-100		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OE}	Output Enable to Output Valid	—	30	—	45	—	48	—	50	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	20	—	30	—	33	—	35	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	20	—	40	—	43	—	45	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	55	—	70	—	85	—	100	ns
Write Cycle										
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{WP}	Write Pulse Width	40	—	55	—	65	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	2	—	5	—	ns
t_{AW}	Address Valid to End of Write	45	—	65	—	82	—	90	—	ns
t_{CW}	Chip Seleet to End of Write	45	—	65	—	80	—	85	—	ns
t_{DW}	Data to Write Time Overlap	30	—	35	—	38	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	20	—	—	30	—	33	—	35	ns
t_{OW}(1)	Output Active from End of Write	5	—	0	—	0	—	0	—	ns

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NOTE:
1. This parameter is guaranteed by design, but not tested.

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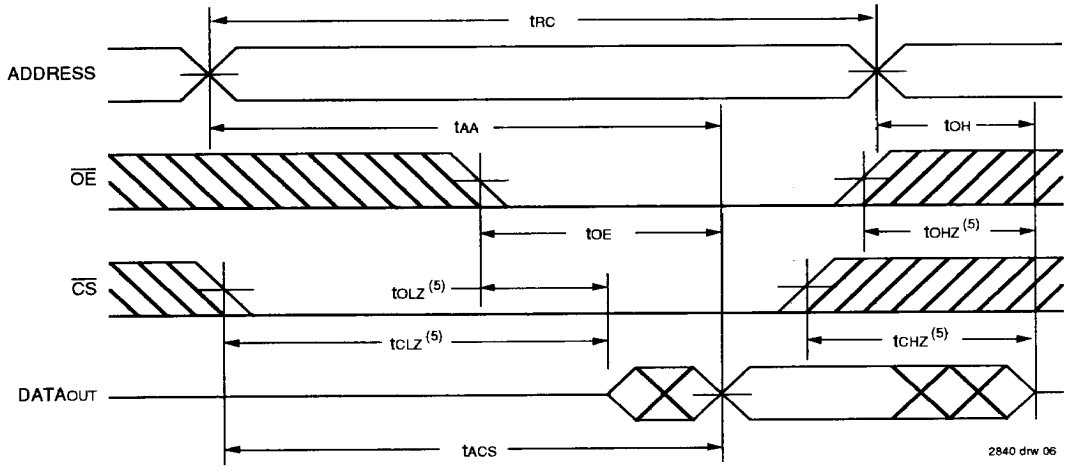
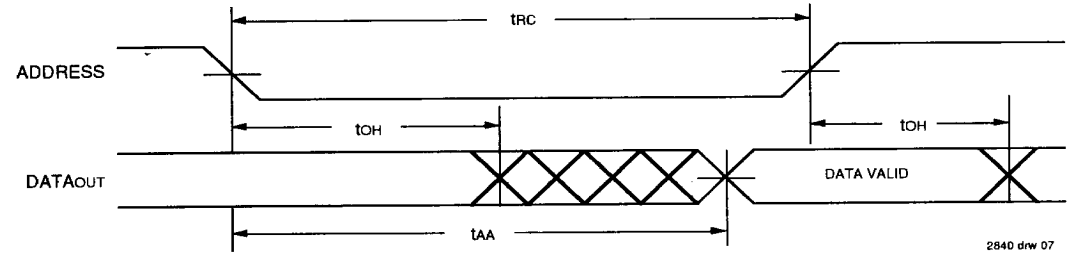
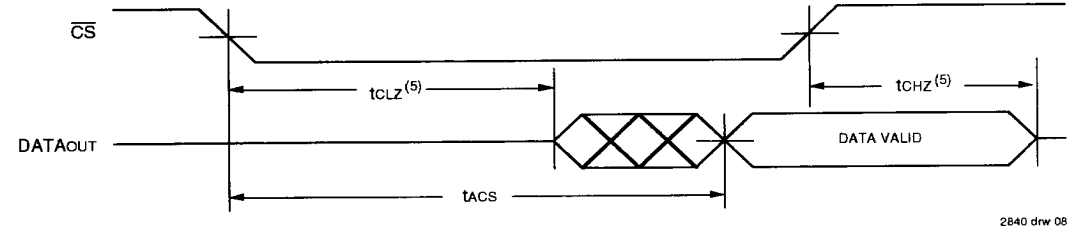
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected $\overline{CS}$ = V_{IL}
3. Address valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = V_{IL}
5. Transition is measured = 200mV from steady state. This parameter is guaranateed by design but not tested.

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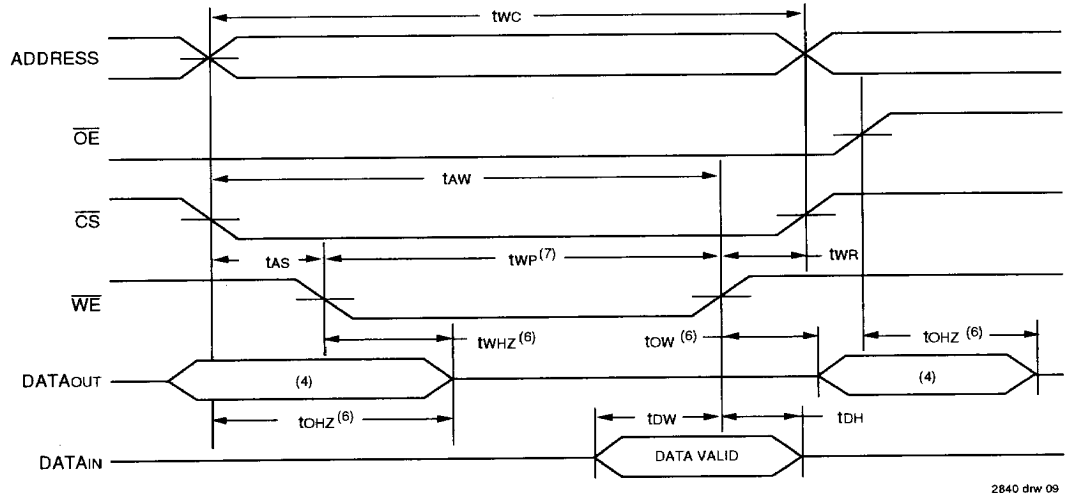
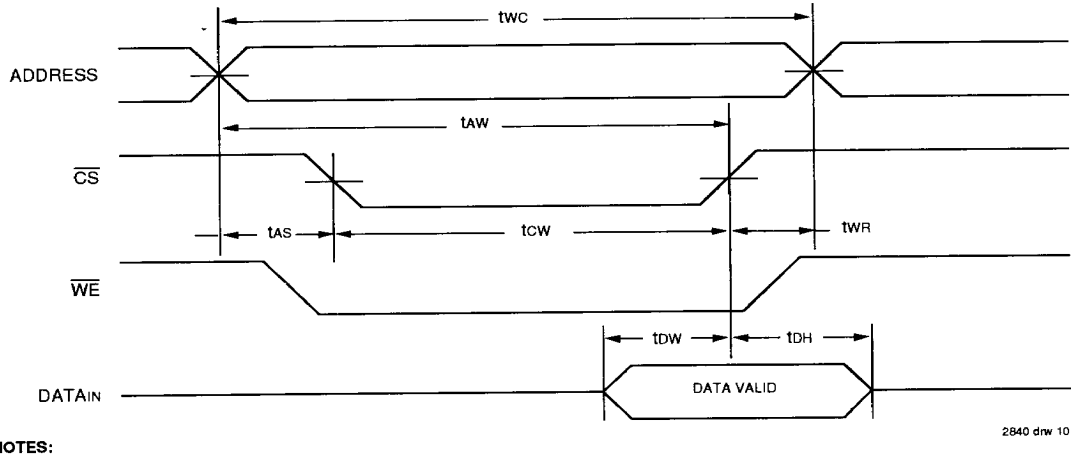
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlay (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS — PLEASE CONSULT FACTORY

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