DATA SHEET

SAB9081
Multistandard Picture-In-Picture (PIP) controller

Preliminary specification
Supersedes data of 1999 Jan 05
File under Integrated Circuits, IC02

1999 Nov 12

Philips
Semiconductors

PHILIPS

Multistandard Picture-In-Picture (PIP) controller

SAB9081

FEATURES

- Double window Picture-in-Picture (PIP) in interlaced or non-interlaced mode at 8-bit resolution
- Internal 1-Mbit DRAM
- Three 8-bit Analog-to-Digital Converters (ADCs) (7-bit performance) with clamp circuit for each acquisition channel
- One PLL which generates the line-locked clocks for the subchannel
- One PLL which generates the line-locked clocks for the main and display channels
- Three 8-bit Digital-to-Analog Converters (DACs)
- Linear zoom in both horizontal and vertical directions for the subchannel
- Linear zoom in horizontal direction for the main channel.

GENERAL DESCRIPTION

The SAB9081 is a multistandard PIP controller which can be used in double window applications. The SAB9081 inserts one or two live video signals with reduced size into another live video signal. The incoming video signals are expected to be analog baseband signals.

The conversion to the digital environment is done on chip with ADCs. Processing and storage of the video data is done entirely in the digital domain. The conversion back to the analog domain is done by DACs.

Internal clocks are generated by PLLs which lock on to the applied horizontal and vertical syncs.

The main input channel is compressed horizontally by a factor of two and directly fed to the output. After compression, a horizontal expansion of two is possible for the main channel.

The subchannel is also compressed horizontally by a factor of two but stored in memory before it is fed to the outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		–	50	–	mA
I_{DDA}	analog supply current		140	165	210	mA
PLL						
$f_{clk(sys)}$	system clock frequency	$1792 \times f_{HSYNC}$	–	28	–	MHz
B_{loop}	loop bandwidth		–	4	–	kHz
t_{jitter}	short-term stability	peak-to-peak jitter for 64 μs	–	–	4	ns
ζ	damping factor		–	0.7	–	

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9081H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT317-2

BLOCK DIAGRAM

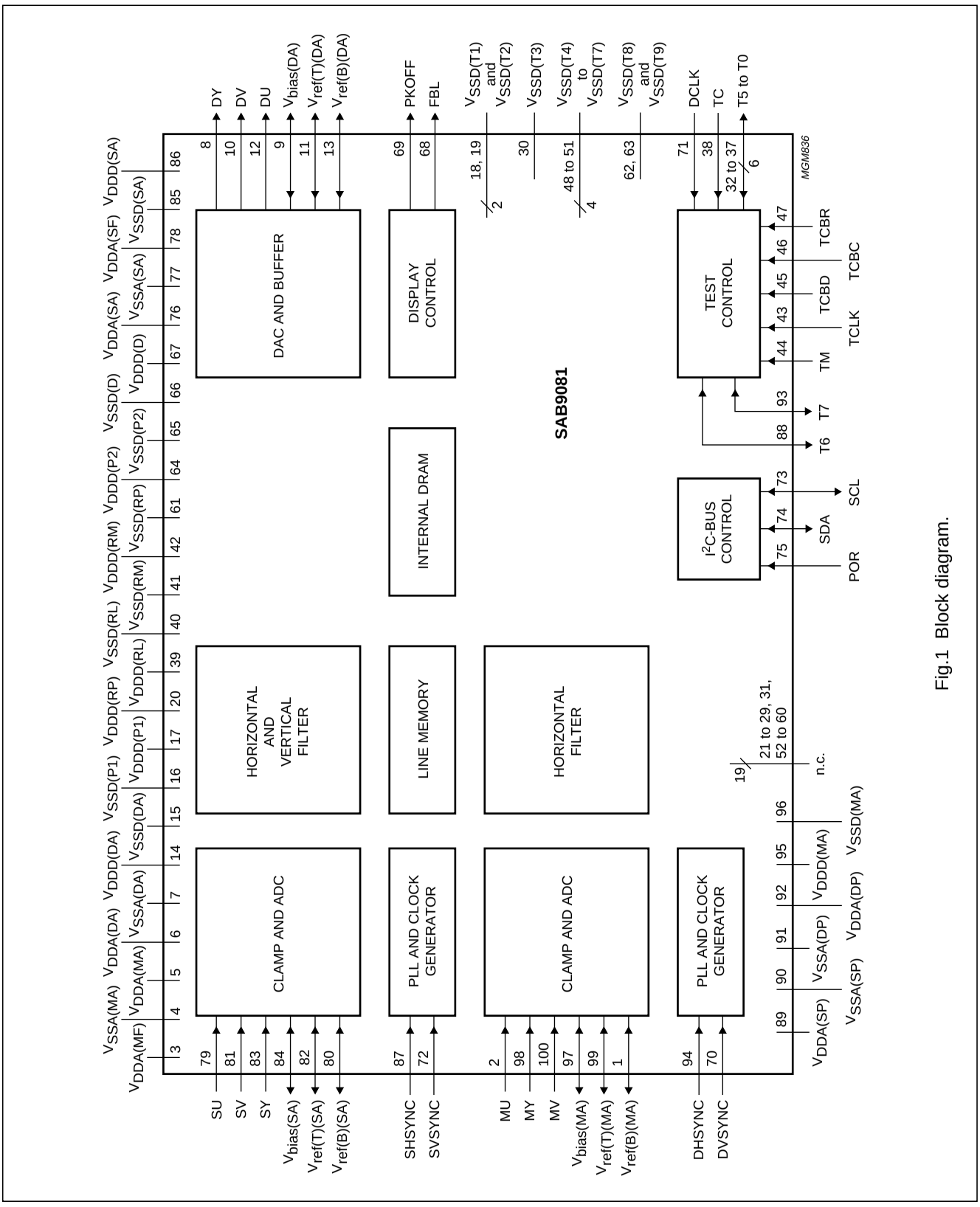


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
$V_{ref(B)(MA)}$	1	I/O	analog bottom reference voltage for main channel ADCs
MU	2	I	analog U input for main channel
$V_{DDA(MF)}$	3	S	analog supply voltage for main channel front-end buffers
$V_{SSA(MA)}$	4	S	analog ground for main channel ADCs
$V_{DDA(MA)}$	5	S	analog supply voltage for main channel ADCs
$V_{DDA(DA)}$	6	S	analog supply voltage for DACs
$V_{SSA(DA)}$	7	S	analog ground for DACs
DY	8	O	analog Y output of DAC
$V_{bias(DA)}$	9	I/O	input/output analog bias reference voltage for DACs
DV	10	O	analog V output of DAC
$V_{ref(T)(DA)}$	11	I/O	input/output analog top reference voltage for DACs
DU	12	O	analog U output of DAC
$V_{ref(B)(DA)}$	13	I/O	analog bottom reference voltage for DACs
$V_{DDD(DA)}$	14	S	digital supply voltage for DACs
$V_{SSD(DA)}$	15	S	digital ground for DACs
$V_{SSD(P1)}$	16	S	digital ground for periphery
$V_{DDD(P1)}$	17	S	digital supply voltage for periphery
$V_{SSD(T1)}$	18	S	digital ground for test
$V_{SSD(T2)}$	19	S	digital ground for test
$V_{DDD(RP)}$	20	S	digital supply voltage for memory periphery
n.c.	21 to 29	–	not connected
$V_{SSD(T3)}$	30	S	digital ground for test
n.c.	31	–	not connected
T5	32	I/O	test data input/output bit 5 (CMOS levels)
T4	33	I/O	test data input/output bit 4 (CMOS levels)
T3	34	I/O	test data input/output bit 3 (CMOS levels)
T2	35	I/O	test data input/output bit 2 (CMOS levels)
T1	36	I/O	test data input/output bit 1 (CMOS levels)
T0	37	I/O	test data input/output bit 0 (CMOS levels)
TC	38	I	test control input (CMOS levels)
$V_{DDD(RL)}$	39	S	digital supply voltage for memory logic
$V_{SSD(RL)}$	40	S	digital ground for memory logic
$V_{SSD(RM)}$	41	S	digital ground for memory core
$V_{DDD(RM)}$	42	S	digital supply voltage for memory core
TCLK	43	I	test clock input (CMOS levels)
TM	44	I	test mode input (CMOS levels)
TCBD	45	I	test control block data input (CMOS levels)
TCBC	46	I	test control block clock input (CMOS levels)
TCBR	47	I	test control block reset input (CMOS levels)
$V_{SSD(T4)}$ to $V_{SSD(T7)}$	48 to 51	S	digital ground for test

SYMBOL	PIN	TYPE	DESCRIPTION
n.c.	52 to 60	–	not connected
$V_{SSD(RP)}$	61	S	digital ground for memory periphery
$V_{SSD(T8)}$ and $V_{SSD(T9)}$	62 and 63	S	digital ground for test
$V_{DDD(P2)}$	64	S	digital supply voltage for periphery
$V_{SSD(P2)}$	65	S	digital ground for periphery
$V_{SSD(D)}$	66	S	digital ground for digital core
$V_{DDD(D)}$	67	S	digital supply voltage for digital core
FBL	68	O	fast blanking control signal output (CMOS levels; +5 V tolerant)
PKOFF	69	O	peak off control signal output (CMOS levels; +5 V tolerant)
DVSYNC	70	I	vertical sync display channel input (CMOS levels; +5 V tolerant)
DCLK	71	I	test clock input (28 MHz; CMOS levels)
SVSYNC	72	I	vertical sync for subchannel input (CMOS levels; +5 V tolerant)
SCL	73	I/O	input/output serial clock (I^2C-bus; CMOS levels; +5 V tolerant)
SDA	74	I/O	input/output serial data/acknowledge output (I^2C-bus; +5 V tolerant)
POR	75	I	power-on reset input (CMOS levels; pull-up resistor connected to V_{DD})
$V_{DDA(SA)}$	76	S	analog supply voltage for subchannel ADCs
$V_{SSA(SA)}$	77	S	analog ground for subchannel ADCs
$V_{DDA(SF)}$	78	S	analog supply voltage for subchannel front-end buffers and clamps
SU	79	I	analog U input for subchannel
$V_{ref(B)(SA)}$	80	I/O	input/output analog bottom reference voltage for subchannel ADCs
SV	81	I	analog V input for subchannel
$V_{ref(T)(SA)}$	82	I/O	input/output analog top reference voltage for subchannel ADCs
SY	83	I	analog Y input for subchannel
$V_{bias(SA)}$	84	I/O	analog bias reference voltage for subchannel ADCs
$V_{SSD(SA)}$	85	S	digital ground for subchannel ADCs
$V_{DDD(SA)}$	86	S	digital supply voltage for subchannel ADCs
SHSYNC	87	I	horizontal sync input for subchannel ($V_i < V_{SHSYNC}$)
T6	88	I/O	test data input/output bit 7 (CMOS levels)
$V_{DDA(SP)}$	89	S	analog supply voltage for subchannel PLL
$V_{SSA(SP)}$	90	S	analog ground for subchannel PLL
$V_{SSA(DP)}$	91	S	analog ground for display channel PLL
$V_{DDA(DP)}$	92	S	analog supply voltage for display channel PLL
T7	93	I/O	test data input/output bit 6 (CMOS levels)
DHSYNC	94	I	horizontal sync input for display channel ($V_i < V_{DHSYNC}$)
$V_{DDD(MA)}$	95	S	digital supply voltage for main channel ADCs
$V_{SSD(MA)}$	96	S	digital ground for main channel ADCs
$V_{bias(MA)}$	97	I/O	analog bias reference voltage for main channel ADCs
MY	98	I	analog Y input for main channel
$V_{ref(T)(MA)}$	99	I/O	analog top reference voltage for main channel ADCs
MV	100	I	analog V input for main channel

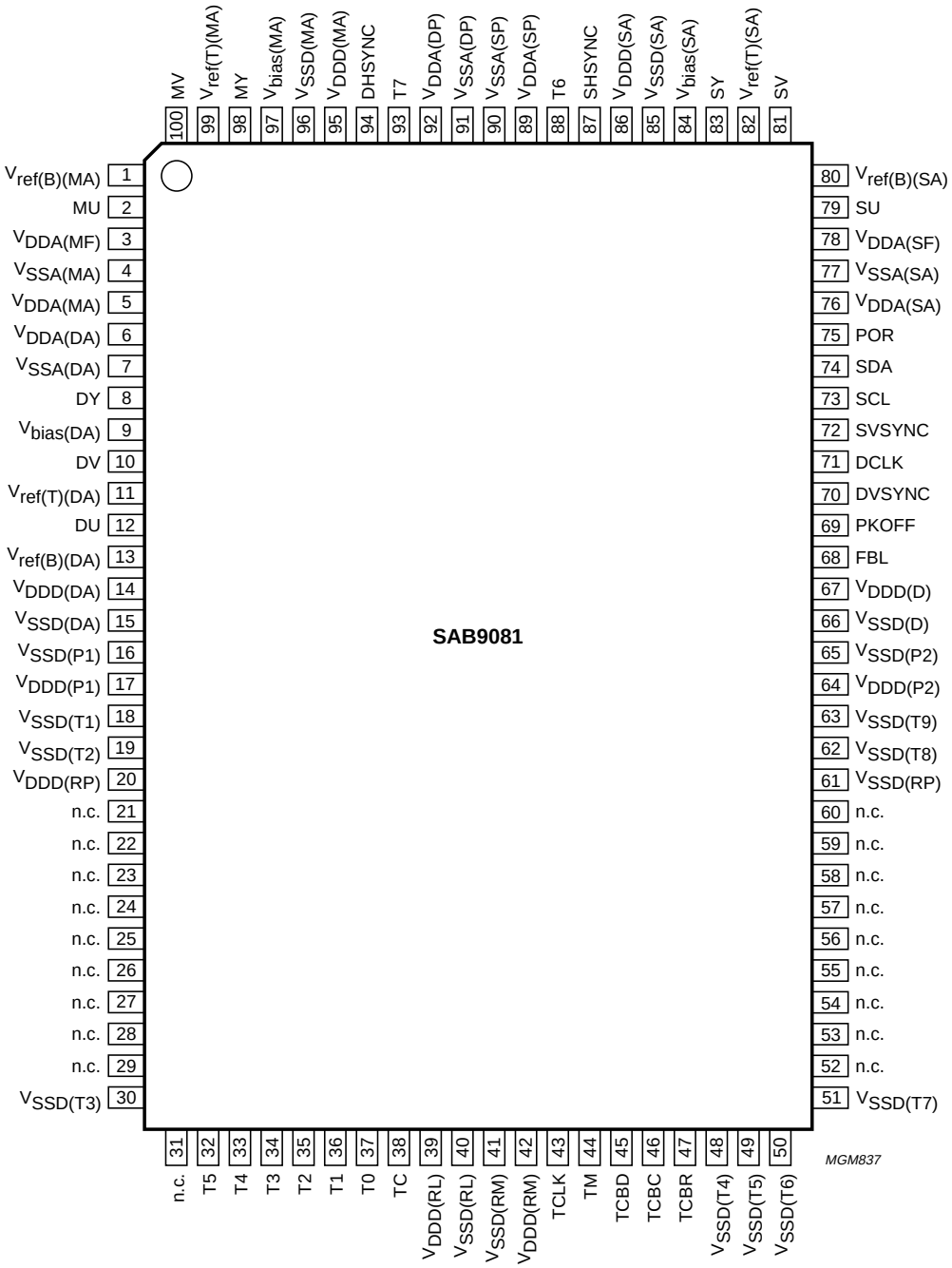


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Acquisition

The internal pixel rate is 28 MHz for the Y, U and V channels. It is expected that the bandwidth of the input signals will be limited to 4.5 MHz for the Y input and 1.125 MHz for the U and V inputs. Inset synchronisation is achieved via the acquisition HSYNC and VSYNC pins of the main channel. The display is driven by the main channel clock.

The starting-point of the acquisition can be controlled with the acquisition fine positioning added to a system constant. With a nominal input f_{HSYNC} and standard NTSC signals, 1408 samples (active video) are acquired and processed by the SAB9081. Here, the nominal input f_{HSYNC} results in a nominal system clock frequency of $1792 \times f_{HSYNC}$ (approximately 28 MHz).

PIP modes

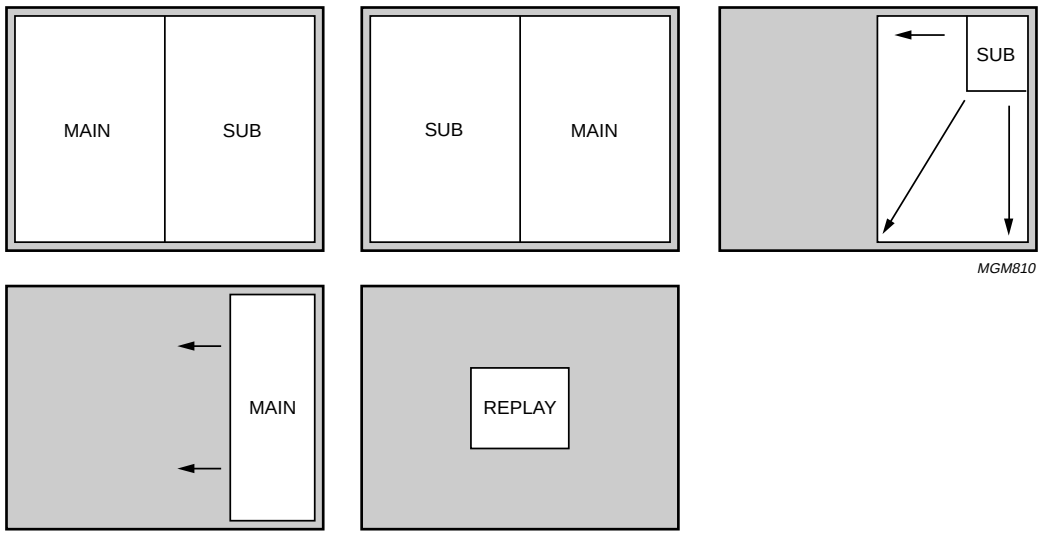


Fig.3 Pip modes.

I²C-bus description

The I²C-bus provides bidirectional 2-line communication between different ICs. The SDA line is the serial data line and the SCL the serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device.

Data transfer may be initiated only when the bus is not busy. The SAB9081 has the I²C-bus address 2CH. Valid subaddresses are 00H to 18H; register 15H (except bits 7 and 6) and registers 16H to 18H are reserved for future extensions.

I²C-bus control is according to the I²C-bus protocol: first, a START sequence must be put on the I²C-bus. Then, the I²C-bus address of the circuit must be sent, followed by a subaddress. After this sequence, the data of the subaddresses must be sent. An auto-increment function gives the option of sending data of the incremented subaddresses until a STOP sequence is sent. Table 1 gives an overview of the I²C-bus addresses. The data bits that are not used should be set to zero.

Table 1 Overview of I²C-bus addresses

For a description of the various data bits, see the following pages.

SUB ADDRESS	DATA BYTES							
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
00H	MPIPON	SPIPON	S1FLD	SFreeze	DNonint	PipMode2	PipMode1	PipMode0
01H	SHBlow1	SHBlow0	SHRed5	SHRed4	SHRed3	SHRed2	SHRed1	SHRed0
02H	SVBlow	SVRed6	SVRed5	SVRed4	SVRed3	SVRed2	SVRed1	SVRed0
03H	BGVfp3	BGVfp2	BGVfp1	BGVfp0	BGHfp3	BGHfp2	BGHfp1	BGHfp0
04H	SDHfp7	SDHfp6	SDHfp5	SDHfp4	SDHfp3	SDHfp2	SDHfp1	SDHfp0
05H	SDVfp7	SDVfp6	SDVfp5	SDVfp4	SDVfp3	SDVfp2	SDVfp1	SDVfp0
06H	–	–	–	–	–	–	–	–
07H	–	–	–	–	–	–	–	–
08H	MAHfp3	MAHfp2	MAHfp1	MAHfp0	SAHfp3	SAHfp2	SAHfp1	SAHfp0
09H	SAVfp7	SAVfp6	SAVfp5	SAVfp4	SAVfp3	SAVfp2	SAVfp1	SAVfp0
0AH	DUVPol	DVSPol	DFPol	DHsync	SUVPol	SVSPol	SFPol	SHsync
0BH	MainFidPos7	MainFidPos6	MainFidPos5	MainFidPos4	MainFidPos3	MainFidPos2	MainFidPos1	MainFidPos0
0CH	SubFidPos7	SubFidPos6	SubFidPos5	SubFidPos4	SubFidPos3	SubFidPos2	SubFidPos1	SubFidPos0
0DH	BGOn	BOn	MFidPOn	SFidPOn	Prio	AlgOff	SFBlkPkOff1	SFBlkPkOff0
0EH	BSel1	BSel0	SBBrt1	SBBrt0	–	SBCol2	SBCol1	SBCol0
0FH	DPal	SPal	SLSel5	SLSel4	SLSel3	SLSel2	SLSel1	SLSel0
10H	I2CHold	SV1	SDSel5	SDSel4	SDSel3	SDSel2	SDSel1	SDSel0
11H	MDHfp7	MDHfp6	MDHfp5	MDHfp4	MDHfp3	MDHfp2	MDHfp1	MDHfp0
12H	MDVfp7	MDVfp6	MDVfp5	MDVfp4	MDVfp3	MDVfp2	MDVfp1	MDVfp0
13H	MHBlow	SV2	MHRed5	MHRed4	MHRed3	MHRed2	MHRed1	MHRed0
14H	–	VBwidth2	VBwidth1	VBwidth0	SV3	HBwidth2	HBwidth1	HBwidth0
15H	DNTSC	SNTSC	all bits are reserved					
16H to 18H	all bits are reserved							

MPIPON (DOUBLE WINDOW)

Bit MPIPON is used to switch the main channel PIP on (logic 1) or off (logic 0).

SPIPON

Bit SPIPON is used to switch the subchannel PIPs on (logic 1) or off (logic 0).

PRIO

The priority bit decides whether the main channel PIP (Prio set to logic 0) or the subchannel PIP (Prio set to logic 1) will be on top when both PIPs overlap.

S1FLD

If S1FLD is set to logic 0, two fields are used for the live PIP. When a 50/60 Hz or a 60/50 Hz mode is detected, the SAB9081 automatically switches to the 1-Field mode (1-Field resolution vertically).

If S1FLD is set to logic 1, only one field is used. This causes joint line errors but saves memory. This bit should not be set in normal modes.

SFREEZE

With SFreeze set to logic 1, the current live subchannel PIP will be frozen. If set to logic 0, it is unfrozen.

ALGOFF

In double window mode, precautions are taken to prevent a joint line error. Under some conditions, this feature should be switched off. This can be realized by setting this bit to logic 1. Normally, bit AlgOff should be set to logic 0. Bit SV3, when set to logic 0, can overrule bit AlgOff. It is recommended to set SV3 to logic 1.

DNONINT

In normal mode (this bit is logic 0), the SAB9081 calculates whether a signal is non-interlaced and reacts accordingly. With bit DNonint set to logic 1, the display channel is forced into the non-interlaced mode. In the non-interlaced mode, only one field is used during the processing of the PIPs.

PIPMODE

Bits PipMode<2:0> determine the PIP modes for the SAB9081, as shown in Table 2.

Table 2 PIP modes

PipMode<2:0>	MODE
000	double window mode
001	replay mode

SHRED AND SVRED (DOUBLE WINDOW)

Bits SHRed<5:0> and SVRed<6:0> determine the reduction factors in the double window mode.

The horizontal reduction is equal to SHRed/96; the vertical reduction is equal to SVRed/96. SHRed should lie in the range from 0 to 48; if set to logic 0, the PIP is off. SVRed should lie in the range from 0 to 96; if set to logic 0, the PIP is off.

When the horizontal reduction factor is 48/96, 704 samples are processed. The horizontal reduction is linear; therefore, when it is 24/96, 352 samples are processed. The same holds for the vertical reduction factor but then with the number of lines. For NTSC, the number of processed lines can be calculated from SVRed/96 $\times$ 228 lines; for PAL, this is SVRed/96 $\times$ 276 lines.

SHRED AND SVRED (REPLAY)

In the replay mode, the ranges of SHRed and SVRed are limited as follows: SHRed = 12; SVRed = 24, 16 or 12. This leads to a fixed horizontal reduction factor of 1⁄8; and to a variable vertical reduction factor of 1⁄4, $\frac{1}{6}$ or $\frac{1}{8}$.

Note that the resulting replay PIP can be expanded by using bits SHBlow and/or SVBlow.

BGHFP AND BGVFP

These bits control the horizontal and vertical positioning of the PIP configuration on the screen. The horizontal range is adjustable in 16 steps of four 28 MHz clock periods. The vertical range is 16 steps of 1 line/field. The background colour can be adjusted with bits BSel, SBBrt and SBCol.

SDHFP AND SDVFP

These bytes control the horizontal and vertical positioning of the subchannel PIPs on the screen. The horizontal range is 256 steps of eight 28 MHz clock periods. The vertical range is 256 steps of 1 line/field.

MAHFP, SAHFP AND SAVFP

Bits MAHfp<3:0>, bits SAHfp<3:0> and byte SAVfp control the horizontal and vertical inset starting-points of the acquired data. The horizontal range is 16 steps of eight 28 MHz clock periods when SV2 is set to logic 1. When SV2 is set to logic 0, the horizontal range is restricted to eight steps. The vertical range is 256 steps of 1 line/field.

DUVPOL, DVSPOL, DFPOL AND DHSYNC

These bits control the PLL/deflection settings. With DUVPol, the polarity of the border UV signals can be inverted when the deflection circuit after the SAB9081 expects inverted signals.

With DVSPol set to logic 0, the SAB9081 triggers on positive edges of the DVSYNC. If DVSPol is set to logic 1, it triggers on negative edges. DFPol can invert the field ID of the incoming fields. Bit DHsync determines the timing of the DHSYNC pulse. If it is set to logic 0, a burstkey is expected; if it is set to logic 1, a horizontal sync is expected at pin DHSYNC.

SUVPOL, SVSPOL, SFPOL AND SHSYNC

These bits control the PLL/decoder settings. With SUVPol, the polarity of the video UV signals can be inverted when the decoder circuit before the SAB9081 emits inverted signals.

With SVSPol set to logic 0, the SAB9081 triggers on positive edges of the SVSYNC. If it is set to logic 1, it triggers on the negative edges. SFPol can invert the field ID of the incoming fields. Bit SHsync determines the timing of the SHSYNC pulse. If it is set to logic 0, a burstkey is expected; if it is set to logic 1, a horizontal sync is expected at pin SHSYNC.

MFIDPON AND SFIDPON

Bits MFidPOn (main field identification position on) and SFidPOn (subfield identification position on) enable the field identification position fine tuning. The default value is off (logic 0), no fine positioning. When on (logic 1), the field identification position is determined by the value of bytes MainFidPos and SubFidPos.

BGON

Bit BGOn determines whether the background is visible. The background has a size of 720 pixels and 240 lines for NTSC and 720 pixels and 288 lines for PAL. The background colour can be adjusted with bits BSel, SBBrt and SBCol.

BON, SBBRT, SBCOL AND BSEL

Bit BOn can switch the sub-borders on (logic 1) or off (logic 0). Bits SBBrt<1:0> and SBCol<2:0> set the brightness and colour type of the selected border. The brightness is set in four levels of 30%, 50%, 70% and 100% IRE. The colour type is one of black (grey), blue, red, magenta, green, cyan, yellow or white (grey). For black and white, a finer scale is available.

BSel selects which colour is set, background or border, see Table 3.

Table 3 BSel modes

BSel<1:0>	BORDER COLOUR SET
00	main
01	sub
10	background
11	sub-border select

MDHFP AND MDVFP

These bytes control the horizontal and vertical positioning of the main PIP on the screen. The horizontal range is 256 steps of eight 28 MHz clock periods. The vertical range is 256 steps of 1 line/field.

MHRED

Bits MHRed<5:0>, in a range from 0 to 48, determine the horizontal reduction factor MHRed/96. If they are set to logic 0, the PIP is off. If they are set to the maximum value of 48, the horizontal reduction factor is 0.5.

SHBLOW AND SVBLOW (REPLAY MODE)

Bits SHBlow<5:0> and bit SVBlow are used in the replay mode. These bits can expand a pixel on the display side by a factor two (01) or four (11) in the horizontal direction (SHBlow) and a factor of two (1) in the vertical direction (SVBlow). Zero values indicate no expansion.

MHBLOW

Bit MHBlow can expand the main picture by a factor of two in the horizontal direction.

SLSEL (REPLAY MODE)

In the replay PIP mode, bits SLSel<5:0> determine at which memory location the PIP data is written, the range depends on the memory usage for each PIP.
The maximum number of PIPs that can be stored in NTSC mode is 42.

SDSEL (REPLAY MODE)

Bits SDSel<5:0> select which PIP is read from memory. Valid numbers are dependent on the maximum value of SLSel.

DPAL AND SPAL

In normal operation (DPal and SPal are logic 0), the SAB9081 calculates from the number of incoming lines whether the signal is NTSC (< 288 lines) or PAL (≥ 288 lines).

If DPal is set to logic 1, the main window is sized to 276 lines. If DPal is set to logic 1 and the subchannel is still NTSC, the subchannel picture will be smaller than the main channel picture (difference of approximately 40 lines).

If SPal is set to logic 1, the subchannel is forced to PAL mode and 276 lines are acquired instead of 228 in NTSC mode.

DNTSC AND SNTSC

In normal operation (DNTSC and SNTSC are logic 0), the SAB9081 calculates from the number of incoming lines whether the signal is NTSC (< 288 lines) or PAL (≥ 288 lines).

If DNTSC is set to logic 1, the main window is sized to 228 lines. If DNTSC is set to logic 1 and the subchannel is still PAL, the subchannel picture will be larger than the main channel picture (difference of approximately 40 lines).

If SNTSC is set to logic 1, the channel is forced to NTSC mode and 228 lines are acquired instead of 276 in PAL mode.

SFBLKPKOFF

Bits SFBlkPkOff<1:0> shift signals FBL and PKOFF with respect to the YUV output, by half pixels, see Table 4.

Table 4 Shifts of FBL and PKOFF

SFBlkPkOff<1:0>	SHIFT OF FBL AND PKOFF
00	no shift
01	+0.5 pixel
10	–0.5 pixel
11	–1 pixel

I2CHOLD

Bit I2CHold controls the updating of the I^2C-bus controlled function towards the PIP. If set to logic 1, some updates are on hold until the bit is set to logic 0. At the next main Vsync, all settings are passed to the PIP functions.

The bits and bytes that are on hold when the I2CHold bit is set to logic 1 are:

- MPIPON, SPIPON, DNonint and PipMode
- SHBlow and SVBlow
- SHRed and SVRed
- BGHfp and BGVfp
- SDHfp and SDVfp
- SHPic and SVPic
- BGOn, BOn and Prio
- BSel, SBBrt and SBCol
- SDSel
- MDHfp and MDVfp
- HBWidth and VBWidth.

SV1

Bit SV1 controls the internal horizontal offset of the background. When set to logic 0, the offset is 0.86 µs; when set to logic 1, the offset is 4.56 µs.

SV2

Bit SV2, when set to logic 0, limits the range of the MAHfp and SAHfp parameters. Otherwise (bit SV2 set to logic 1), the parameters have their maximum range (which is recommended).

SV3

Bit SV3, when set to logic 0, can overrule bit AlgOff when the main channel is NTSC and the subchannel is PAL. In this particular case, bit AlgOff is always set to logic 0 internally. Otherwise (bit SV3 set to logic 1), bit AlgOff is never overruled. It is recommended to set SV3 to logic 1.

HBWIDTH AND VBWIDTH

Bits HBWidth<2:0> and VBWidth<2:0> control the horizontal and vertical border sizes in steps of two pixels and one line. The default horizontal border size is four pixels and the vertical border size is two lines per field. Default means after power-up and no I^2C-bus data sent to the PIP controller.

NOTES

1. When the input signals for the main and/or subchannel are non-interlaced, joint line errors can occur. When non-interlaced signals are input, the SAB9081 switches automatically to the non-interlaced mode.
2. When the prevent joint line error algorithm is switched off (AlgOff is set to logic 1), joint line errors can still occur in the 2-Field mode.
3. When a PAL signal is applied to the main channel and an NTSC signal is applied to the subchannel, the subchannel will automatically enter the 1-Field mode. Now, a joint line error can occur. In the PAL/NTSC mode, the subpicture will be smaller than the main picture (difference of approximately 40 lines).
4. When an NTSC signal is applied to the main channel and a PAL signal is applied to the subchannel, the subchannel will automatically enter the 1-Field mode. Now, a joint line error can occur. In the NTSC/PAL mode, the subpicture will be larger than the main picture (difference of approximately 40 lines).

Acquisition channel ADCs and clamping

The analog input signals are converted to digital signals by three ADCs per channel. The resolution of the ADCs is 8 bits (DNL is 7 bits and INL is 6 bits) and the sampling is performed at the system clock frequency of 28 MHz for the Y input. A bias voltage (V_{bias}) is used to decouple the AC components on internal references.

The inputs should be AC coupled and an internal clamp circuit (using external clamp capacitors) will clamp the input to a level derived internally from $V_{ref(B)(MA/SA)}$ for the luminance channels and, for the chrominance channels, to $(V_{ref(T)(MA/SA)} + V_{ref(B)(MA/SA)})/2$ + LSB/2. The clamping starts at the active edge of the burst key. Internal video buffers amplify the standard Y, U and V input signals to the correct ADC levels.

PLL

The PLL generates an internal system clock of $1792 \times f_{HSYNC}$, from the HSYNC, which is approximately 28 MHz.

DACs and video buffers

The 28 MHz digital video signals are fed to the 8-bit DACs that produce the required analog video signals. The video buffers amplify these signals prior to being fed to the output to drive another device.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	–0.5	5.0	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	ambient temperature	0	70	°C
V_{esd}	electrostatic discharge handling	–	2	kV
$R_{th(j-a)}$	thermal resistance	–	45	K/W
P_{max}	maximum power dissipation	–	1.0	W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611, Part E”*, dated 14 December 1992.

ESD LEVELS

The standard ESD specification is JEDEC Class II (2 kV Human Body Model, 200 V Machine Model) unless indicated otherwise.

Table 5 ESD performance

PIN	SYMBOL	HUMAN BODY MODEL (V)	MACHINE MODEL (V)
68	FBL	1000	standard specification
69	PKOFF	1000	
70	DVSYNC	1000	
72	SVSYNC	1000	
73	SCL	1000	
74	SDA	1000	
rest in range 1 to 17	all other pins	standard specification	
rest in range 64 to 100			

ANALOG CHARACTERISTICS

V_{DDA} = 3.3 V; V_{DDD} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	positive supply voltage		3.0	3.3	3.6	V
V_{SSA}	ground voltage		–	0	–	V
$\Delta V_{DDA(max)}$	maximum DC difference between supply voltages		–	0	100	mV
$\Delta V_{SSA(max)}$	maximum DC difference between ground voltages		–	0	100	mV
$I_{DDD(q)}$	quiescent current of digital supply voltages	note 1	–	0	50	µA
$I_{DDA(DP)}$	display PLL supply current		–	0.4	–	mA
$I_{DDA(SP)}$	sub PLL supply current		–	0.4	–	mA
$I_{DDA(MA)}$	main ADCs supply current	note 2	60	70	90	mA
$I_{DDA(SA)}$	sub ADCs supply current	note 2	60	70	90	mA
$I_{DDA(DA)}$	DACs supply current		8	10	12	mA
$I_{DDA(MF)}$	main buffers supply current		4	6	9	mA
$I_{DDA(SF)}$	sub buffers supply current		4	6	9	mA
$I_{DDA(tot)}$	total analog supply current	note 2	140	165	210	mA
$I_{DDD(tot)}$	total digital supply current		–	50	–	mA
Analog-to-digital converter and clamping						
$V_{ref(T)}$	top reference voltage	note 3	2.70	2.82	2.95	V
$V_{ref(B)}$	bottom reference voltage	note 3	0.95	1.07	1.20	V
$V_{iY(p-p)}$	Y input signal amplitude (peak-to-peak value)	note 4	–	1.00	1.04	V
$V_{i(V)(p-p)}$	V input signal amplitude (peak-to-peak value)	note 4	–	1.05	1.10	V
$V_{i(U)(p-p)}$	U input signal amplitude (peak-to-peak value)	note 4	–	1.33	1.38	V
I_i	input current	clamping off	–	0.1	–	µA
		clamping on	–	55	–	µA
C_i	input capacitance		–	5	–	pF
f_{sample}	sample frequency	note 5	–	$1792 \times f_{HSYNC}$	–	kHz
RES	resolution		8	8	8	bit
DNL	differential non-linearity		–1.4	–	+1.4	LSB
INL	integral non-linearity		–2.0	–	+2.0	LSB
α_{cs}	channel separation		–	48	–	dB
$V_{clamp(Y)}$	Y clamping voltage level	note 6	1.25	1.34	1.45	V
$V_{clamp(U,V)}$	U/V clamping voltage level	note 7	1.80	1.93	2.15	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter and output stage						
$V_{ref(T)}$	top reference voltage		1.10	1.20	1.30	V
$V_{ref(B)}$	bottom reference voltage		0.15	0.23	0.30	V
R_L	load resistance		1	–	1000	kΩ
C_L	load capacitance		0	–	5	pF
f_{sample}	sample frequency	note 8	–	$1792 \times f_{HSYNC}$	–	kHz
RES	resolution		8	8	8	bit
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
α_{cs}	channel separation		–	48	–	dB
Display PLL and clock generation						
$f_{i(PLL)}$	input frequency					
	NTSC		14	15.75	17	kHz
	PAL		14	15.625	17	kHz
Sub PLL and clock generation						
$f_{i(subPLL)}$	input frequency					
	NTSC		14	15.75	17	kHz
	PAL		14	15.625	17	kHz

Notes

1. Digital clocks are silent, input pins POR and TM are connected to V_{DDA}.
2. This value is measured with an external bias resistor of 39 kΩ, resulting in a bias current of 55 μA.
3. Voltages $V_{ref(T)}$ and $V_{ref(B)}$ are made by a resistor division of V_{DDA}. They can be calculated with the formulas:

   $$V_{ref(T)} = V_{DDA} \times \frac{2.82}{V_{DDA(nom)}} V \text{ and } V_{ref(B)} = V_{DDA} \times \frac{1.07}{V_{DDA(nom)}} V .$$

4. The input signals are amplified to meet an internal peak-to-peak voltage level of $0.8 \times (V_{ref(T)} - V_{ref(B)})$, which equals the internal ADC input range.
5. The internal system clock frequency is $1792 \times f_{HSYNC}$ of the input channel.
6. The Y clamp level is not equal to the $V_{ref(B)}$ of the ADCs.
7. The UV channels are clamped to: $\frac{V_{ref(B)} + V_{ref(T)} + V_{LSB}}{2}$.
8. The internal system clock frequency is $1792 \times f_{HSYNC}$ of the main channel.

DIGITAL CHARACTERISTICS

V_{DDA} = 3.3 V; V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC characteristics						
V_{IH}	HIGH-level input voltage					
	default		$0.8V_{DDD}$	–	V_{DDD} + 0.5	V
	pin 74		$0.8V_{DDD}$	–	5.5[1]	V
	5 V tolerant pins 68, 69, 70, 72, 73		$0.8V_{DDD}$	–	5.5[1]	V
V_{IL}	LOW-level input voltage	default	–0.5	–	$0.2V_{DDD}$	V
V_{hys}	hysteresis voltage		0.8	–	–	V
V_{OH}	HIGH-level output voltage	I_{OH} = –X mA; V_{DDD} = 3.0 V; note 2	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = X mA; V_{DDD} = 3.0 V; note 2	–	–	0.4	V
		I_{OL} = 2 mA; V_{DDD} = 3.0 V	–	–	0.4	V
$\|I_{LI}\|$	input leakage current	V_I = 0 V	–	–	1	µA
		$V_I = V_{DDD}$	–	–	1	µA
$\|I_{OZ}\|$	3-state output leakage current	V_O = 0 V or $V_O = V_{DDD}$	–	–	1	µA
$I_{lu(I/O)}$	I/O latch-up current	V < 0 V; V > V_{DDD}	200	–	–	mA
R_{pu}	internal pull-up resistor		16	33	78	kΩ
AC characteristics						
$f_{clk(sys)}$	system clock frequency	note 3	–	$1792 \times f_{HSYNC}$	–	kHz
t_r	rise time		–	6	25	ns
t_f	fall time		–	6	25	ns

Notes

1. The absolute maximum input voltage is 6.0 V.
2. X is the source/sink current under worst case conditions. X is reflected in the name of the I/O cell according to the drive capability. Minimum value of X is 1 mA.
3. The internal system clock frequency is $1792 \times f_{HSYNC}$ of the main channel and subchannel.

TEST AND APPLICATION INFORMATION

Figure 4 gives the application diagram in a standard configuration. Input signals main channel CVBS and subchannel CVBS from different video sources are processed by the SAB9081 and inserted by the YUV to RGB switch.

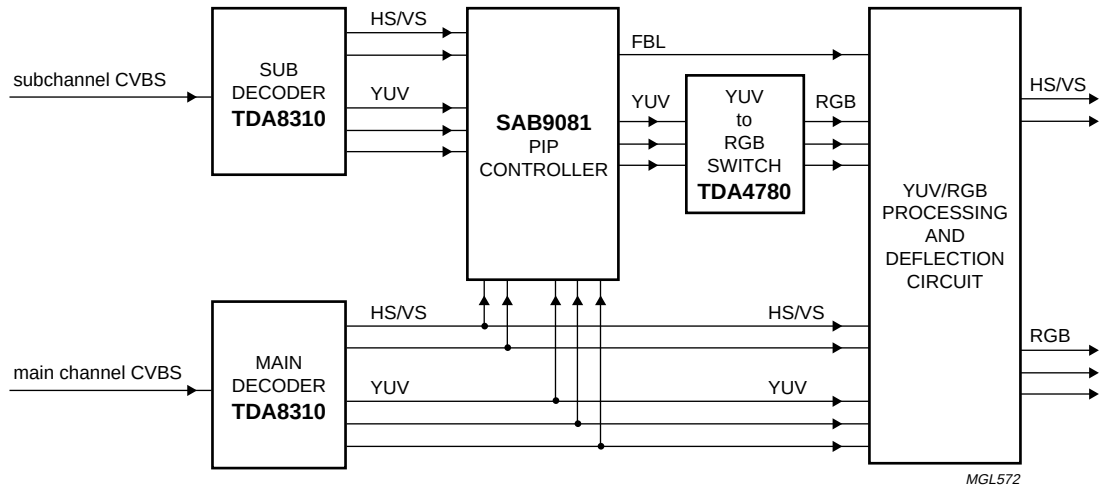
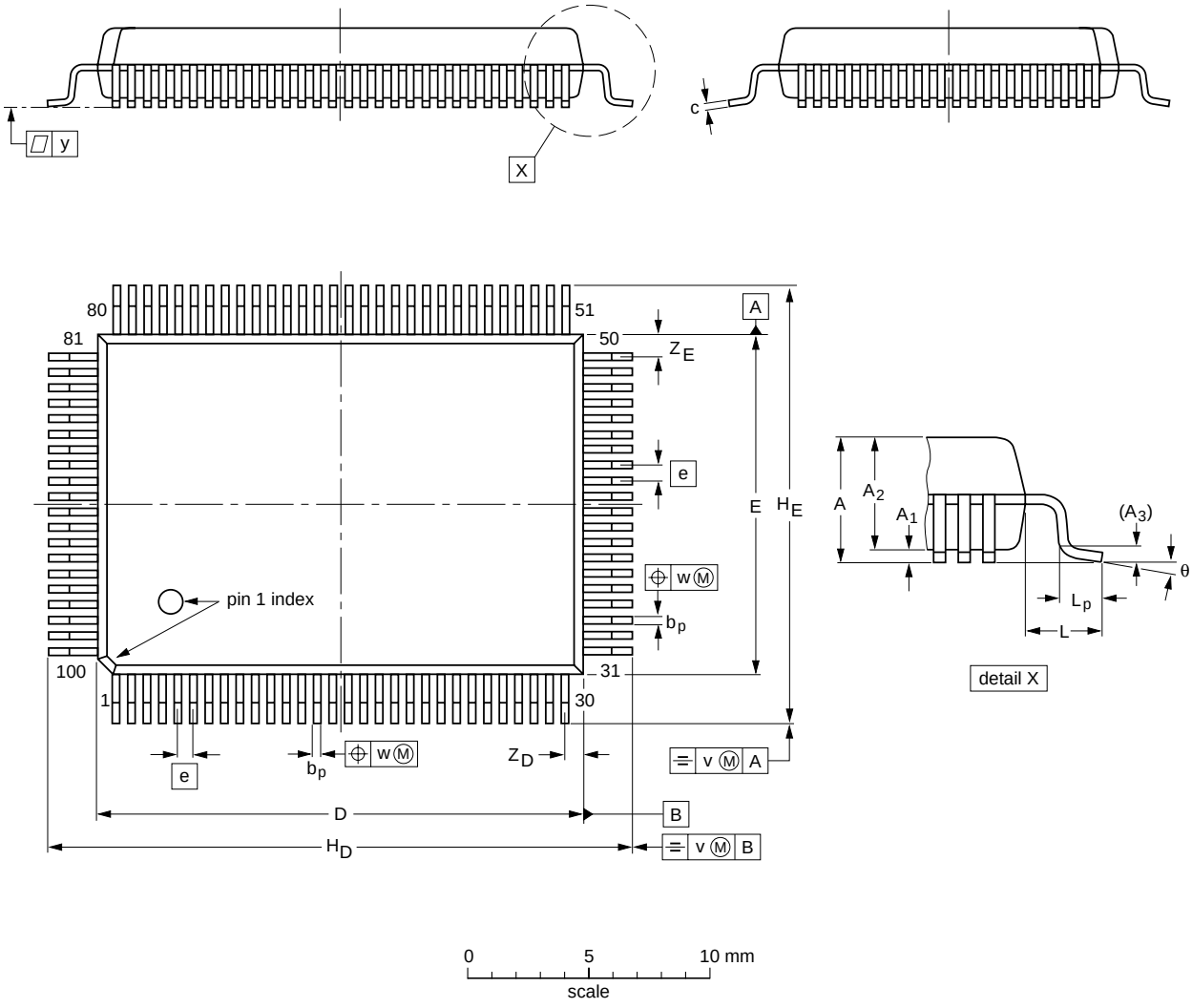


Fig.4 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 545004/25/02/pp24 Date of release: 1999 Nov 12 Document order number: 9397 750 06137

Let's make things better.

Philips Semiconductors

PHILIPS