NEC
NEC Electronics Inc.

μPD9513AD/9514AD
CMOS SERIAL INTERFACE CODEC-FILTER COMBINATION

April 1987

Description

The μPD9513AD and μPD9514AD are monolithic PCM codecs with integrated filters. These devices provide transmit A/D and receive D/A conversions of vf signals using companded μ-law or A-law format. They interface the PCM highway through serial ports.

At the vf input, the transmit section includes an adjustable-gain operational amplifier, a lowpass antialiasing filter, and a 200-3400 Hz bandpass filter. The filtered signal is sampled and encoded using a very accurate dc reference voltage. An autozero circuit corrects for dc offset.

The receive section reconstructs an analog signal from the companded digital signal and passes the signal through a 3400-Hz lowpass filter that corrects for the (sin x)/x response of the decoder output. A balanced power amplifier at the analog vf receive port allows maximum flexibility in output configurations.

The μPD9513AD and 9514AD can operate in fixed or variable data rate mode. In the fixed data rate mode, the master receive clock and the PCM data clock are selected as 1.536, 1.544, or 2.048 MHz. In the variable data rate mode, the PCM data clock can vary from 64 kHz to 2.048 MHz. The μPD9514AD allows asynchronous master transmit and receive clocks; the μPD9513AD uses one master clock for both transmit and receive sections. The μPD9514AD also has analog loopback and signaling capabilities.

The μPD9513AD and 9514AD are most suited to telecommunications applications. They are ideal for D3/D4 type channel banks and subscriber carrier systems, digital PBXs and central office switching systems, and digital telephone handsets. Their wide dynamic range makes them attractive for any application requiring digital processing of vf signals.

Packaged in a 24-pin DIP, the μPD9514AD offers more capability and flexibility. The μPD9513AD in a 20-pin DIP offers higher-density packaging.

Ordering Information

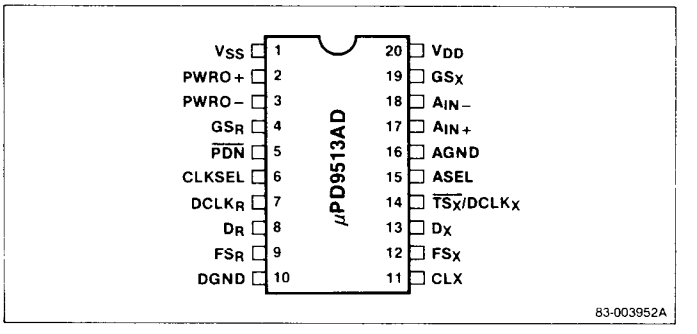
Part No.	Package Type	Signaling
μPD9513AD	20-pin ceramic DIP (300 mil)	No
μPD9514AD	24-pin ceramic DIP (600 mil)	Yes

Features

- ☐ Complete codec and filtering in a single chip
  - — Transmit highpass and lowpass filters
  - — Transmit op amp for gain adjustment
  - — Receive lowpass filter with (sin x)/x correction
  - — Receive output power amplifier
  - — Autozero circuit
  - — Highly-accurate reference voltage
  - — μ-law or A-law selectable by pin connection
  - — Serial digital I/O interface
- ☐ Two timing modes
  - — Fixed data rate mode (1.536, 1.544, or 2.048 MHz)
  - — Variable data rate mode (64 kHz to 2.048 MHz)
- ☐ Meets or exceeds D3/D4 and CCITT specifications
- ☐ Low power consumption
  - — 80 mW in normal operation
  - — 8 mW in power-down mode

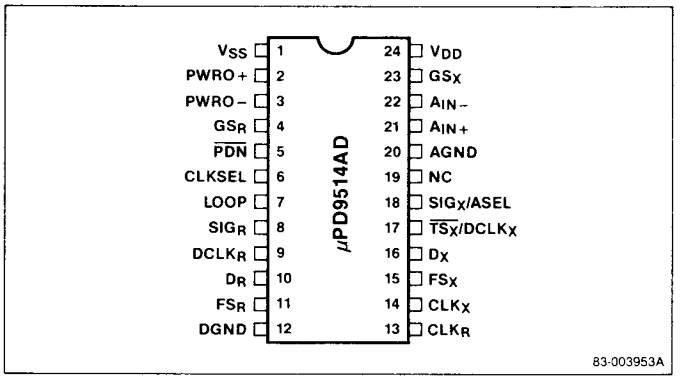
Pin Configurations

20-Pin Ceramic DIP



83-003952A

24-Pin Ceramic DIP



83-003953A

Pin Identification

Pin No. 9513AD	Pin No. 9514AD	Symbol	Function
1	1	V_{SS}	Negative supply voltage, −5 V
2	2	PWRO+	Receive power amplifier, noninverting output
3	3	PWRO−	Receive power amplifier, inverting output
4	4	GS_R	Receive power amplifier, gain set resistor
5	5	$\overline{PDN}$	Power-down select input
6	6	CLKSEL	Master clock select (by strapping)
	7	LOOP	Analog loopback control input
	8	SIG_R	Receive signaling output
7	9	$DCLK_R$	Receive PCM data clock input; or fixed data rate mode select (by strapping)
8	10	D_R	Receive PCM input
9	11	FS_R	Receive 8-kHz frame sync clock input
10	12	DGND	Digital ground; not tied to analog ground internally
	13	CLK_R	Receive master clock input
11		CLK	Master clock input
	14	CLK_X	Transmit master clock input
12	15	FS_X	Transmit 8-kHz frame sync clock input
13	16	D_X	Transmit PCM output
14	17	$\overline{TS_X}$	Transmit channel time slot strobe output (fixed rate mode)
		$DCLK_X$	Transmit PCM data clock input (variable data rate mode)
15		ASEL	A-law select (by strapping)
	18	ASEL	A-law select (by strapping)
		SIG_X	Transmit signaling input when A-law is not selected
	19	NC	No connection
16	20	AGND	Analog ground; not tied to digital ground internally
17	21	A_{IN+}	Transmit op amp analog input, noninverting
18	22	A_{IN-}	Transmit op amp analog input, inverting
19	23	GS_X	Transmit op amp, gain set resistor
20	24	V_{DD}	Positive supply voltage, +5 V

Pin Functions

The information that follows adds to the brief descriptions in the pin identification table.

Receive Output [PWRO+ and PWRO−]

The balanced 600-ohm output of the receive power amplifier is between PWRO+ and PWRO−. Either PWRO+ or PWRO− can be used as an unbalanced 300-ohm output.

Receive Gain Set [GS_R]

External resistors connecting PWRO+, PWRO−, and GS_R set the receive power amplifier gain between 0 and −12 dB.

Power-Down Select [$\overline{PDN}$]

Low logic level on $\overline{PDN}$ selects the power-down mode.

Master Clock Select [CLKSEL]

Strap CLKSEL (pin 6) according to the master clock frequency (CLK or CLK_X and CLK_R).

Frequency	Strap Pin 6 to
2.048 MHz	V_{SS}
1.544 MHz	DGND
1.536 MHz	V_{DD}

Analog Loopback Control [LOOP]

Applying high logic level to the LOOP pin activates analog loopback. Internally, the receive output is looped back to the transmit input; connections are PWRO+ to A_{IN+}, PWRO− to GS_R, and GS_X to A_{IN-}.

Receive Signaling [SIG_R]

In the receive section, bit 8 of the channel word in each signaling frame is extracted and held latched until updated in the next signaling frame. The signaling state is output continuously on the SIG_R pin.

Data Rate Mode Select [$DCLK_R$].

Strapping $DCLK_R$ to V_{SS} selects the fixed data rate mode. Omitting the strap selects the variable data rate mode and the $DCLK_R$ pin becomes the input for the receive PCM data clock, which is 64 kHz to 2.048 MHz.

Receive PCM Input [D_R]

During the proper channel time slot defined by receive frame sync clock FS_R, the eight-bit channel word is clocked in from the PCM highway at the PCM data clock rate. The PCM data clock is $DCLK_R$ in the variable data rate mode and CLK (9513AD) or CLK_R (9514AD) in the fixed data rate mode.

Receive Frame Sync Clock [FS_R]

This 8-kHz clock defines the time slot of a particular channel in the frame. In the fixed data rate mode, the clock pulse is double width in signaling frames. In the variable data rate mode, the clock remains high during the entire time slot.

If the FS_R pin is held low for 300 ms, the receive section enters the standby mode.

Receive Master Clock [CLK_R]

The receive master clock input to the μPD9514AD may be 2.048, 1.544, or 1.536 MHz. (The CLKSEL pin is strapped accordingly.)This clock controls the decoder and filter in the receive section. If the data rate is fixed, it also clocks in data from the PCM highway.

Master Clock [CLK]

In the μPD9513AD, the CLK input serves as master clock to the transmit and receive sections.

Transmit Master Clock [CLK_X]

The transmit master clock input to the μPD9514AD may be 2.048, 1.544, or 1.536 MHz. It controls the coder and filter in the transmit section and, if the data rate is fixed, clocks data out to the PCM highway.

Transmit Frame Sync Clock [FS_X]

This 8-kHz clock functions in the transmit section the same as FS_R in the receive section.

Transmit PCM Output [D_X]

During the proper channel time slot as defined by the 8-kHz frame sync clock FS_X, the eight-bit channel word is clocked onto the PCM highway by eight consecutive rising edges of CLK or CLK_X (fixed data rate mode) or $DCLK_X$ (variable data rate mode).

Transmit Timeslot Strobe [$\overline{TS_X}$]

In the fixed data rate mode, the $\overline{TS_X}$ pin is an open-drain output that goes low during the output of the channel word at D_X.

Transmit Data Clock [$DCLK_X$]

In the variable data rate mode, $DCLK_X$ is the transmit PCM data clock, variable from 64 kHz to 2.048 MHz.

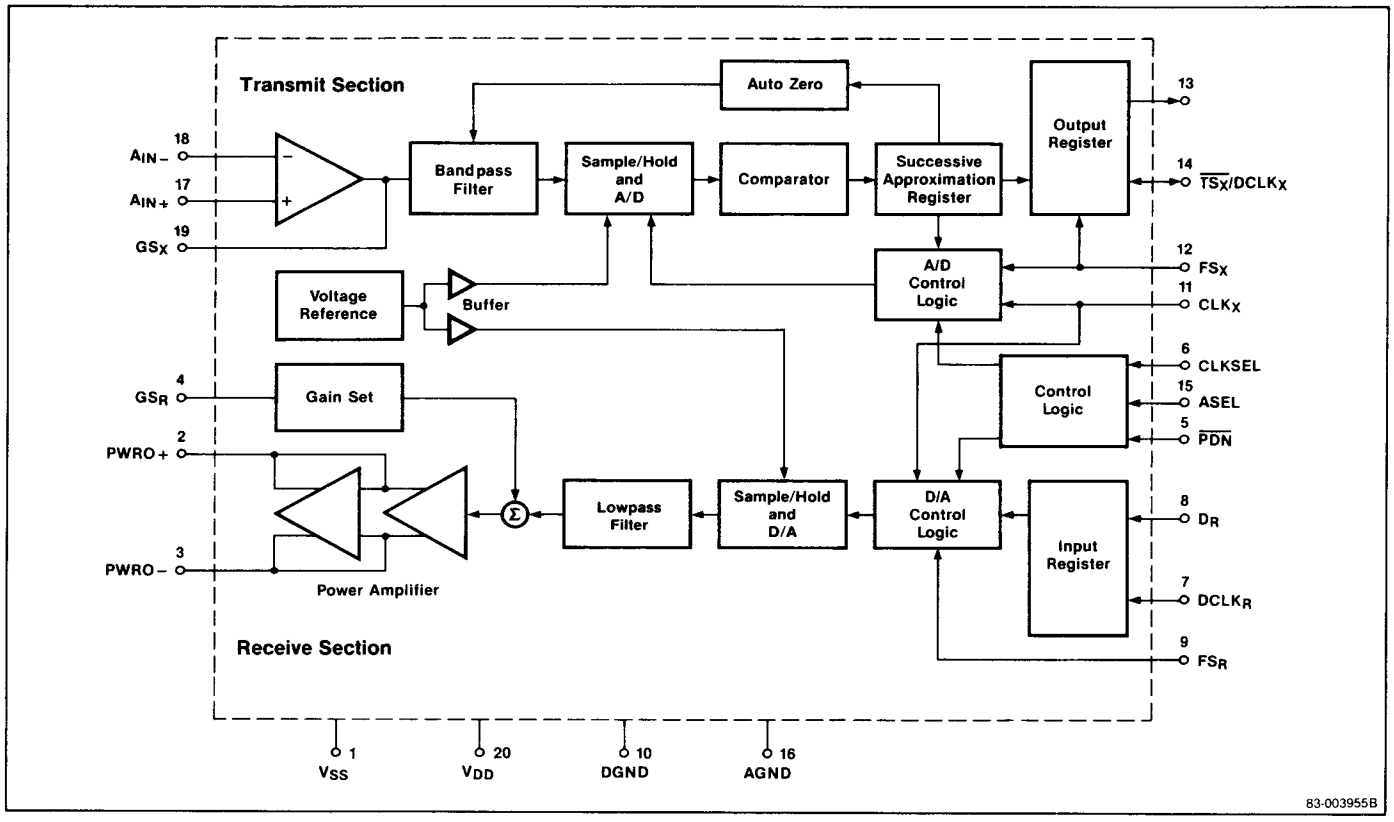
Transmit Signaling [SIG_X]

The logic state of SIG_X is transmitted as bit 8 of the channel word in signaling frames.

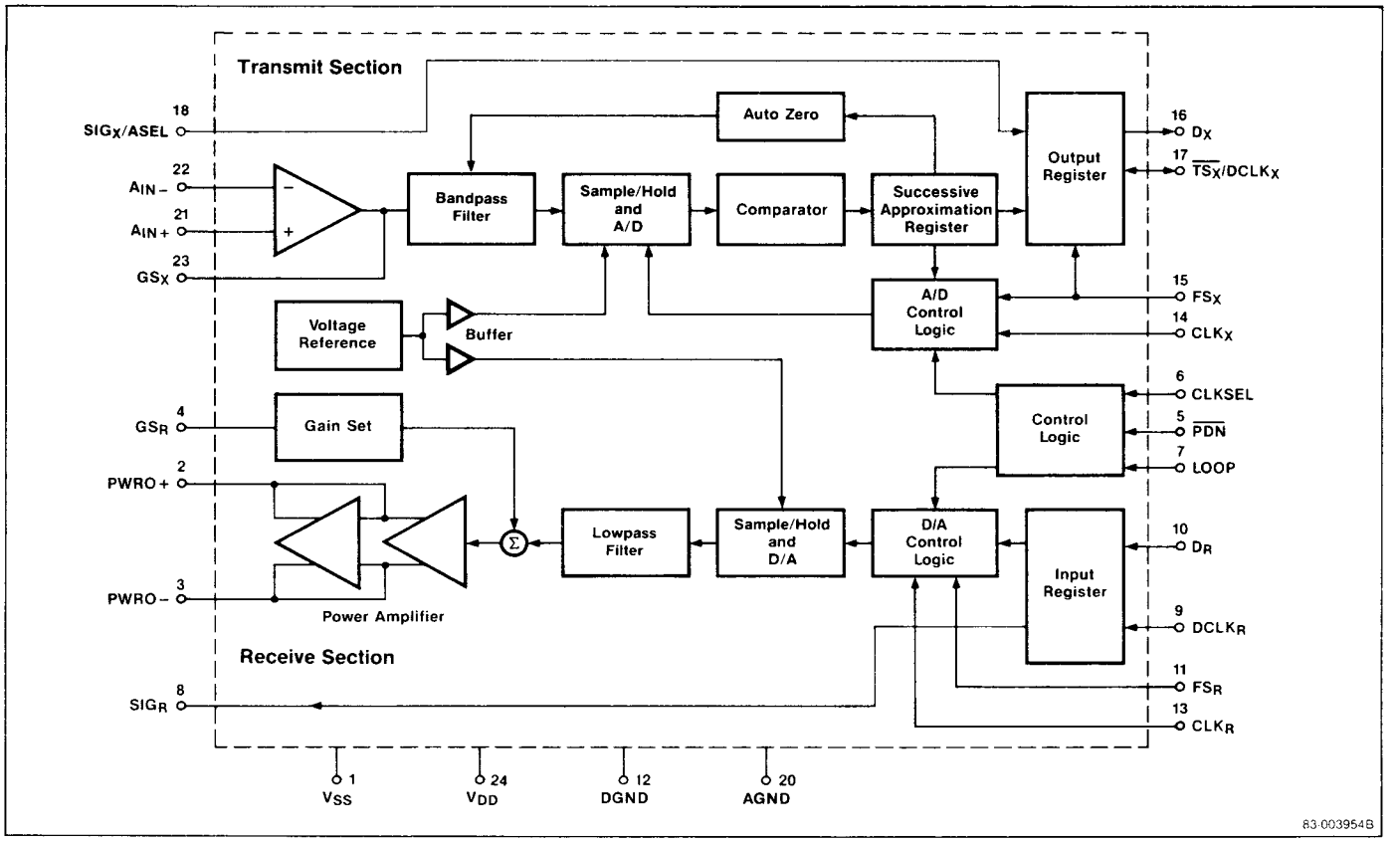
Transmit Analog Input [A_{IN+} and A_{IN-}]

The vf analog signal enters the unbalanced noninverting input A_{IN+} of the transmit operational amplifier. The gain is set by external resistors connected between the op amp's inverting input pin A_{IN-} and the transmit gain set pin GS_X.

Block Diagram, μPD9513AD



Block Diagram, μPD9514AD



Operational Description

Power-Up

The μPD9513AD and 9514AD reset on power-up to maintain the integrity of the PCM highway during the power-up sequence. For approximately four frames (500 μs) after power is applied, digital outputs D_X and $\overline{TS_X}$ are held in a high-impedance state and digital output SIG_R is held low. After this initial delay, the transmit digital outputs become functional and occur in the proper time slot. The SIG_R output remains low until it is updated during a signaling frame.

Because of the autozero circuit settling time, analog circuits, such as filters, sample-and-hold, and D/A converters, require about 60 ms to reach equilibrium. Thus, signaling information is available almost immediately, whereas valid voice information is delayed.

Power-Down and Standby Modes

Power-down and standby modes reduce power consumption from 80 mW to 8 mW.

Holding $\overline{PDN}$ low establishes the power-down mode, disabling most internal circuits. Only circuits that are required for power-up, such as the power-down controller, data clock, and frame sync buffers, stay enabled. Within 10 μs after $\overline{PDN}$ is held low, digital outputs D_X and $\overline{TS_X}$ go to high impedance and SIG_R goes low. Pulling PDN up to high restores the power-up mode.

The standby mode allows the user to selectively power down the transmit and receive sections by holding low the frame sync clock inputs FS_X and FS_R, respectively.

Fixed Data Rate Mode

Connecting the $DCLK_R$ pin to V_{SS} selects the fixed data rate mode. In this mode, transmit and receive clocks CLK_X and CLK_R serve as master clocks to operate the codec and filter circuits and also as PCM data clocks to clock bits to and from the PCM highway. By strapping at the CLKSEL pin, CLK_X and CLK_R are selected to be 2.048, 1.544, or 1.536 MHz. Only these three frequencies are possible in the fixed data rate mode.

Frame synchronization clock FS_X controls data transfer from D_X to the PCM highway. The clock sets the channel sampling frequency at 8 kHz. After FS_X is detected high on the falling edge of CLK_X, data is clocked out serially on the next eight rising edges of CLK_X. In the following falling edge, the three-state output at D_X returns to the floating state.

The timeslot strobe enable output $\overline{TS_X}$ is low during data transfer out of D_X. This signal can be used to gate the 8-bit word onto the PCM highway when an external buffer is driving the output line.

Receive data is clocked in from the PCM highway after FS_R is detected high on the falling edge of CLK_R. The next eight falling edges of CLK_R latch the receive data.

Variable Data Rate Mode

Connecting the $DCLK_R$ pin to the external PCM data clock (instead of to V_{SS}) selects the variable data rate mode. The clock frequency can vary from 64 kHz to 2.048 MHz. Master clock inputs CLK_R and CLK_X are still restricted to 2.048, 1.544, or 1.536 MHz as selected by strapping at the CLKSEL pin.

Operation in this mode is similar to the fixed data rate mode except the PCM data clocks are $DCLK_X$ and $DCLK_R$ instead of CLK_X and CLK_R. Because signaling is not supported, the frame sync pulses are single width.

Signaling

The signaling function is available only with the μPD9514AD in the fixed data rate mode. The width of the pulse on FS_X and FS_R distinguishes between a signaling and nonsignaling frame. A single-width pulse (one master clock period) designates a nonsignaling frame; a double-width pulse designates a signaling frame.

When data is transferred onto D_X in a transmit signaling frame, the least significant bit (LSB) of the encoded PCM data is replaced with the signaling state present on SIG_X. In a receive signaling frame, the seven most significant bits of the PCM data are routed to the decoder and the least significant bit is latched at the SIG_R output until updated in the next signaling frame. The D/A converter compensates for the lost LSB and minimizes deterioration in SD and GT characteristics.

Asynchronous Operation

The μPD9514AD transmit and receive sections can operate asynchronously. Therefore, in either fixed or variable data rate mode, master clocks CLK_R and CLK_X can be independent of each other.

Analog Loopback

The μPD9514AD offers an internal loopback test capability. Setting the LOOP input pin high connects the vf receive port to the vf transmit port internally: PWRO+ to A_{IN+}, GS_R to PWRO−, and A_{IN-} to GS_X. This feature allows the user to remotely test the line circuit by comparing the digital codes sent to digital receive port D_R with the resulting codes output at digital transmit port D_X. Because of the difference in transmission levels, a 0-dBm0 digital tone input at D_R returns to D_X as a +3-dBm0 digital tone output. Therefore, the maximum input level that can be tested with analog loopback is +3 dBm0.

VF Transmit

At the vf transmit input, an uncommitted operational amplifier is provided for gain adjustment in the passband. The op amp input leads are A_{IN-} and A_{IN+} and the output is GS_X. For normal operation as a noninverting amplifier, the device functions best with gain settings of 0 to 20 dB, load resistance (including the gain-setting resistance) greater than 10 kΩ, and load capacitance less than 50 pF. See figure 1.

The op amp output goes through a bandpass filter that fulfills the flatness and frequency response specified by CCITT G.712. The filter includes an antialiasing section that has 35 dB attenuation at the 8-kHz sampling frequency and a notch section that rejects 50- and 60-Hz power line frequencies.

The filtered signal continues to the encoder sample-and-hold circuit. With the on-chip autozero circuit, which corrects for dc offset, and the precision voltage reference, the encoder performs the A/D conversion with μ-law or A-law companding as selected by strapping at the ASEL pin. The encoded PCM data is stored in the output register waiting for FS_X to initiate data transfer to the PCM highway.

VF Receive

Digital data entering at D_R is decoded through the D/A converter according to the selected companding law. A lowpass filter corrects for the (sin x)/x response of the decoder. At the vf receive output port, a differential power amplifier can drive balanced loads as low as 600 ohms. Two external resistors set the amplifier gain between 0 and −12 dB. See figure 2.

Either of the power amp outputs can drive an unbalanced load as low as 300 ohms.

Figure 1. Transmit Amplifier Gain Setting

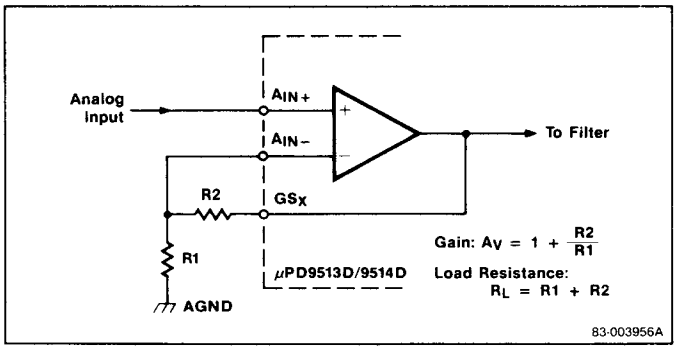
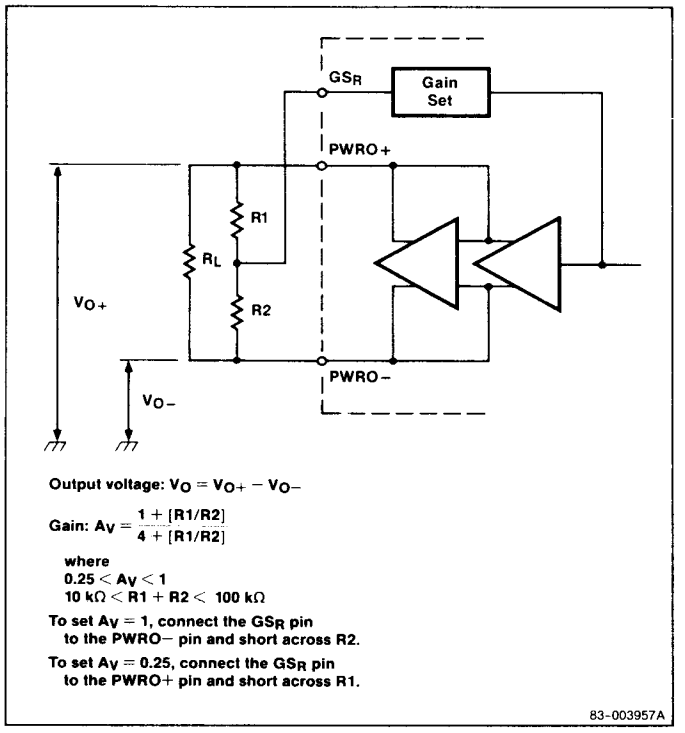


Figure 2. Receive Power Amplifier Gain Setting



Absolute Maximum Ratings

$T_A = +25°C$

Parameter	Symbol	Rating	Conditions
Supply voltage	V_{DD}	−0.3 to +7.0 V	
	V_{SS}	−7.0 to +0.3 V	
Analog input voltage	V_{AIN}	V_{SS} − 0.3 to V_{DD} + 0.3 V	Pins A_{IN+}, A_{IN-}, GS_X, GS_R
Digital input voltage	V_{DIN1}	−0.3 to V_{DD} + 0.3 V	For pins other than CLKSEL
	V_{DIN2}	V_{SS} − 0.3 to V_{DD} + 0.3 V	Pins CLKSEL, $DCLK_R$
Voltage applied to digital output pin	V_{DOUT}	−0.3 to V_{DD} + 0.3 V	For all digital output pins
Analog ground pin voltage	V_{AG}	±0.1 V	$V_{DG} = 0$
Analog output pin short-circuit time	t_s	Unlimited	Pins PWR0+, PWR−
Power dissipation	P_D	500 mW	
Operating temperature	T_{OPT}	0 to +70°C	
Storage temperature	T_{STG}	−65 to +150°C	
Soldering temperature	T_{SOLD}	+260°C	Less than 10 seconds

Note:

(1) Voltages are based on the condition that $V_{DG} = V_{AG} = 0$.

(2) Connection between AGND and DGND pins should be as short as possible.

Recommended Operating Conditions

T_A = 0 to +70°C; V_{DD} = +5 ±0.25 V; V_{SS} = −5 ±0.25 V; $V_{DG} = V_{AG}$ = 0

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Power						
Supply voltage	V_{DD}	+4.75	+5.0	+5.25	V	
	V_{SS}	−5.25	−5.0	−4.75	V	
Analog						
Transmit amplifier						
Input analog voltage	V_{AIN}	−2.17		+2.17	V	
Gain setting range	GR_{AX}	0		+20	dB	
Load resistance	RL_{AX}	10			kΩ	
Load capacitance	CL_{AX}			50	pF	
Receive amplifier						
Load resistance	RL_{AR}	300			Ω	Unbalanced output
		600			Ω	Balanced output
Load capacitance	CL_{AR}			100	pF	Pins PWRO+, PWRO−
Digital						
Input at digital pins other than CLKSEL						
Low voltage	V_{IL}	0		0.8	V	
High voltage	V_{IH}	2.0		V_{DD}	V	
Input at CLKSEL pin						
Low voltage	V_{ILO}	V_{SS}		V_{SS} − 0.5	V	f_{CLK} = 2.048 MHz
Intermediate voltage	V_{IIO}	V_{DG} − 0.5		V_{DG} + 0.5	V	f_{CLK} = 1.544 MHz
High voltage	V_{IHO}	V_{DD} − 0.5		V_{DD}	V	f_{CLK} = 1.536 MHz
Clock						
Master clock frequency	f_{CLK} ($1/t_{CY}$)		1.536		MHz	CLKSEL connected to V_{DD}
			1.544		MHz	CLKSEL connected to DGND
			2.048		MHz	CLKSEL connected to V_{SS}
Master clock duty cycle	t_{CDC}	45	50	55	%	
Data clock frequency	f_{DCLK}	64 kHz		2.048	MHz	
Master clock pulse width	t_{CLK}	220			ns	
Frame sync clock freq	f_{FS}	7.9996	8.0000	8.0004	kHz	
D_R setup time	t_{DSR}	10			ns	
D_R hold time	t_{DHR}	60			ns	
Clock rise time	t_R			30	ns	
Clock fall time	t_F			30	ns	
Timing in Fixed Data Rate Mode						
Frame sync delay	t_{FSD}	100		t_{CY} − 100	ns	
SIG_X setup time	t_{SS}	0			ns	μPD9514AD
SIG_X hold time	t_{SH}	0			ns	μPD9514AD

Recommended Operating Conditions (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Timing in Variable Data Rate Mode						
Timeslot delay	t_{TSD}	140		$t_{DCY} - 140$	ns	Referenced to $DCLK_X$, $DCLK_R$
Frame sync delay	t_{FSD}	100		$t_{CY} - 100$	ns	
Data clock pulse width	t_{DCLK}	220			ns	
Timing in Variable Data Rate Mode, 64-kb Operation						
Transmit frame sync minimum downtime	t_{FSLX}	488			ns	FS_X is TTL high for remainder of frame
Receive frame sync minimum downtime	t_{FSLR}	1952			ns	FS_R is TTL high for remainder of frame
Data clock pulse width	t_{DCLK}	0.195		10	μs	

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{DD} = +5 \pm 0.25$ V; $V_{SS} = -5 \pm 0.25$ V; $V_{DG} = V_{AG} = 0$
$DCLK_R = DCLK_X = 2.048$ MHz
All outputs are unloaded unless otherwise specified.
For typical values, $T_A = +25°C$, $V_{DD} = +5$ V, and $V_{SS} = -5$ V.

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Power						
Normal operating current	I_{DD}		8	13.0	mA	
	I_{SS}		−8	−13.0	mA	
Power-down current	I_{DDPD}		0.8	1.3	mA	10 μs after $\overline{PDN}$ is set to low.
	I_{SSPD}		−0.8	−1.0	mA	
Standby current	I_{DDST}		0.8	1.3	mA	300 ms after FS_X and FS_R are set to low.
	I_{SSST}		−0.8	−1.0	mA	
Power dissipation						
Normal	P_D		80	136.5	mW	
Power-down	P_{DPD}		8	12.1	mW	10 μs after $\overline{PDN}$ is set to low.
Standby	P_{DST}		8	12.1	mW	300 ms after FS_X and FS_R are set to low.
Digital Interface						
Digital input current	I_{ID1}			10	μA	$V_{DIN} = 0$ to V_{DD}
	I_{ID2}			10	μA	Pins CLKSEL, $DCLK_R$; $V_{DIN} = V_{SS}$ to V_{DD}
Output low voltage	V_{OL}			0.4	V	Pins D_X, $\overline{TS_X}$, SIG_R; $I_{OL} \leq 3.2$ mA
Output high voltage	V_{OH}	2.4			V	Pin D_X, $I_{OH} \leq 9.6$ mA; Pin SIG_R, $I_{OH} \leq 1.2$ mA
Digital output capacitance	C_{OD}		5		pF	
Digital input capacitance	C_{ID}			10	pF	

DC Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Transmit Amplifier						
Input leakage current	I_B			100	nA	V_{AIN} = −2.17 to 2.17 V; Pins A_{IN+}, A_{IN-}
Input resistance	R_{IN}	10			MΩ	
Input offset voltage	V_{IO}	−25		25	mV	
Common mode rejection	CMRR	55			dB	V_{AIN} = −2.17 to +2.17 V
Voltage gain	A_V	5000				
Maximum output voltage swing	V_{CM}	−2.17		2.17	V	$R_L \geq 10$ kΩ
Receive Power Amplifier						
Output offset voltage	V_{OS}	−150	75	150	mV	Unbalanced output connection, pins PWRO+ and PWRO−
Maximum output voltage swing						
Unbalanced output	V_{CM1}	−3.06		3.06	V	$R_L \geq 300$ Ω
Balanced output	V_{CM2}	−6.12		6.12	V	$R_L \geq 600$ Ω

Transmission Characteristics

T_A = +25°C; V_{DD} = +5 ±0.25 V; V_{SS} = −5 ±0.25 V
Analog input signal level V_{IN} = 0 dBm0 (f = 1020 Hz); analog input op amp gain = 1 (noninverting)
Digital input signal level = 0 dBm0 (f = 1020 Hz); receive output power amplifier gain = 1; unbalanced output (PWRO+) unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Gain						
Encoder milliwatt response (transmit gain tolerance)	EmW	−0.15		+0.15	dBm0	μ-law: V_{IN} = 1.064 V rms A-law: V_{IN} = 1.068 V rms V_{DD} = +5 V; V_{SS} = −5 V
EmW variation with temperature and power supply	EmW_{TS}	−0.12		+0.12	dB	T_A = 0 to +70°C
Digital milliwatt response (receive gain tolerance)	DmW	−0.15		+0.15	dBm0	Measured relative to $0TLP_R$; signal input per CCITT recommendation G.712; output signal of 1000 Hz; V_{DD} = +5 V; V_{SS} = −5 V
DmW variation with temperature and power supply	DmW_{TS}	−0.08		+0.08	dB	T_A = 0 to +70°C

Transmission Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Gain (cont)						
Zero transmission level point, transmit section						
μ-law	$OTLP1_X$		+2.76		dBm	Referenced to 600 Ω
			+1.00		dBm	Referenced to 900 Ω
A-law	$OTLP2_X$		+2.79		dBm	Referenced to 600 Ω
			+1.03		dBm	Referenced to 900 Ω
Zero transmission level point, receive section						
μ-law	$OTLP1_R$		+5.76		dBm	Referenced to 600 Ω
			+4.00		dBm	Referenced to 900 Ω
A-law	$OTLP2_R$		+5.79		dBm	Referenced to 600 Ω
			+4.03		dBm	Referenced to 900 Ω
Gain Tracking Variation of gain with input level; reference level = −10 dBm0 unless otherwise specified.						
Transmit gain tracking error						
μ-law	$GT1_X$	−0.25		+0.25	dB	+3 to −40 dBm0
		−0.5		+0.5	dB	−40 to −50 dBm0
		−1.2		+1.2	dB	−50 to −55 dBm0
A-law	$GT2_X$	−0.25		+0.25	dB	+3 to −40 dBm0
		−0.5		+0.5	dB	−40 to −50 dBm0
		−1.2		+1.2	dB	−50 to −55 dBm0
A-law, white noise input CCITT G.712	$GT3_X$		−0.1		dB	−10 to −55 dBm0
			−0.3		dB	−55 to −60 dBm0
Receive gain tracking error						
μ-law	$GT1_R$	−0.25		+0.25	dB	+3 to −40 dBm0
		−0.5		+0.5	dB	−40 to −50 dBm0
		−1.2		+1.2	dB	−50 to −55 dBm0
A-law	$GT2_R$	−0.25		+0.25	dB	+3 to −40 dBm0
		−0.5		+0.5	dB	−40 to −50 dBm0
		−1.2		+1.2	dB	−50 to −55 dBm0
A-law, white noise input CCITT G.712	$GT3_R$		+0.1		dB	−10 to −55 dBm0
			+0.3		dB	−55 to −60 dBm0

Transmission Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Frequency Response						
Analog input operational amplifier gain = 1 (noninverting); receive output power amplifier gain = 1 (unbalanced, PWRO+)						
Transmit branch; gain relative to gain at 1020 Hz, 0 dBm0	$G_{RX}1$			−30	dB	16.67 Hz
	$G_{RX}2$			−25	dB	50 Hz
	$G_{RX}3$			−23	dB	60 Hz
	$G_{RX}4$	−1.8		−0.125	dB	200 Hz
	$G_{RX}5$	−0.125		+0.125	dB	0.3 to 3.0 kHz
	$G_{RX}6$	−0.35		+0.03	dB	3.3 kHz
	$G_{RX}7$	−0.7		−0.1	dB	3.4 kHz
	$G_{RX}8$			−14	dB	4.0 kHz
	$G_{RX}9$			−32	dB	4.6 kHz and above
Receive branch; gain relative to gain at 1020 Hz, 0 dBm0	$G_{RR}1$			+0.125	dB	Below 200 Hz
	$G_{RR}2$	−0.5		+0.125	dB	200 Hz
	$G_{RR}3$	−0.125		+0.125	dB	0.3 to 3.0 kHz
	$G_{RR}4$	−0.35		+0.03	dB	3.3 kHz
	$G_{RR}5$	−0.7		−0.1	dB	3.4 kHz
	$G_{RR}6$			−14	dB	4.0 kHz
	$G_{RR}7$			−30	dB	4.6 kHz and above
Noise						
Transmit noise	$N_{XC}1$			15	dBrnc0	A_{IN+} is grounded to AGND; input amplifier gain = 1; C-message weighting
	$N_{XC}2$			18	dBrnc0	Same as $N_{XC}1$; signaling data added to frame 6
	N_{XP}			−75	dBm0p	Same as $N_{XC}1$ except psophometric weighting
Receive noise	$N_{RC}1$			11	dBrnc0	D_R = 11111111; measure at PWRO+ with C-message weighting
	$N_{RC}2$			12	dBrnc0	Same as $N_{RC}1$ except D_R is zero code with sign bit toggled at 1-kHz rate
	N_{RP}			−79	dBm0p	Same as $N_{RC}1$ except D_R is the lowest positive decode level; psophometric weighting
Single-frequency noise	NSF			−50	dBm0	End-to-end measurement; CCITT G.712 4.2
Crosstalk, transmit to receive	CT_{TR}			−71	dB	Transmit input at A_{IN+} = 0-dBm0, 1020-Hz analog signal; D_R = lowest positive decode level
Crosstalk, receive to transmit	CT_{RT}			−71	dB	A_{IN+} is grounded to AGND; D_R = 0-dBm0, 1020-Hz digital signal
Transmit section power supply rejection ratio	$PSRR_T1$		40		dB	+100-mV signal on V_{DD}
	$PSRR_T2$		40		dB	+100-mV signal on V_{SS}
Receive section power supply rejection ratio	$PSRR_R3$		30		dB	+100 mV signal on V_{DD}
	$PSRR_R4$		30		dB	+100 mV signal on V_{SS}

Transmission Characteristics (cont)

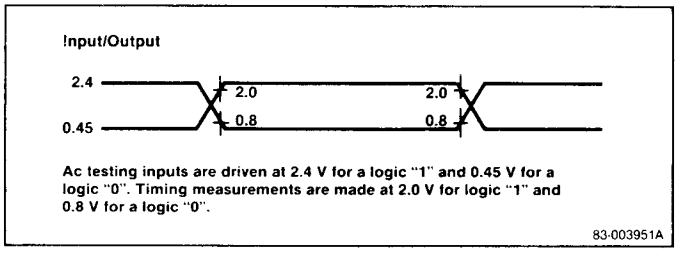
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Distortion						
Transmit signal-to-distortion ratio						
μ-law, CCITT G.712 Method 2	$SD1_X$	36			dB	0 to −30 dBm0
		30			dB	−30 to −40 dBm0
		25			dB	−40 to −45 dBm0
A-law, CCITT G.712 Method 2	$SD2_X$	36			dB	0 to −30 dBm0
		30			dB	−30 to −40 dBm0
		25			dB	−40 to −45 dBm0
A-law, CCITT G.712 Method 1	$SD3_X$		38		dB	−6 to −27 dBm0
			36		dB	−34 dBm0
			31		dB	−40 dBm0
			16		dB	−55 dBm0
Receive signal-to-distortion ratio						
μ-law, CCITT G.712 Method 2	$SD1_R$	36			dB	0 to −30 dBm0
		30			dB	−30 to −40 dBm0
		25			dB	−40 to −45 dBm0
A-law, CCITT G.712 Method 2	$SD2_R$	36			dB	0 to −30 dBm0
		30			dB	−30 to −40 dBm0
		25			dB	−40 to −45 dBm0
A-law, CCITT G.712 Method 1	$SD3_R$		38		dB	−6 to −27 dBm0
			36		dB	−34 dBm0
			31		dB	−40 dBm0
			16		dB	−55 dBm0
Transmit single-frequency distortion products	DP_X			−46	dBm0	AT&T Advisory No. 64 (3.8) 0-dBm0 input signal
Receive single-frequency distortion products	DP_R			−46	dBm0	AT&T Advisory No. 64 (3.8) 0-dBm0 input signal
Intermodulation distortion, end-to-end						
CCITT G.712 (7.1)	IMD_1			−35	dB	
CCITT G.712 (7.2)	IMD_2			−49	dBm0	
Spurious out-of-band signals, end-to-end	SOS			−25	dBm0	CCITT G.712 (6.1)
Spurious in-band signals, end-to-end	SIS			−40	dBm0	CCITT G.712 (9)
Transmit absolute delay	D_{AX}		245		μs	Fixed data rate, f_{CLKX} = 2.048 MHz

Transmission Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Distortion (cont)						
Transmit differential envelope delay relative to D_{AX}	D_{DX}					
500 to 600 Hz			170		μs	
600 to 1000 Hz			95		μs	
1000 to 2500 Hz			45		μs	
2600 to 2800 Hz			105		μs	
Receive absolute delay	D_{AR}		190		μs	Fixed data rate. f_{CLKR} = 2.048 MHz
Receive differential envelope delay relative to D_{AR}	D_{DR}					
500 to 600 Hz			45		μs	
600 to 1000 Hz			35		μs	
1000 to 2500 Hz			85		μs	
2600 to 2800 Hz			110		μs	
Timing Parameters in Fixed Data Rate Mode						
Data enable delay	t_{DZX}	0		145	ns	$C_L < 100$ pF
Data delay	t_{DDX}	0		145	ns	$C_L < 100$ pF
Data hold time	t_{HZX}	60		220	ns	$C_L = 0$
$\overline{TS_X}$ enable delay	t_{SON}	0		145	ns	$C_L < 100$ pF
$\overline{TS_X}$ disable delay	t_{SOFF}	50		210	ns	$C_L = 0$
SIG_R update time	t_{SIGR}	0		2	μs	
Timing Parameters in Variable Data Rate Mode						
D_X active delay	t_{DON}	0		65	ns	$C_L < 100$ pF
D_X inactive delay	t_{DOFF}	0		90	ns	$C_L < 100$ pF
Data delay	t_{DFSX}	0		140	ns	
Data delay	t_{DDX}	0		100	ns	$C_L < 100$ pF

Timing Waveforms

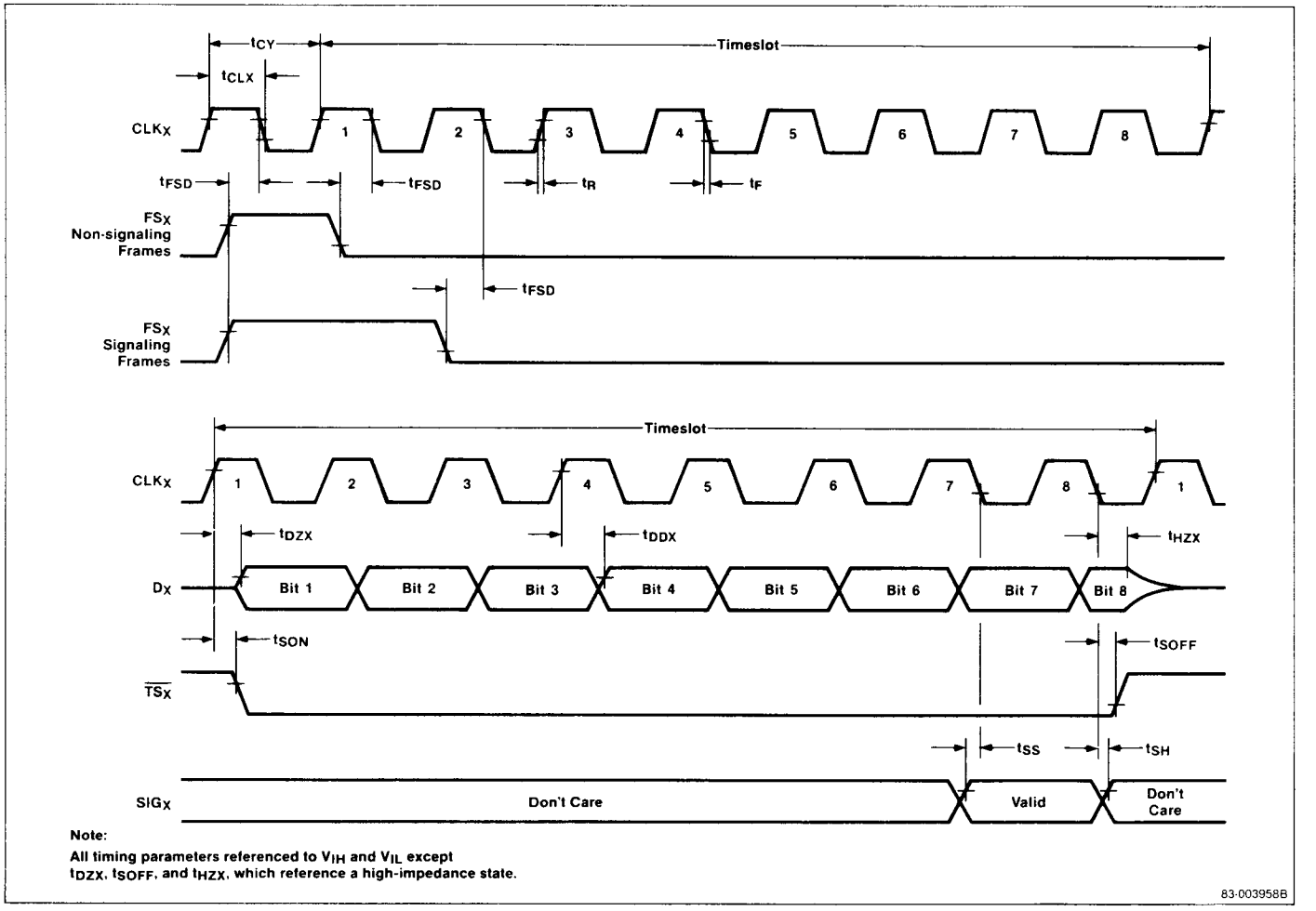
Timing Measurement Points



Ac testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for logic "1" and 0.8 V for a logic "0".

83-003951A

Transmit Timing, Fixed Data Rate Mode



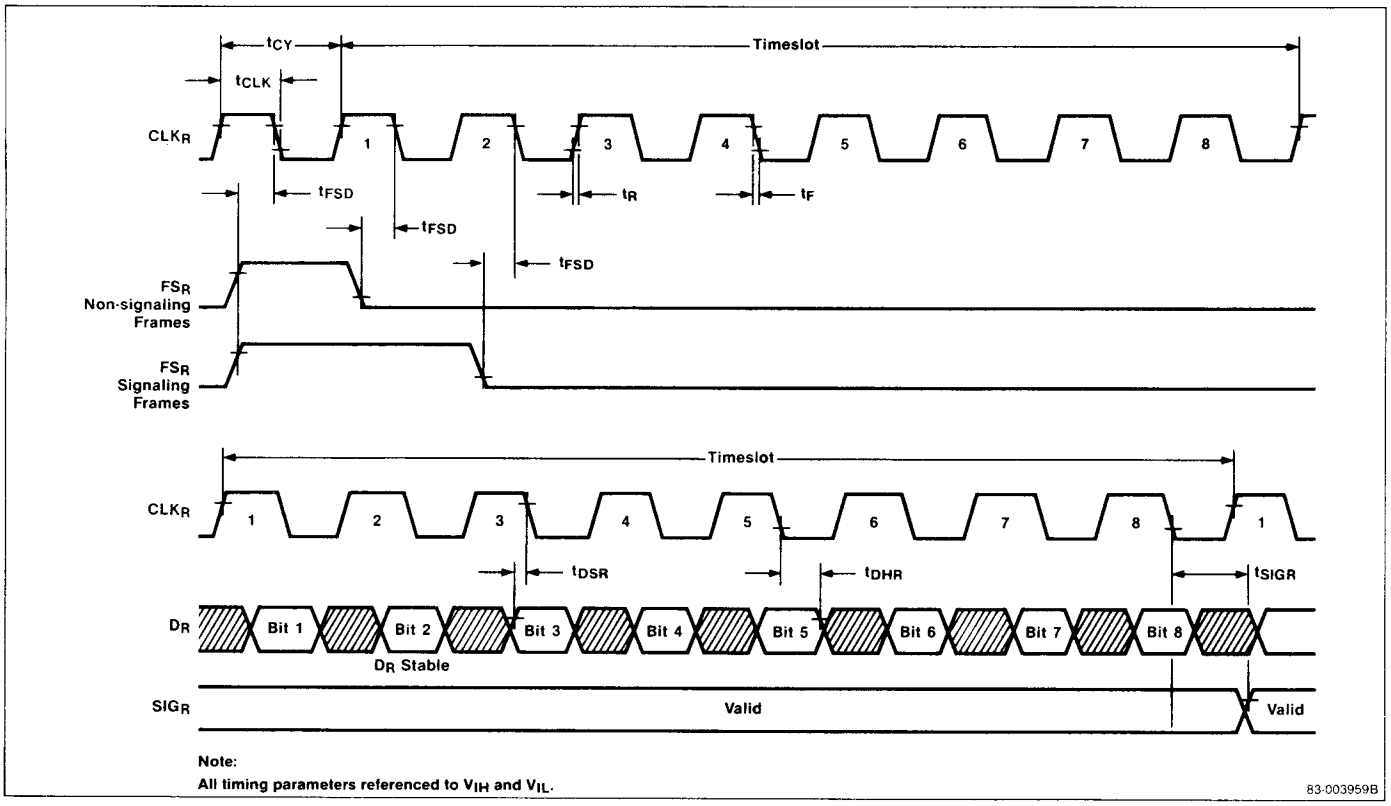
Note:

All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF}, and t_{HZX}, which reference a high-impedance state.

83-003958B

Timing Waveforms (cont)

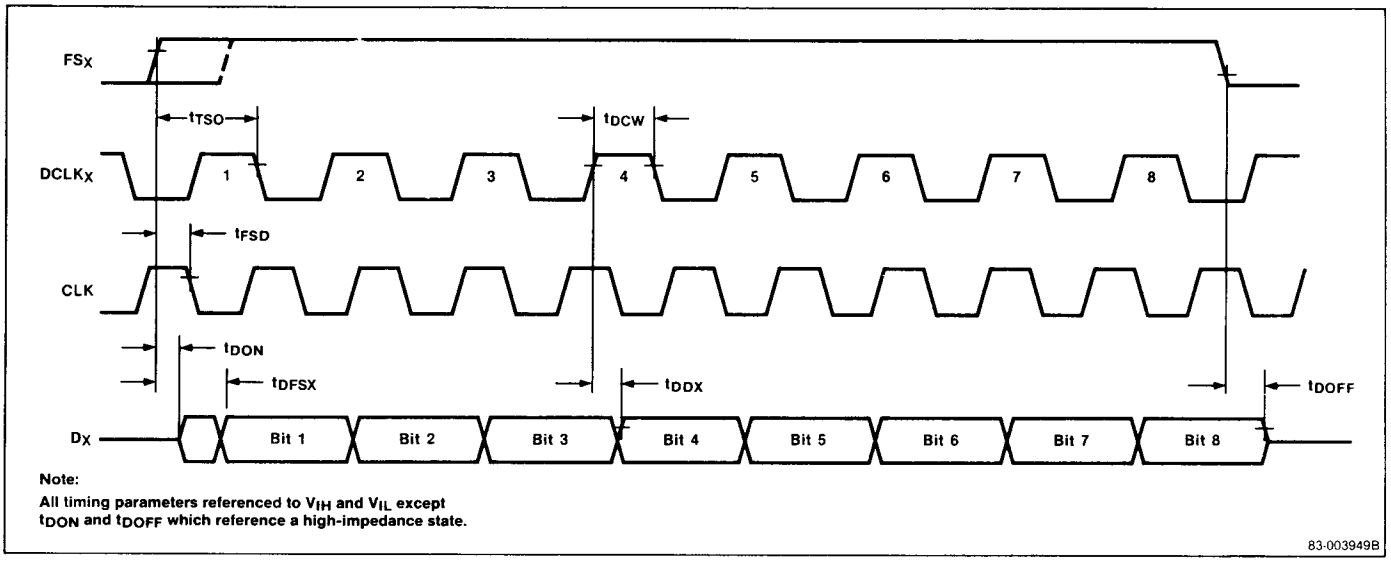
Receive Timing, Fixed Data Rate Mode



Note:
All timing parameters referenced to V_{IH} and V_{IL}.

83-003959B

Transmit Timing, Variable Data Rate Mode

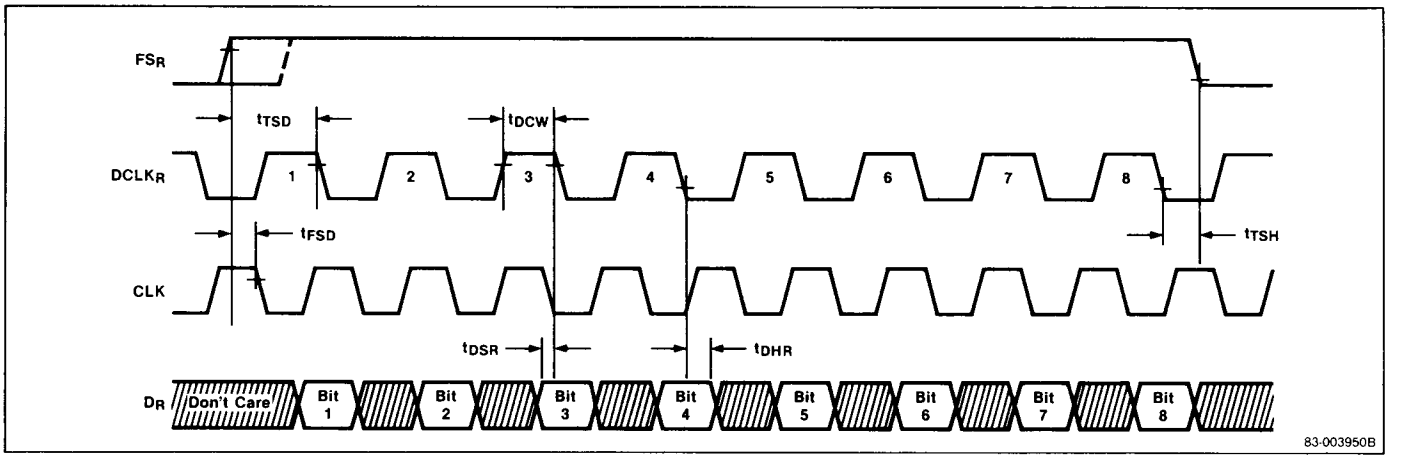


Note:
All timing parameters referenced to V_{IH} and V_{IL} except
t_{DON} and t_{DOFF} which reference a high-impedance state.

83-003949B

Timing Waveforms (cont)

Receive Timing, Variable Data Rate Mode



Packaging Information (cont)

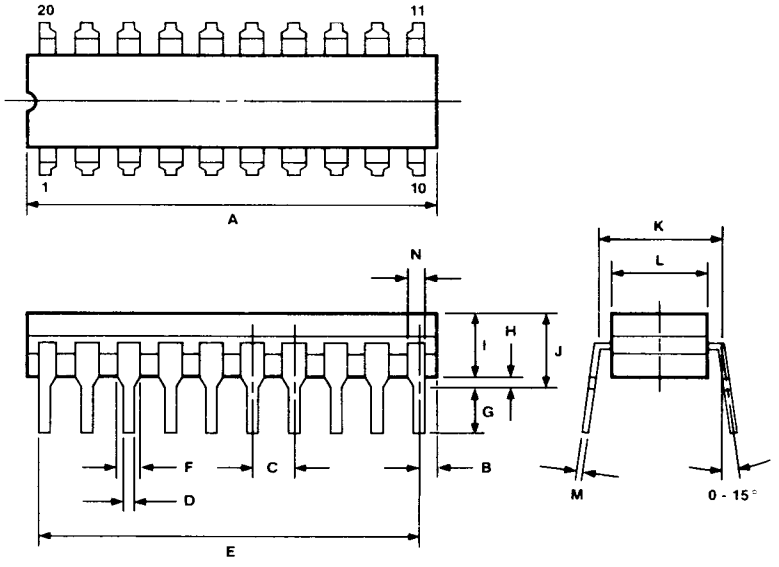
20-Pin Ceramic DIP (300-mil), μPD9513AD

Item	Millimeters	Inches
A	25.40 max	1.000 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	$.50^{+.09}_{-.15}$	$.020^{+.004}_{-.006}$
E	22.86	.900
F	.95 min	.037 min
G	2.54 min	.100 min
H	.51 min	.020 min
I	4.57 max	.180 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.60 max	.300 max
M	$.25^{+.11}_{-.05}$	$.010^{+.004}_{-.002}$
N	.85 min	.033 min

Note:

[1] Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-004C42B

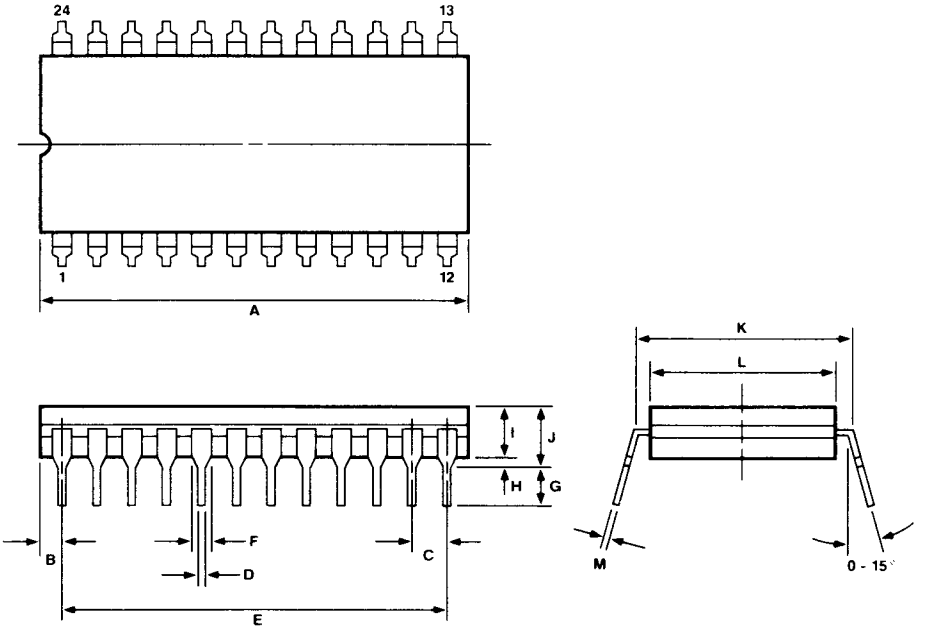
24-Pin Ceramic DIP (600-mil), μPD9514AD

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	$.50^{+.09}_{-.15}$	$.020^{+.004}_{-.006}$
E	27.94	1.100
F	.90 min	.036 min
G	2.54 min	.100 min
H	.51 min	.020 min
I	4.57 max	.180 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.20 max	.56 max
M	$.25^{+.11}_{-.05}$	$.010^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-004044B

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