128K × 8 CMOS FLASH MEMORY

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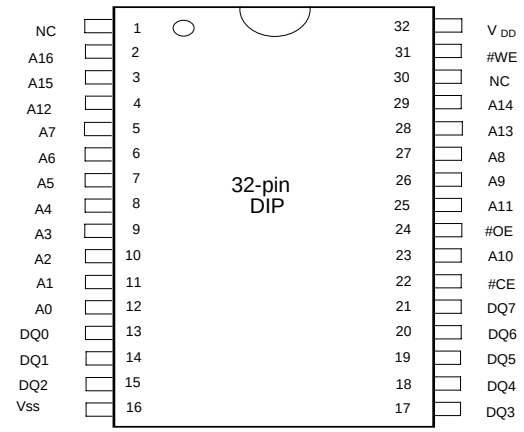
1. GENERAL DESCRIPTION

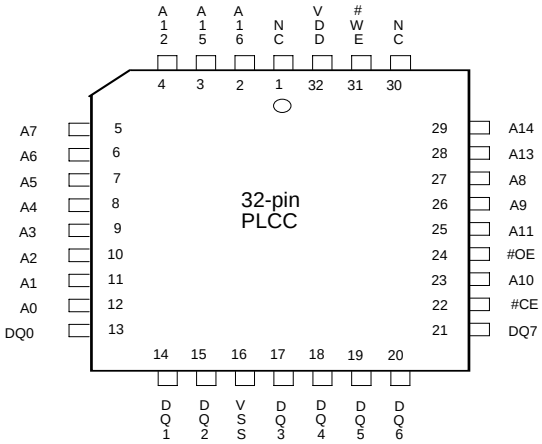
The W39F010 is a 1Mbit, 5-volt only CMOS flash memory organized as 128K × 8 bits. For flexible erase capability, the 1Mbits of data are divided into 32 small even pages with 4 Kbytes. The byte-wide (× 8) data appears on DQ7 – DQ0. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W39F010 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

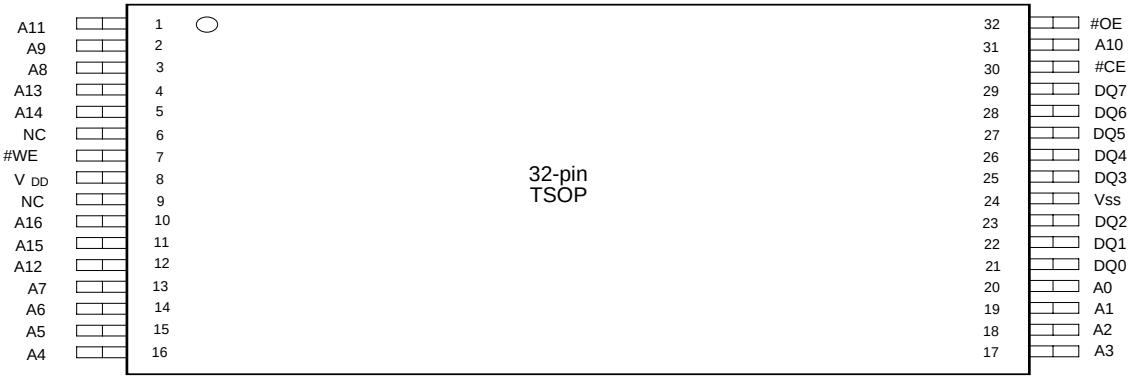
2. FEATURES

- Single 5-volt operations
  - 5-volt Read
  - 5-volt Erase
  - 5-volt Program
- Fast Program operation:
  - Byte-by-Byte programming: 50 μS (max.)
- Fast Erase operation:
  - Chip Erase cycle time: 100 mS (max.)
  - Page Erase cycle time: 25 mS (max.)
- Read access time: 70/90 nS
- 32 even pages with 4K bytes
- Any individual page can be erased
- Hardware protection:
  - Optional 16K byte Top/Bottom Boot Block with lockout protection
- Flexible 4K-page size can be used as Parameter Blocks
- Typical program/erase cycles:
  - 1K/10K
- Twenty-year data retention
- Low power consumption
  - Active current: 15 mA (typ.)
  - Standby current: 15 μA (typ.)
- End of program detection
  - Software method: Toggle bit/Data polling
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin 600 mil DIP, 32-pin PLCC, 32- pin STSOP (8 x 14 mm) and 32- pin TSOP

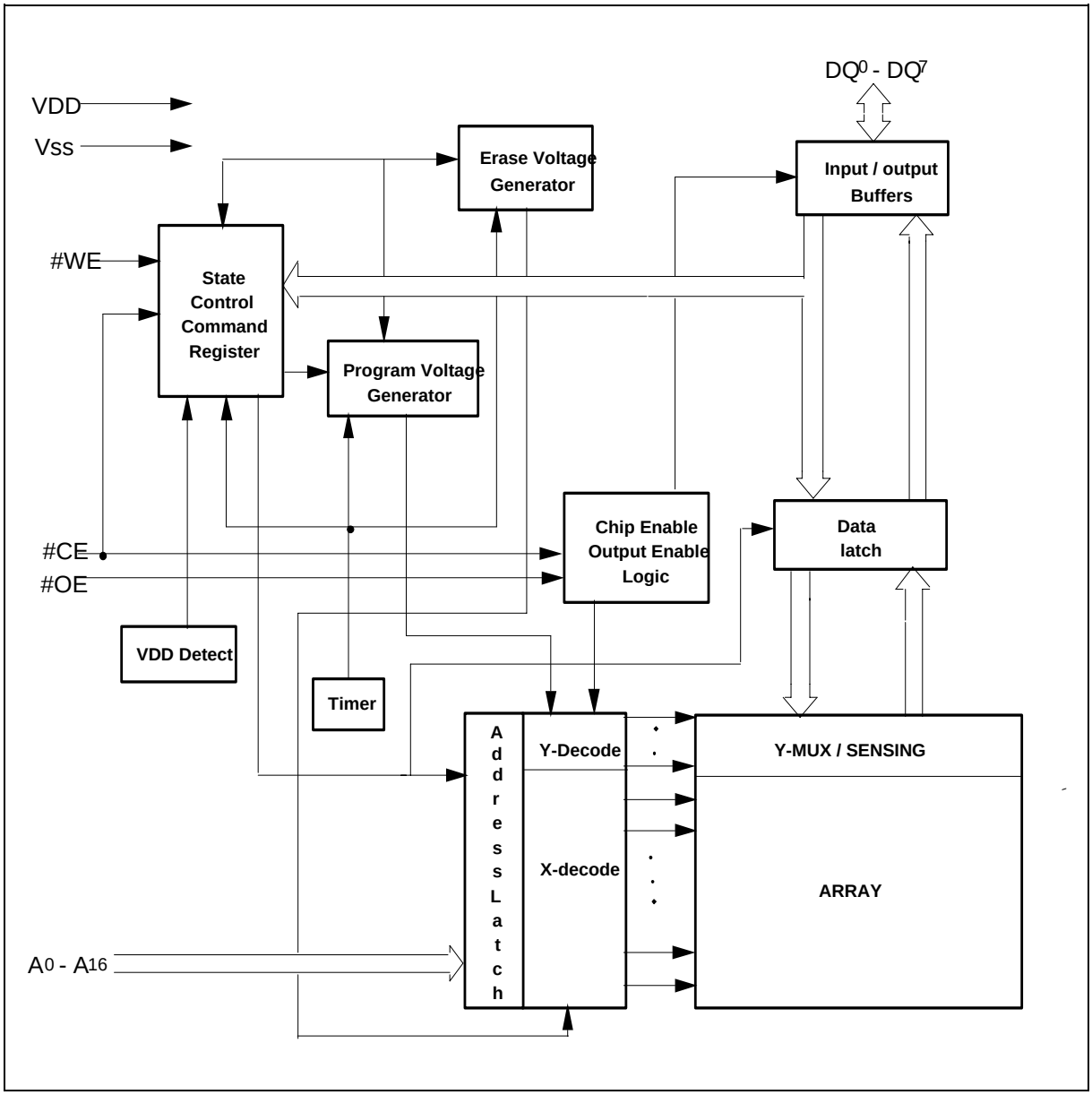
3. PIN CONFIGURATIONS







4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYMBOL	PIN NAME
A0 – A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connections

6. FUNCTIONAL DESCRIPTION

6.1 Device Bus Operation

6.1.1 Read Mode

The read operation of the W39F010 is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

6.1.2 Write Mode

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to bring #WE to logic low state, while #CE is at logic low state and #OE is at logic high state. Addresses are latched on the falling edge of #WE or #CE, whichever happens later; while data is latched on the rising edge of #WE or #CE, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

6.1.3 Standby Mode

There are two ways to implement the standby mode on the W39F010 device, both using the #CE pin.

A CMOS standby mode is achieved with the #CE input held at V_{DD} ±0.5V. Under this condition the current is typically reduced to less than 50 μA. A TTL standby mode is achieved with the #CE pin held at V_{IH}.

Under this condition the current is typically reduced to 2 mA.

In the standby mode the outputs are in the high impedance state, independent of the #OE input.

6.1.4 Output Disable Mode

With the #OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

6.2 Data Protection

The W39F010 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from V_{DD} power-up and power-down transitions or system noise.

6.3 Boot Block Operation

There are two alternatives to set the boot block. The 16K-byte in the top/bottom location of this device can be locked as boot block, which can be used to store boot codes. It is located in the last 16K bytes or first 16K bytes of the memory with the address range from 1C000(hex) to 1FFFF(hex) for top location or 00000(hex) to 03FFF(hex) for bottom location.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout), other memory locations can be changed by the regular programming method.

In order to detect whether the boot block feature is set on the first/last 16K-byte block or not, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address 0002(hex) for first(bottom) location or 1FFF2(hex) for last(top) location. If the DQ0/DQ1 of output data is "1," the 16Kbytes boot block programming lockout feature will be activated; if the DQ0/DQ1 of output data is "0," the lockout feature will be inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-byte command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

6.3.1 Low V_{DD} Inhibit

To avoid initiation of a write cycle during V_{DD} power-up and power-down, the W39F010 locks out when V_{DD} < 2.0V (see DC Characteristics section for voltages). The write and read operations are inhibited when V_{DD} is less than 2.0V typical. The W39F010 ignores all write and read operations until V_{DD} > 2,0V. The user must ensure that the control pins are in the correct logic state when V_{DD} > 2.0V to prevent unintentional writes.

6.3.2 Write Pulse "Glitch" Protection

Noise pulses of less than 10 nS (typical) on #OE, #CE, or #WE will not initiate a write cycle.

6.3.3 Logical Inhibit

Writing is inhibited by holding any one of #OE = V_{IL}, #CE = V_{IH}, or #WE = V_{IH}. To initiate a write cycle #CE and #WE must be a logical zero while #OE is a logical one.

6.3.4 Power-up Write Inhibit

Power-up of the device with #WE = #CE = V_{IL} and #OE = V_{IH} will not accept commands on the rising edge of #WE except 5mS delay (see the power up timing in AC Characteristics). The internal state machine is automatically reset to the read mode on power-up.

6.4 Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. "Command Definitions" defines the valid register command sequences.

6.4.1 Read Command

The device will automatically power-up in the read state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition.

The device will automatically returns to read state after completing an Embedded Program or Embedded Erase algorithm.

Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

6.4.2 Auto-select Command

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system.

The device contains an auto-select command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the auto-select command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of DAH. A read cycle from address XX01H returns the device code (W39F010 = A1).

To terminate the operation, it is necessary to write the auto-select exit command sequence into the register.

6.4.3 Byte Program Command

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two "unlock" write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded program algorithm. Addresses are latched on the falling edge of #CE or #WE, whichever happens later and the data is latched on the rising edge of #CE or #WE, whichever happens first. The rising edge of #CE or #WE (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see "Hardware Sequence Flags"). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for Data Polling operations. Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Programming is allowed in any sequence and across page boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to program 0 back to 1, the toggle bit will stop toggling. Only erase operations can convert "0"s to "1"s.

Refer to the Programming Command Flow Chart using typical command strings and bus operations.

6.4.4 Chip Erase Command

Chip erase is a six-bus-cycle operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles are asserted, followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically erase and verify the entire memory for an all one data pattern. The erase is performed sequentially on each pages at the same time (see "Feature"). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last #WE pulse in the command sequence and terminates when the data on DQ7 is "1" at which time the device returns to read the mode.

Refer to the Erase Command Flow Chart using typical command strings and bus operations.

6.4.5 Page Erase Command

Page erase is a six-bus cycles operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles then follows by the page erase command. The page address (any address location within the desired page) is latched on the falling edge of #WE, while the command (50H) is latched on the rising edge of #WE.

Page erase does not require the user to program the device prior to erase. When erasing a page, the remaining unselected pages are not affected. The system is not required to provide any controls or timings during these operations.

The automatic page erase begins after the erase command is completed, right from the rising edge of the #WE pulse for the last page erase command pulse and terminates when the data on DQ7, Data Polling, is "1" at which time the device returns to the read mode. Data Polling must be performed at an address within any of the pages being erased.

Refer to the Erase Command flow Chart using typical command strings and bus operations.

6.5 Write Operation Status

6.5.1 DQ7: Data Polling

The W39F010 device features Data Polling as a method to indicate to the host that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7.

During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce a "1" at the DQ7 output.

For chip erase, the Data Polling is valid after the rising edge of the sixth pulse in the six #WE write pulse sequences. For page erase, the Data Polling is valid after the last rising edge of the page erase #WE pulse. Data Polling must be performed at addresses within any of the pages being erased. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable (#OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte′s valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0 – DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or page erase time-out (see "Command Definitions").

6.5.2 DQ6: Toggle Bit

The W39F010 also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (#OE toggling) data from the device at any address will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth #WE pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth #WE pulse in the six write pulse sequence. For page erase, the Toggle Bit is valid after the last rising edge of the page erase #WE pulse. The Toggle Bit is active during the page erase time-out.

Either #CE or #OE toggling will cause DQ6 to toggle.

7. TABLE OF OPERATING MODES

7.1 Device Bus Operations

MODE	PIN			
	#CE	#OE	#WE	DQ0 – DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	Din
Standby	V_{IH}	X	X	High Z
Write Inhibit	X	V_{IL}	X	High Z/Dout
	X	X	V_{IH}	High Z/Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	High Z

7.2 Command Definitions

COMMAND Description	NO. OF Cycles	1ST CYCLE Addr. (1)Data	2ND CYCLE Addr. Data	3RD CYCLE Addr. Data	4TH CYCLE Addr. Data	5TH CYCLE Addr. Data	6TH CYCLE Addr. Data	7TH CYCLE Addr. Data
Read	1	A_{IN} D_{OUT}						
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10	
Page Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	PA(3) 50	
Byte Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}			
Top Boot Block Lockout –16KByte	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 70	1FFFF XX(4)
Bottom Boot Block Lockout - 16KByte	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 70	00000 XX(4)
Product ID Entry	3	5555 AA	2AAA 55	5555 90				
Product ID Exit (2)	3	5555 AA	2AAA 55	5555 F0				
Product ID Exit (2)	1	XXXX F0						

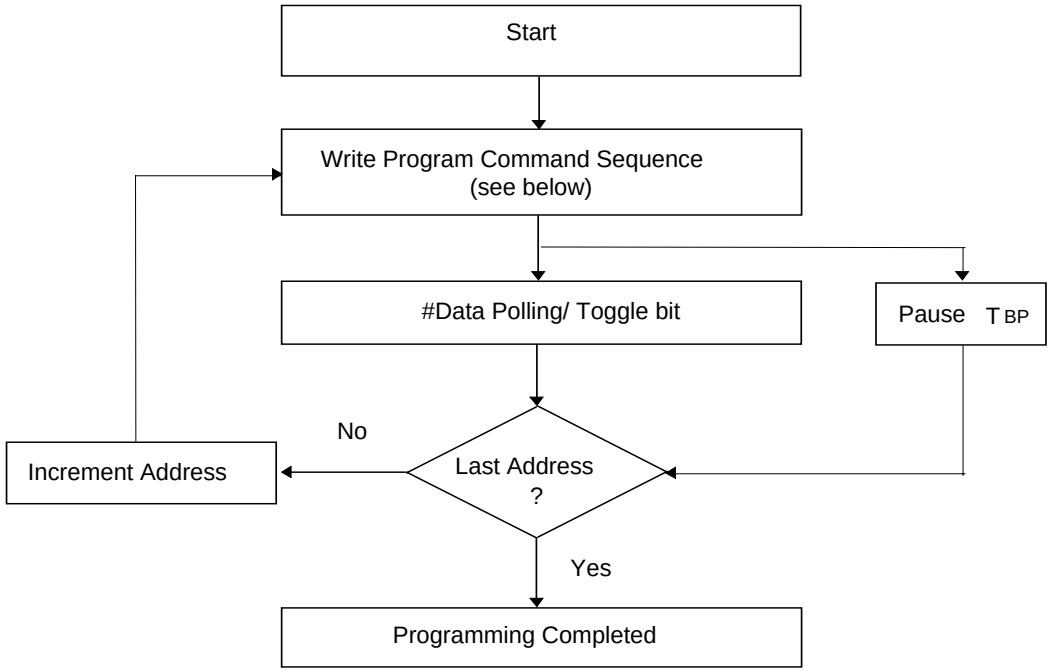
Notes:

1. Address Format: A14 – A0 (Hex); Data Format: DQ7 – DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.
3. PA: Page Address

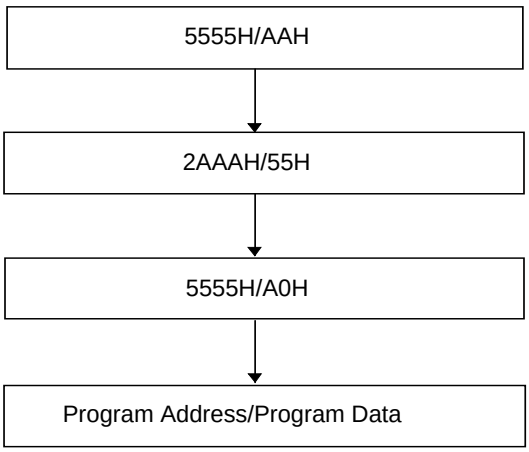
PA = 1FXXXh for Page 31	PA = 0FXXXh for Page 15
PA = 1EXXXh for Page 30	PA = 0EXXXh for Page 14
PA = 1DXXXh for Page 29	PA = 0DXXXh for Page 13
PA = 1CXXXh for Page 28	PA = 0CXXXh for Page 12
PA = 1BXXXh for Page 27	PA = 0BXXXh for Page 11
PA = 1AXXXh for Page 26	PA = 0AXXXh for Page 10
PA = 19XXXh for Page 25	PA = 09XXXh for Page 9
PA = 18XXXh for Page 24	PA = 08XXXh for Page 8
PA = 17XXXh for Page 23	PA = 07XXXh for Page 7
PA = 16XXXh for Page 22	PA = 06XXXh for Page 6
PA = 15XXXh for Page 21	PA = 05XXXh for Page 5
PA = 14XXXh for Page 20	PA = 04XXXh for Page 4
PA = 13XXXh for Page 19	PA = 03XXXh for Page 3
PA = 12XXXh for Page 18	PA = 02XXXh for Page 2
PA = 11XXXh for Page 17	PA = 01XXXh for Page 1
PA = 10XXXh for Page 16	PA = 00XXXh for Page 0

4. XX: Don't care

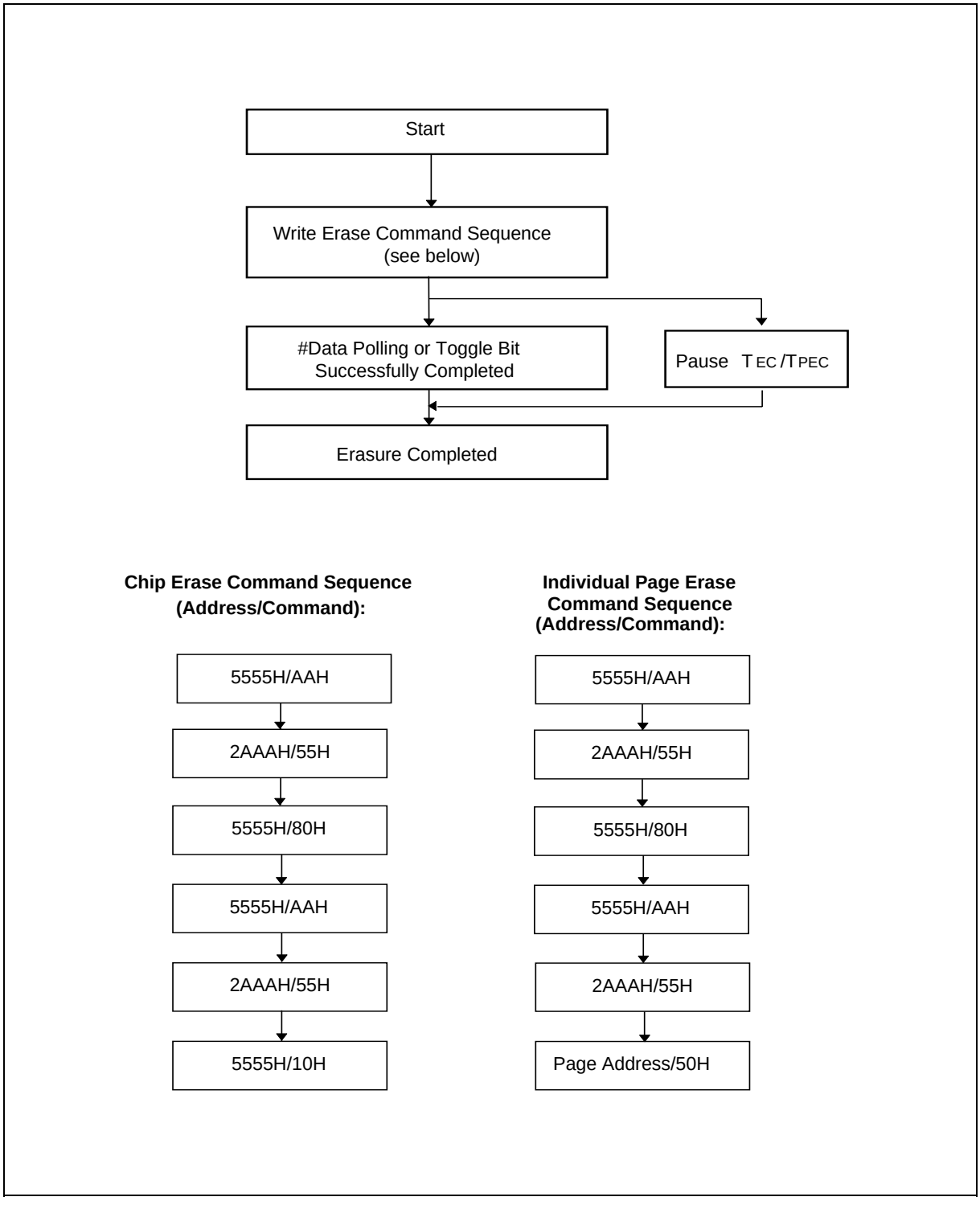
7.3 Embedded Programming Algorithm



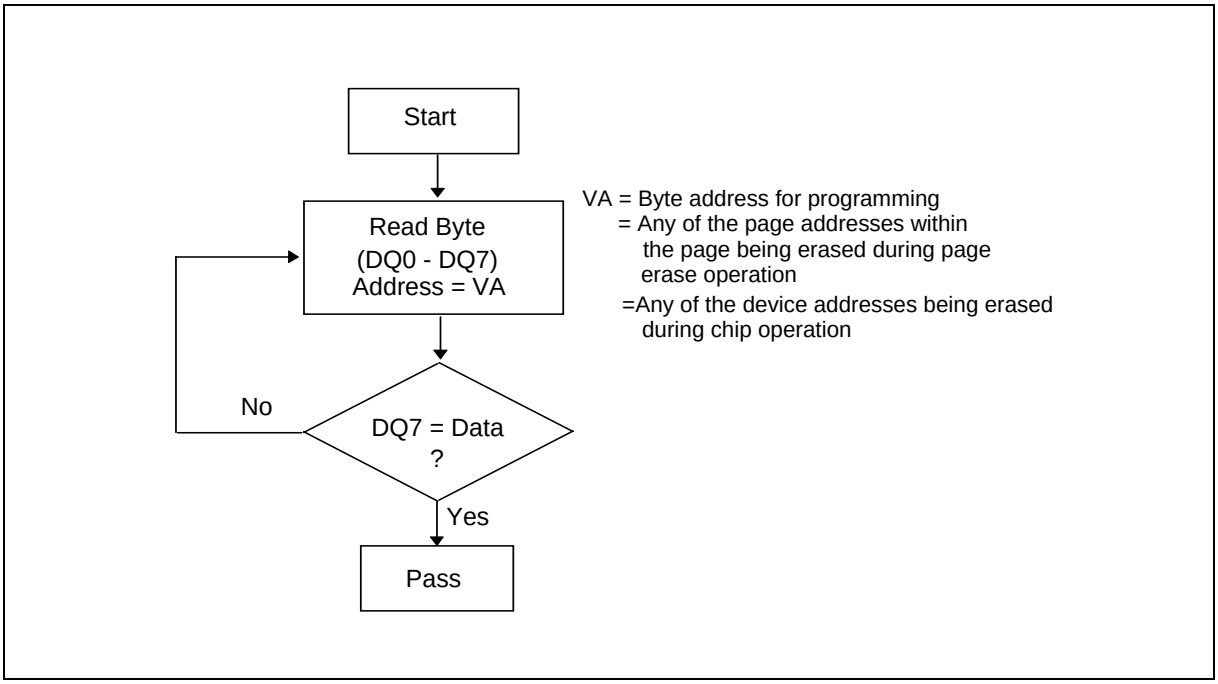
Program Command Sequence (Address/Command):



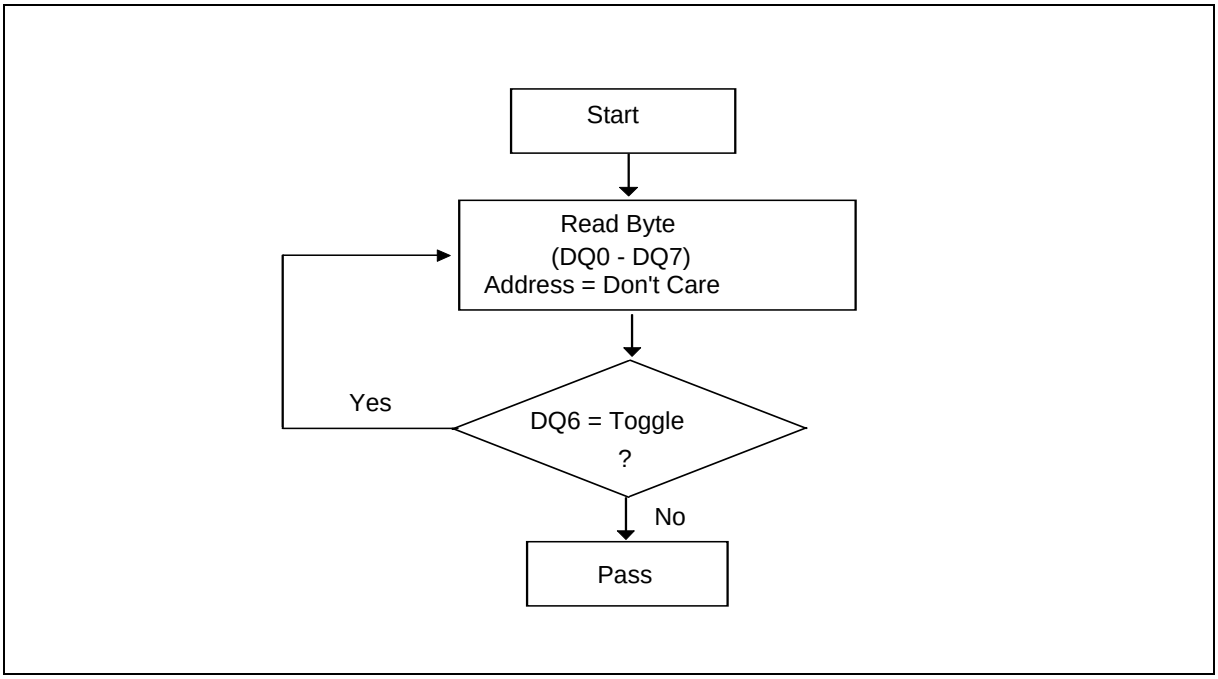
7.4 Embedded Erase Algorithm



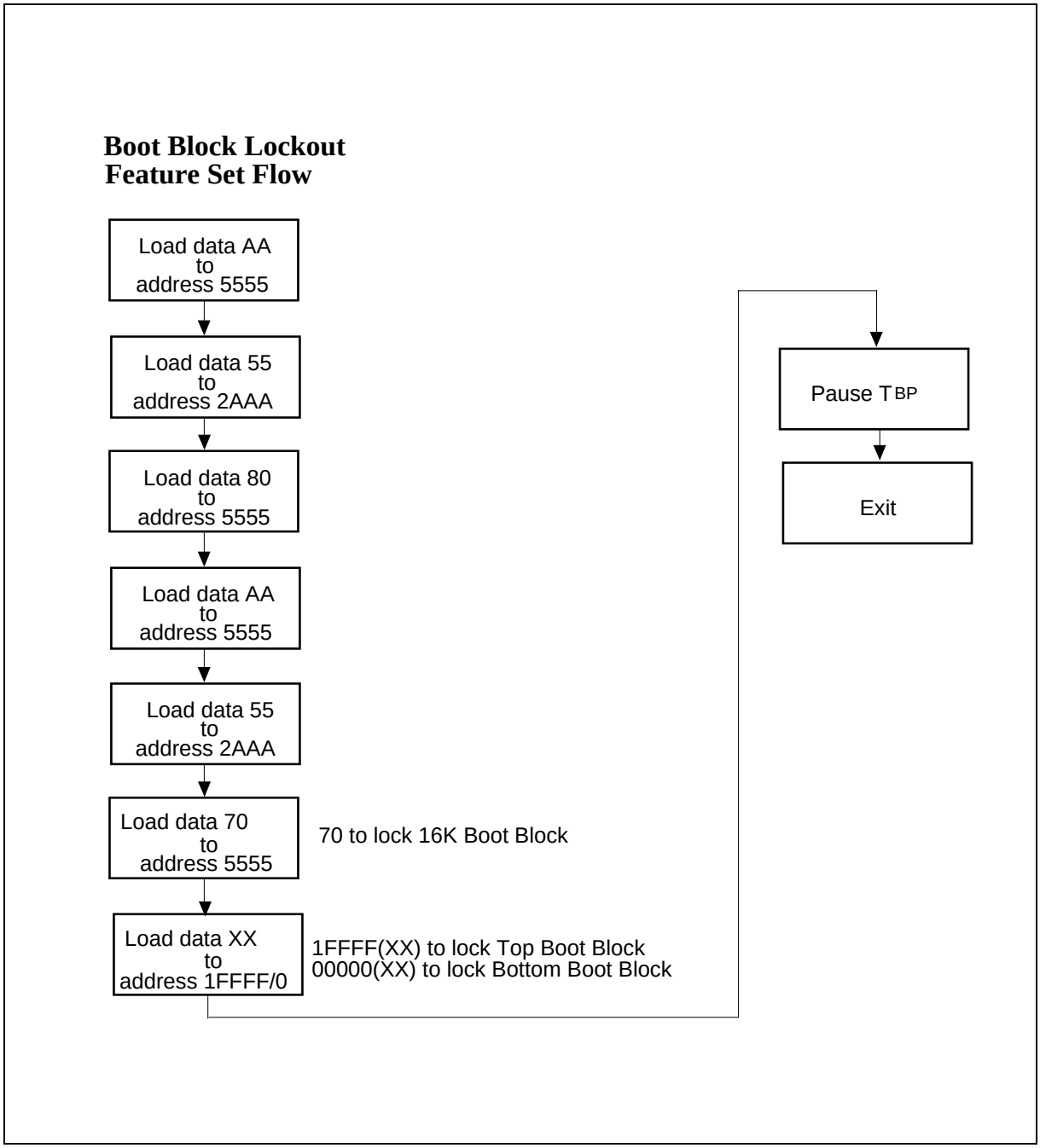
7.5 Embedded #Data Polling Algorithm



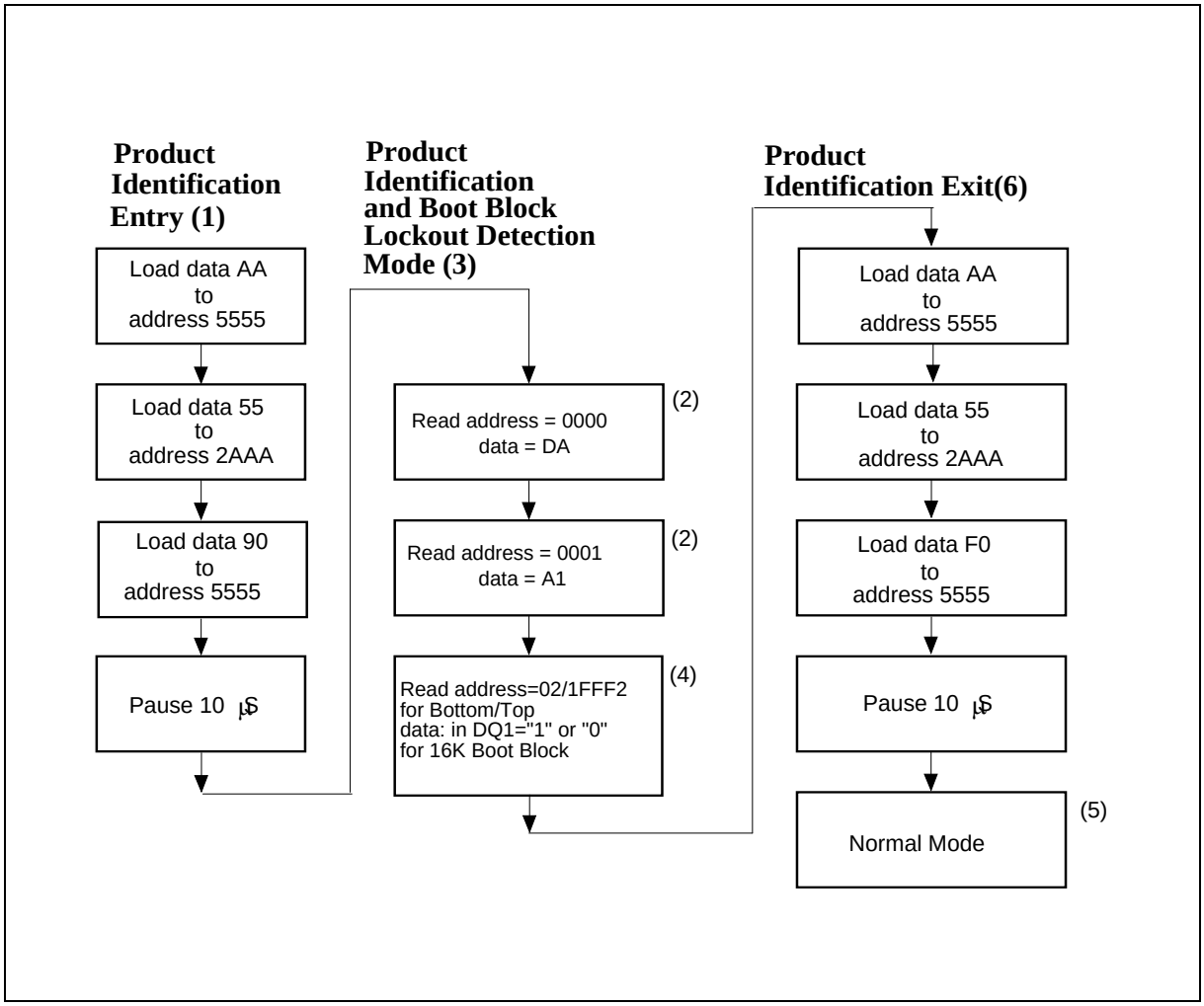
Embedded Toggle Bit Algorithm



7.6 Boot Block Lockout Enable Flow Chart



7.7 Software Product Identification and Boot Block Lockout Detection Flow Chart



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the output data in DQ0 or DQ1= " 1 " the boot block programming lockout feature is activated; if the output data in DQ0 or DQ1= " 0 ," the lockout feature is inactivated and the matched boot block can be programmed.

(5) The device returns to standard operation mode.

(6) Optional 1-byte cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

8. DC CHARACTERISTICS

8.1 Absolute maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-2.0 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
Voltage on Any Pin to Ground Potential Except A9	-2.0 to +7.0	V
Voltage on A9 Pin to Ground Potential	-2.0 to +13.0	V

Note: Exposure to conditions beyond those listed under Absolute maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC Operating Characteristics

(V_{DD} = 5V ±0.5V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{DD}	#CE = #OE = V_{IL}, #WE = V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	15	30	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	#CE = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	1	2	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	#CE = V_{DD} -0.3V, all DQs open Other inputs = V_{DD} -0.3V/ V_{SS}	-	15	50	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	1	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	1	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

8.3 Pin Capacitance

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

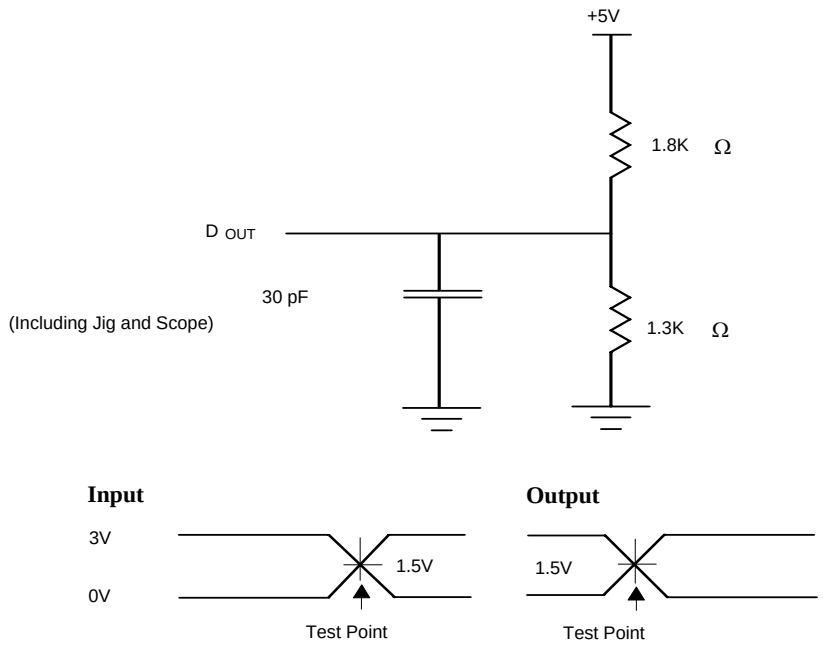
PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	10	12	pF

9. AC CHARACTERISTICS

9.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

9.2 AC Test Load and Waveform



AC Characteristics, continued

9.3 Read Cycle Timing Parameters

(V_{DD} = 5V ±0.5V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39F010-70		W39F010-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	nS
Address Access Time	T_{AA}	-	70	-	90	nS
Output Enable Access Time	T_{OE}	-	35	-	45	nS
#CE Low to Active Output	T_{CLZ}	0	-	0	-	nS
#OE Low to Active Output	T_{OLZ}	0	-	0	-	nS
#CE High to High-Z Output	T_{CHZ}	-	25	-	25	nS
#OE High to High-Z Output	T_{OHZ}	-	25	-	25	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	nS

9.4 Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	40	-	-	nS
#WE and #CE Setup Time	T_{CS}	0	-	-	nS
#WE and #CE Hold Time	T_{CH}	0	-	-	nS
#OE High Setup Time	T_{OES}	0	-	-	nS
#OE High Hold Time	T_{OEH}	0	-	-	nS
#CE Pulse Width	T_{CP}	100	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	40	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Byte programming Time	T_{BP}	-	35	50	µS
Chip Erase Cycle Time	T_{EC}	-	50	100	mS
Page Erase Cycle Time	T_{EP}	-	12.5	25	mS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

AC Characteristics, Continued

9.5 Power-up Timing

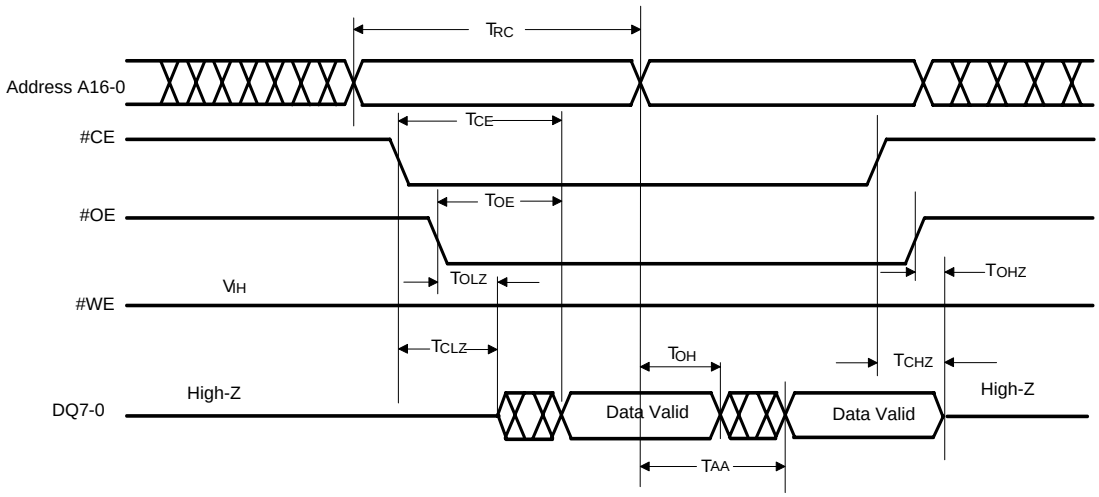
PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	μS
Power-up to Write Operation	TPU. WRITE	5	mS

9.6 Data Polling and Toggle Bit Timing Parameters

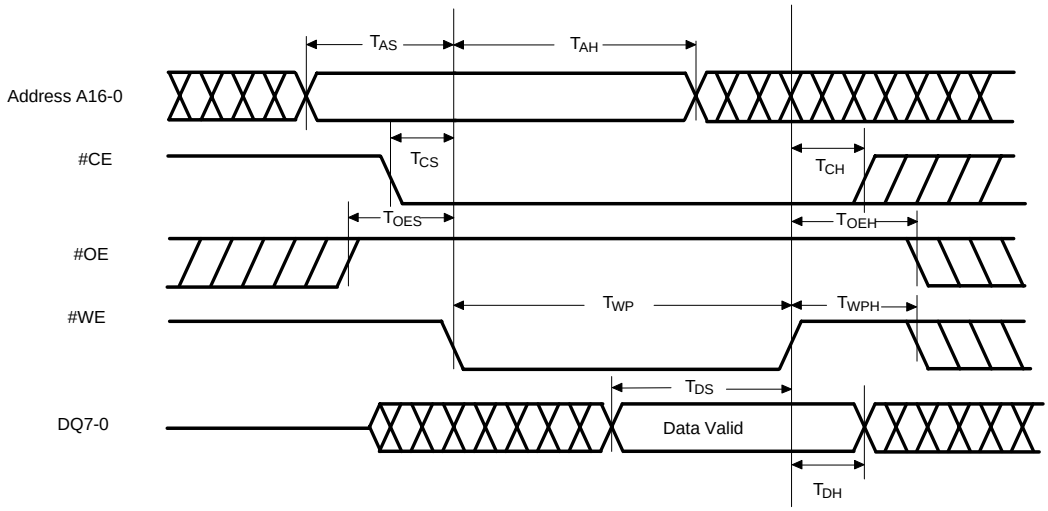
PARAMETER	SYM.	W39F010-70		W39F010-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
#OE to Data Polling Output Delay	TOEP	-	35	-	45	nS
#CE to Data Polling Output Delay	TCEP	-	70	-	90	nS
#OE to Toggle Bit Output Delay	TOET	-	35	-	45	nS
#CE to Toggle Bit Output Delay	TCET	-	70	-	90	nS

10. TIMING WAVEFORMS

10.1 Read Cycle Timing Diagram

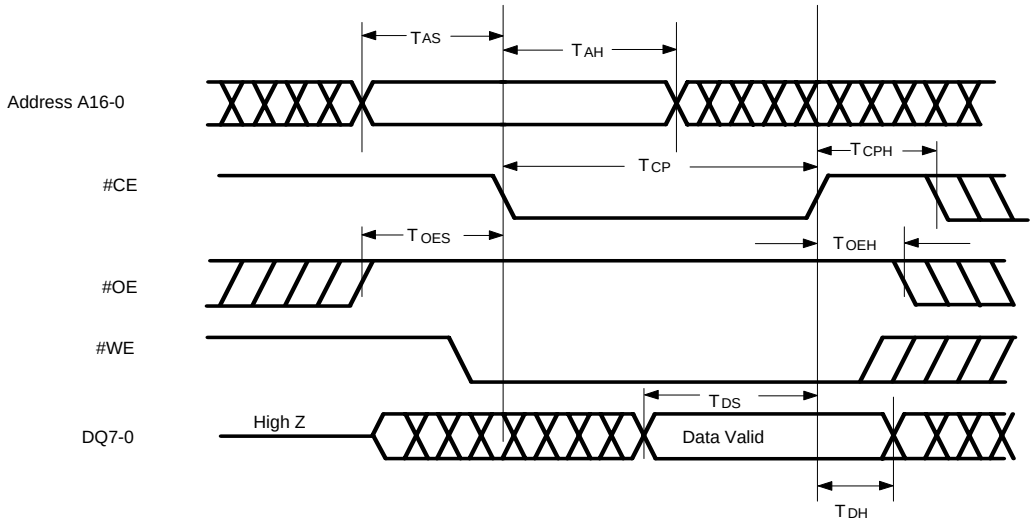


10.2 #WE Controlled Command Write Cycle Timing Diagram

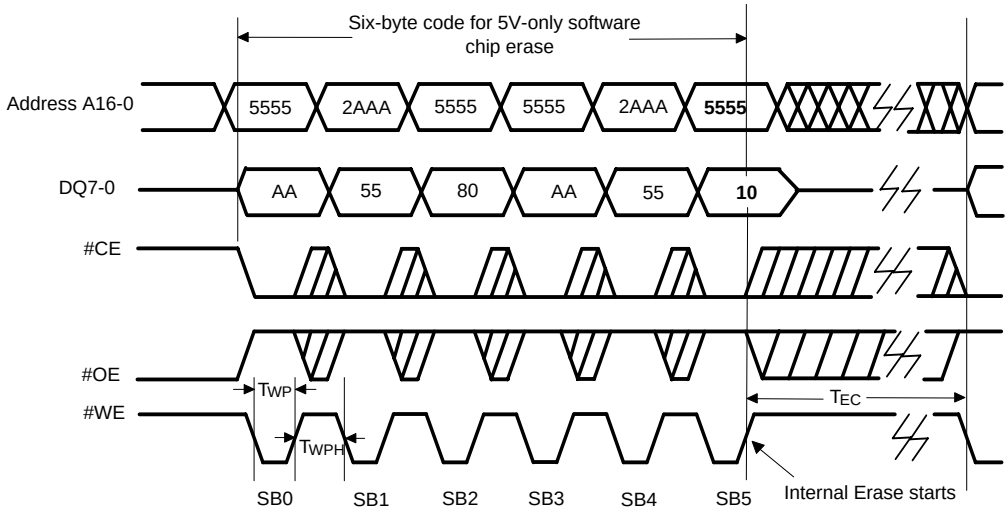


Timing Waveforms, Continued

10.3 #CE Controlled Command Write Cycle Timing Diagram

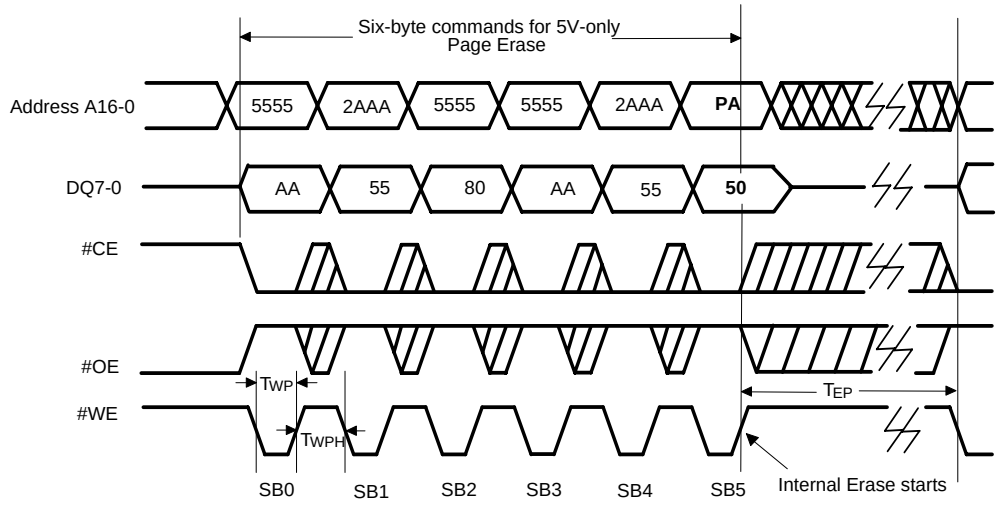


10.4 Chip Erase Timing Diagram



Timing Waveforms, Continued

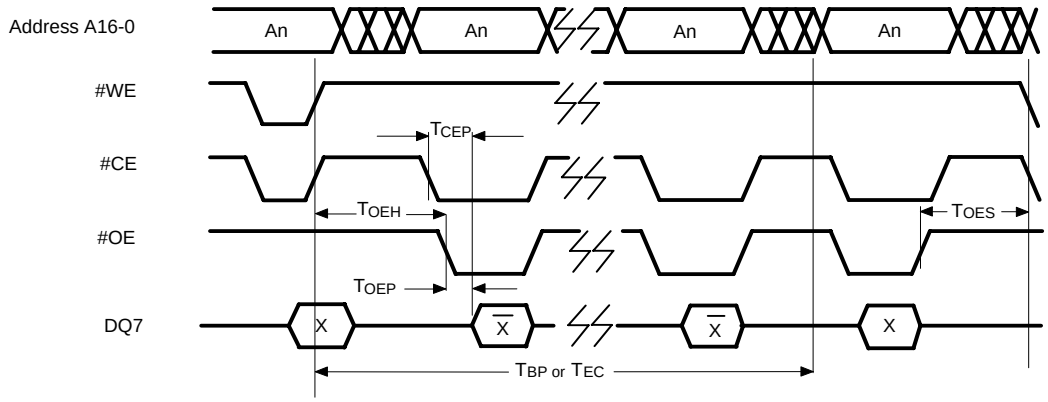
10.5 Page Erase Timing Diagram



PA = Page Address

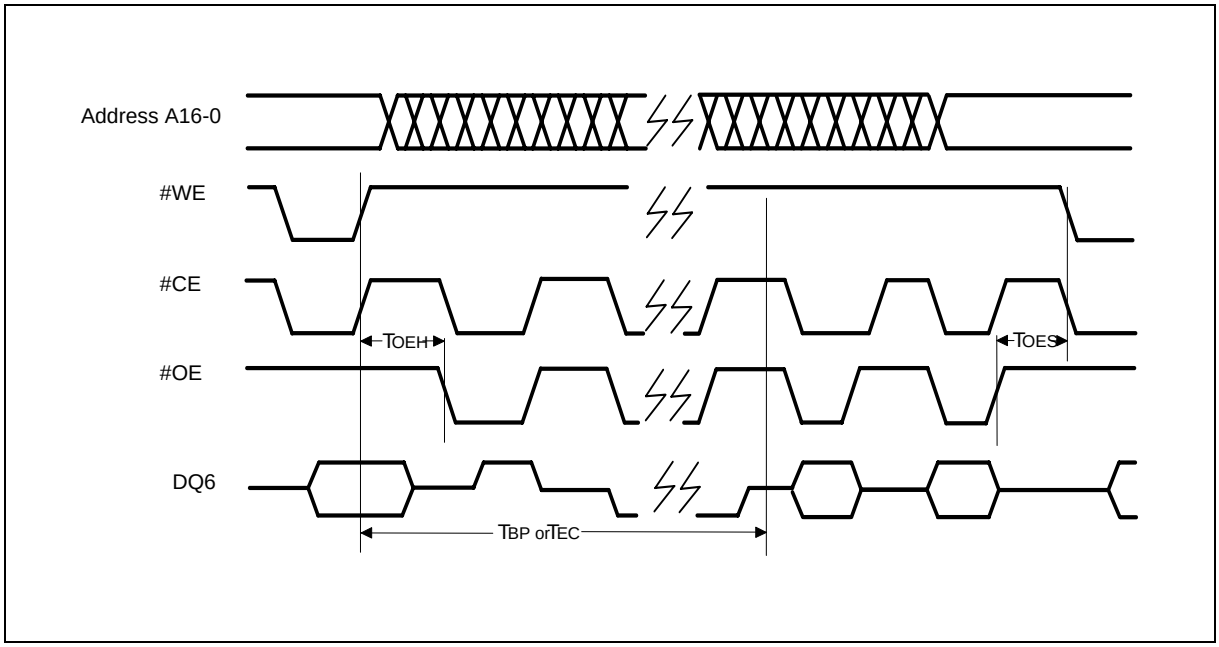
Please refer to page 9 for detail informati

10.6 #DATA Polling Timing Diagram



Timing Waveforms, Continued

10.7 Toggle Bit Timing Diagram



11. ORDERING INFORMATION

PART NO.	ACCESS TIME (NS)	POWER SUPPLY CURRENT MAX. (MA)	STANDBY VDD CURRENT MAX. (MA)	PACKAGE	CYCLE
W39F010-70B	70	30	2	32-pin DIP	10K
W39F010-90B	90	30	2	32-pin DIP	10K
W39F010T-70B	70	30	2	32-pin TSOP (8 mm x 20 mm)	10K
W39F010T-90B	90	30	2	32-pin TSOP (8 mm x 20 mm)	10K
W39F010Q-70B	70	30	2	32-pin STSOP (8 mm x 14 mm)	10K
W39F010Q-90B	90	30	2	32-pin STSOP (8 mm x 14 mm)	10K
W39F010P-70B	70	30	2	32-pin PLCC	10K
W39F010P-90B	90	30	2	32-pin PLCC	10K
W39F010P-70Z	70	30	2	32-pin PLCC (Lead free)	10K
W39F010P-90Z	90	30	2	32-pin PLCC (Lead free)	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

12. HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin PLCC W39F010P-70

1st line: winbond logo

2nd line: the part number: W39F010P-70

3rd line: the lot number

4th line: the tracking code: 149 O B SA

149: Packages made in '01, week 49

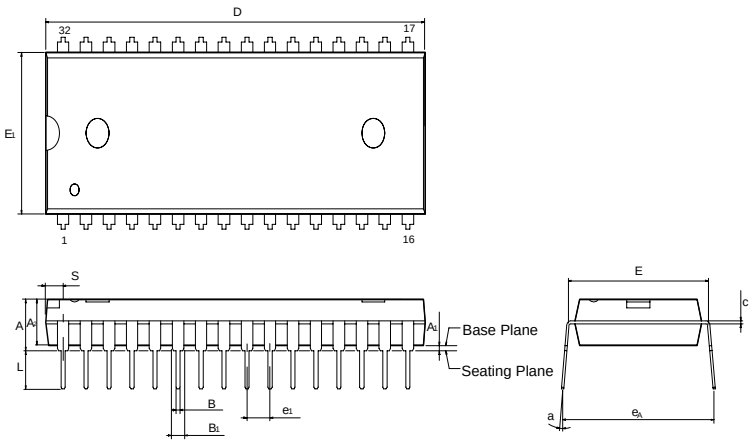
O: Assembly house ID: A means ASE, O means OSE, ...etc.

B: IC revision; A means version A, B means version B, ...etc.

SA: Process code

13. PACKAGE DIMENSIONS

13.1 32-pin P-DIP

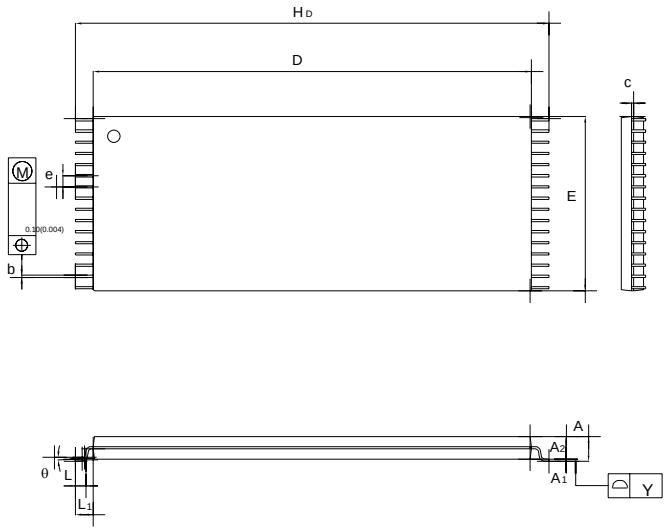


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold fl
   tie bar burrs.
2. Dimension E1 does not include interlea
3. Dimensions D & E1 include mold mism
   are determined at the mold parting li
4. Dimension B1 does not include dam
   protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be b
   final visual inspection spec.

13.2 32-pin TSOP (8 x 20 mm)

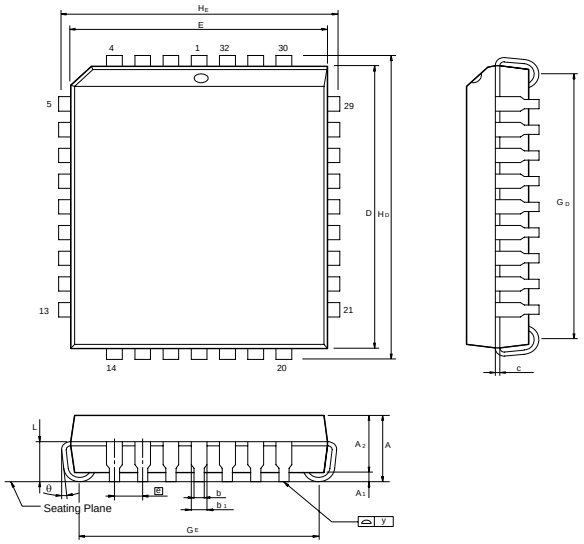


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:
Controlling dimension: Millimeters

Package Dimensions, Continued

13.3 32-pin PLCC

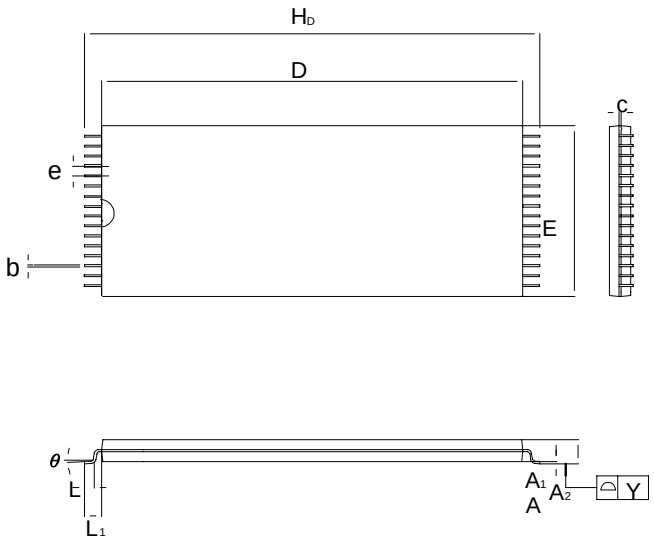


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.

13.4 32-pin STSOP (8 x 14 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 2000	-	Initial Issued
A2	June 17, 2002	1, 23	Add cycle of 1K
		1	Change active current from 10 to15mA (typ.) Change standby current from 20 to15 μA (typ.)
		4	Modify Low VDD Inhibit
		10, 11, 12	Delete old flow chart and add Embedded Algorithm
		10	Remove Block Erase from the Embedded Erase Algorithm
		11	Correct Embedded #Data Polling Algorithm
		16	Change IDD from 10/20 mA to15/30 mA (typ./max.) Change ISB2 from 20/50 μA to15/50 μA (typ./max.)
		1, 23	Rename TSOP (8 x 14 mm) as STSOP (8 x 14 mm)
		24	Add HOW TO READ THE TOP MARKING
A3	April 15, 2005	27	Add Important Notice
A4	December 26, 2005	27	Add 32-pin PLCC lead free part

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064