MOTOROLA

32K x 9 Bit Synchronous Static RAM

62S950A

Commercial Plus and Mil/Aero Applications

ELECTRICALLY TESTED PER:
MPG62S950A

The 62S950A is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, high-speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of external clock (K). Asynchronous control consist of output enable ($\overline{G}$). CMOS circuitry reduces the overall power consumption and provides for greater reliability.

Address (A_0-A_{14}) and control signals, except output enable ($\overline{G}$), are sampled through positive-edge triggered noninverting registers. Data outputs are asynchronously controlled by ($\overline{G}$).

Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{W}$) at the rising edge of (K). Data for the write may be delayed until the latter half of the write cycle.

The 62S950A is packaged in a 32-pin ceramic leadless chip carrier (LCC). Multiple ground pins have been utilized to minimize effects induced by output noise.

- Single 5.0 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times — 15, 25, 35 ns and Cycle Times — 15, 25, 35 ns
- Internal Input Register (Address Control)
- Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability — 85 pF per I/O
- High Board Design LCC Package
- Active High Chip Select Input for Easy Depth Expansion

Note: All power supply and ground pins must be connected for proper operation of the device.

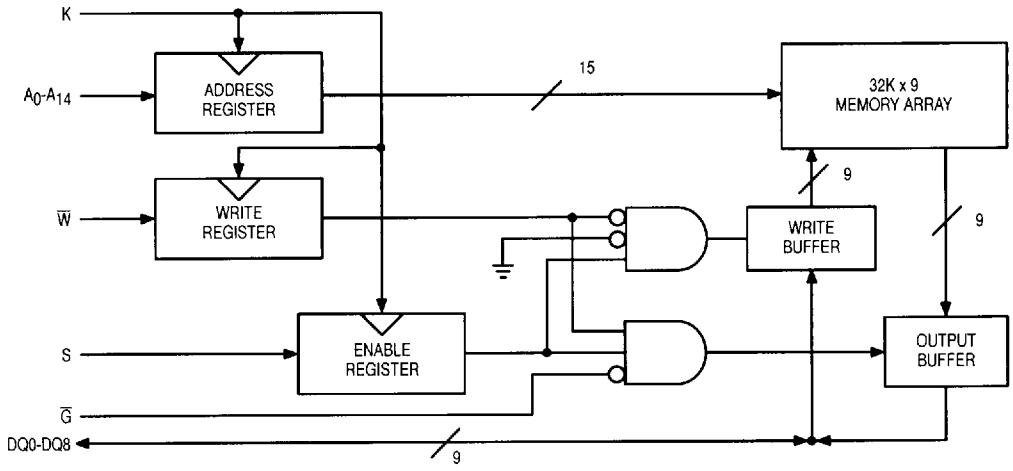
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 62S950A - XX/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE:
LCC: U

XX = Speed in ns (15, 25, 35)

BLOCK DIAGRAM



PIN ASSIGNMENT AND FUNCTION TABLE

Pin	Symbol	Name
1	A13	Address Input
2	A12	Address Input
3	A11	Address Input
4	A10	Address Input
5	A9	Address Input
6	A8	Address Input
7	A7	Address Input
8	V_{CC}	+5 V Power Supply
9	K	Clock
10	V_{SS}	Ground
11	A0	Address Input
12	A1	Address Input
13	A2	Address Input
14	A3	Address Input
15	A4	Address Input
16	A5	Address Input

Pin	Symbol	Name
17	A6	Address Input
18	DQ0	Data Input/Output
19	DQ1	Data Input/Output
20	V_{SS}	Ground
21	DQ2	Data Input/Output
22	DQ3	Data Input/Output
23	$\overline{SW}$	Synchronous Write
24	V_{SS}	Ground
25	$\overline{G}$	Output Enable
26	S0	Chip Select
27	DQ8	Data Input/Output
28	DQ4	Data Input/Output
29	DQ5	Data Input/Output
30	DQ6	Data Input/Output
31	DQ7	Data Input/Output
32	A14	Address Input

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

S0	$\overline{SW}$	$\overline{G}$	K	Operation	I/O Status
L	X	X	L-H	Deselected	High-Z
H	L	X	L-H	Write	High-Z
H	L	X	L	Write	Data-In
H	H	—	L-H	Read Initiated	—
H	H	H	X	Read	High-Z
H	H	L	X	Read	Data-Out

Notes:
1. X = Don't Care.
2. S0 and $\overline{SW}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. $\overline{W}$ = L for the last clock transition from low to high. Similarly for S = H.

AC TEST LOADS OR EQUIVALENT

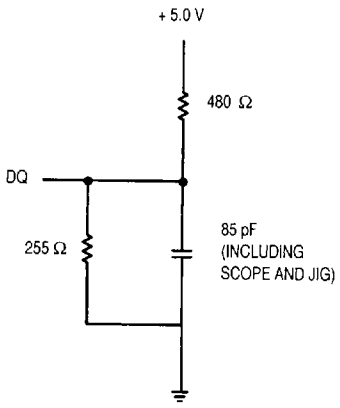


Figure 1A.

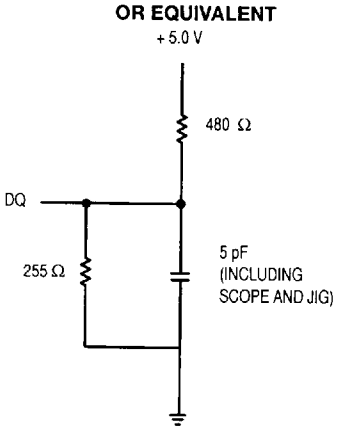


Figure 1B.

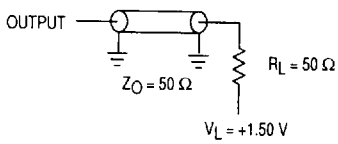


Figure 1C.

ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS} = 0 V)			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{OUT}	± 20	mA
Power Dissipation (T_A = 25°C, V_{CC} = 5 V, t_{KHKH} = 20 ns)	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 55 to +125	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Temperature Range	T_A	– 55 to +125	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55 to + 125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5 *	0.0	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, S0 = V_{IH}, All Inputs = V_{IL} = 0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) t_{KHKH} = 15 ns	I_{CCA}	—	170	mA
Standby Current (S0 = V_{IL}, All Inputs = V_{IL} and V_{IH})	I_{SB1}	—	40	mA
CMOS Standby Current (S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	0.1	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (all Pins Expect DQ0-DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0-DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55 to + 125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ... See Figure 1A Unless Otherwise Noted

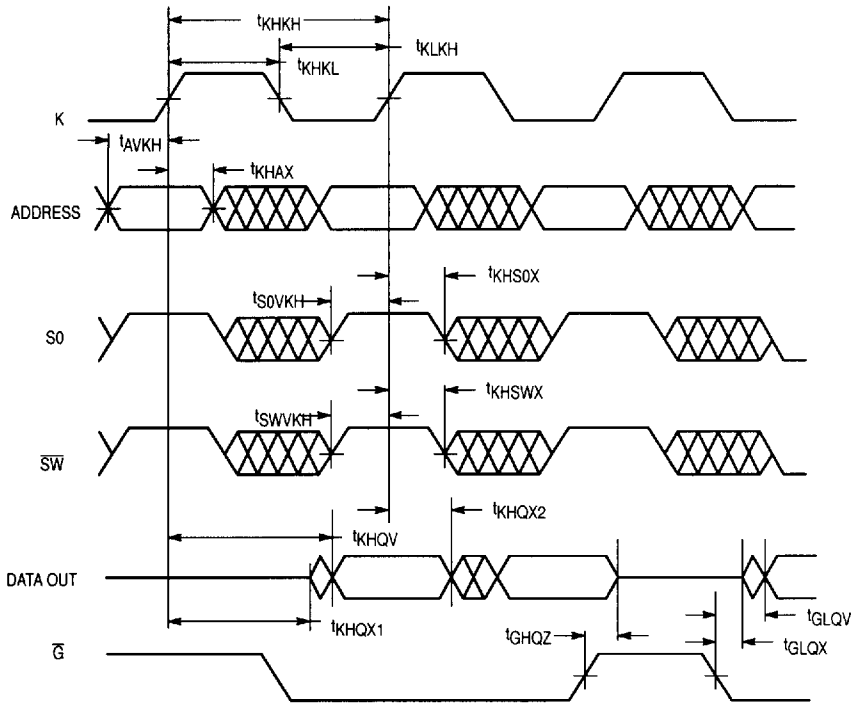
Read/Write Cycle Timing (See Note 1, 2, and 3)

Parameter	Symbol	62S950A-15		62S950A-25		62S950A-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Cycle Time	t_{KHKH}	15	—	25	—	35	—	ns	6
Clock High Pulse Width	t_{KHKL}	7	—	11	—	20	—	ns	
Clock Low Pulse Width	t_{KLKH}	7	—	11	—	20	—	ns	
Read Access Times:									
Clock Access Time	t_{KHQV}	—	15	—	25	—	35	ns	
Output Enable to Output Valid	t_{GLQV}	—	6	—	10	—	15	ns	
Write Cycles:									
Data-In Valid to Clock High (Transparent Data)	t_{DVKH}	6	—	6	—	6	—	ns	
Clock High to Data Invalid (Transparent Data)	t_{KHDX}	2	—	2	—	2	—	ns	
Output Buffer Control:									
Clock High to Output Low-Z after Write	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQX}	—	8	—	10	—	12	ns	4
Clock High to Q High-Z	t_{KHQZ}	—	8	—	8	—	8	ns	4
Register Setup Times for:									
Address Synchronous Write Chip Select	t_{AVKH} t_{WVKH} t_{S0VKH}	2	—	2	—	2	—	ns	5
Register Hold Times for:									
Address Synchronous Write Chip Select	t_{KHAX} t_{KHWX} t_{KHS0X}	2	—	2	—	2	—	ns	5

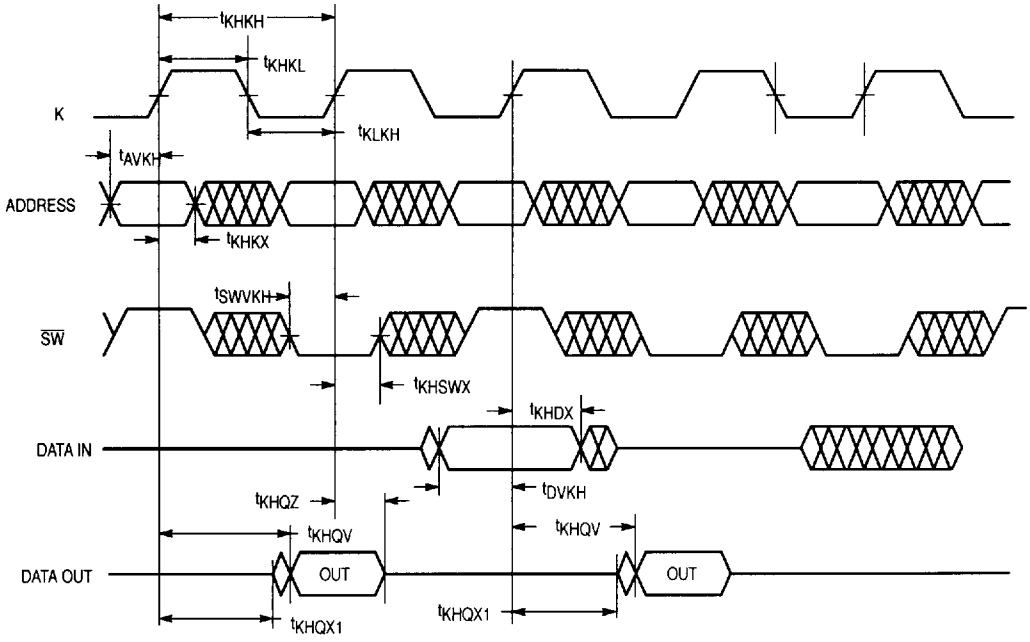
NOTES:

1. A read cycle is defined by $\overline{SW}$ high for the setup and hold times. A write cycle is defined by $\overline{SW}$ low for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. G is a don't care when $\overline{SW}$ is sampled low.
4. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. At any given voltage and temperature, $t_{GHQZmax}$ is less than $t_{GLQXmin}$, for a given device and from device to device.
5. This is a synchronous device. All address inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) when the device is selected. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of the clock (K) when the device is selected.
6. See Figure 1C.

READ CYCLE

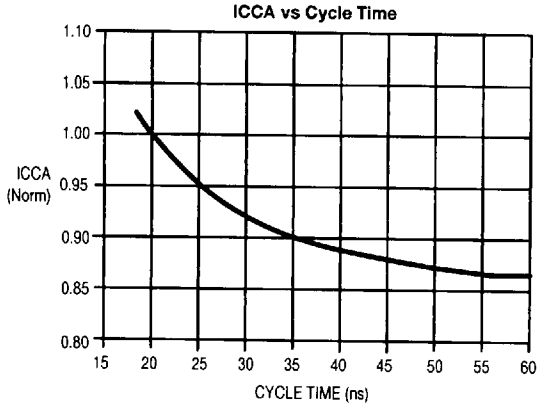


READ-WRITE-READ CYCLE

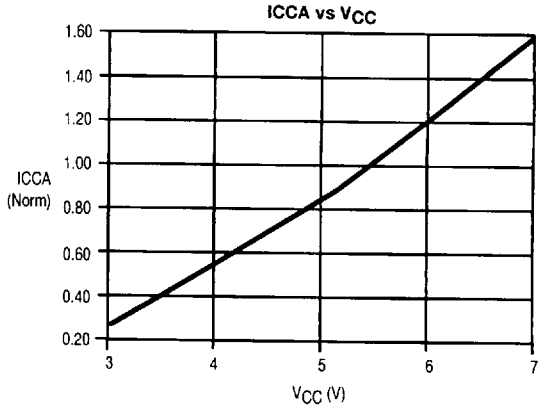


Derating Curves

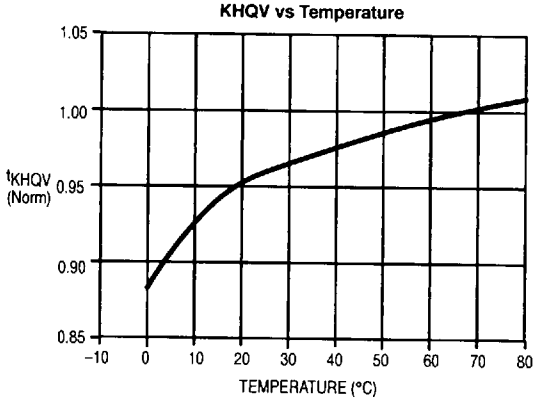
ICCA vs Cycle Time



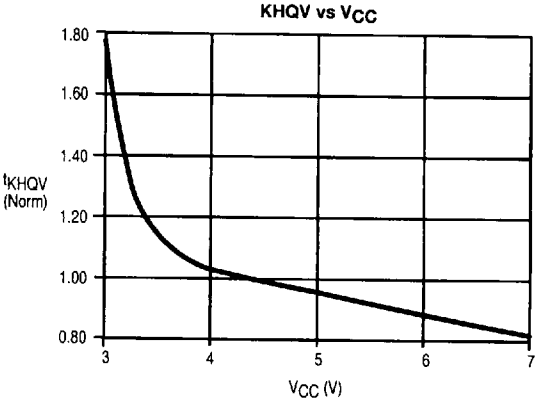
ICCA vs V_{CC}



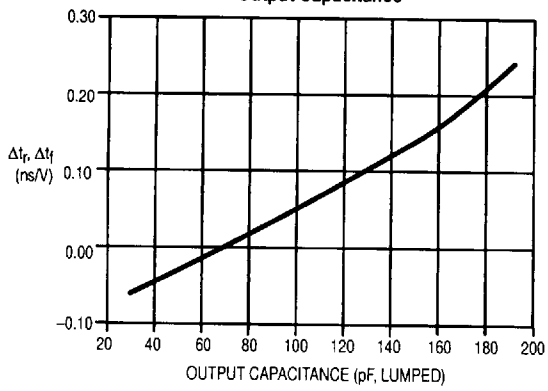
KHQV vs Temperature



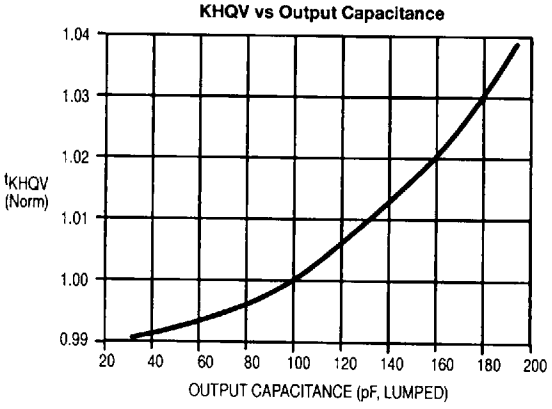
KHQV vs V_{CC}



Change In Output Rise/Fall Times vs Output Capacitance



KHQV vs Output Capacitance



NOTE:
Derating curves are based on component typical values