4 MEG x 16 DRAM

Extended Data Out (EDO) DRAM

FEATURES

- Single +3.3V ±0.3V power supply.
- Industry-standard x16 pinout, timing, functions, and package.
- 12 row, 10 column addresses
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle CAS\-BEFORE-RAS\ (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention
- Level 1 Moisture Sensitivity Rating, JEDEC J-STD-020

OPTIONS — MARKINGS

- Package(s)
  - 50-pin TSOP (400-mil) — DG
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Refresh Rates
  - Standard Refresh — None
  - Self Refresh — S*
- Operating Temperature Ranges
  - Military (-55°C to +125°C) — XT
  - Industrial (-40°C to +85°C) — IT

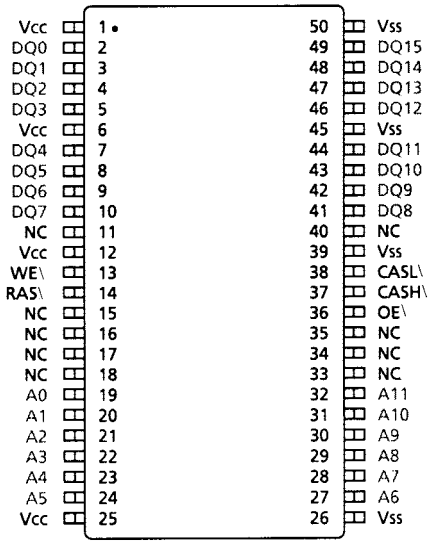
NOTE: The \ symbol indicates signal is active LOW.

*Contact factory for availability. Self refresh option available on IT version only.

PIN ASSIGNMENT

(Top View)

50-Pin TSOP (DG)



Configuration	4 Meg x 16
Refresh	4K
Row Address	A0-A11
Column Addressing	A0-A9

KEY TIMING PARAMETERS

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

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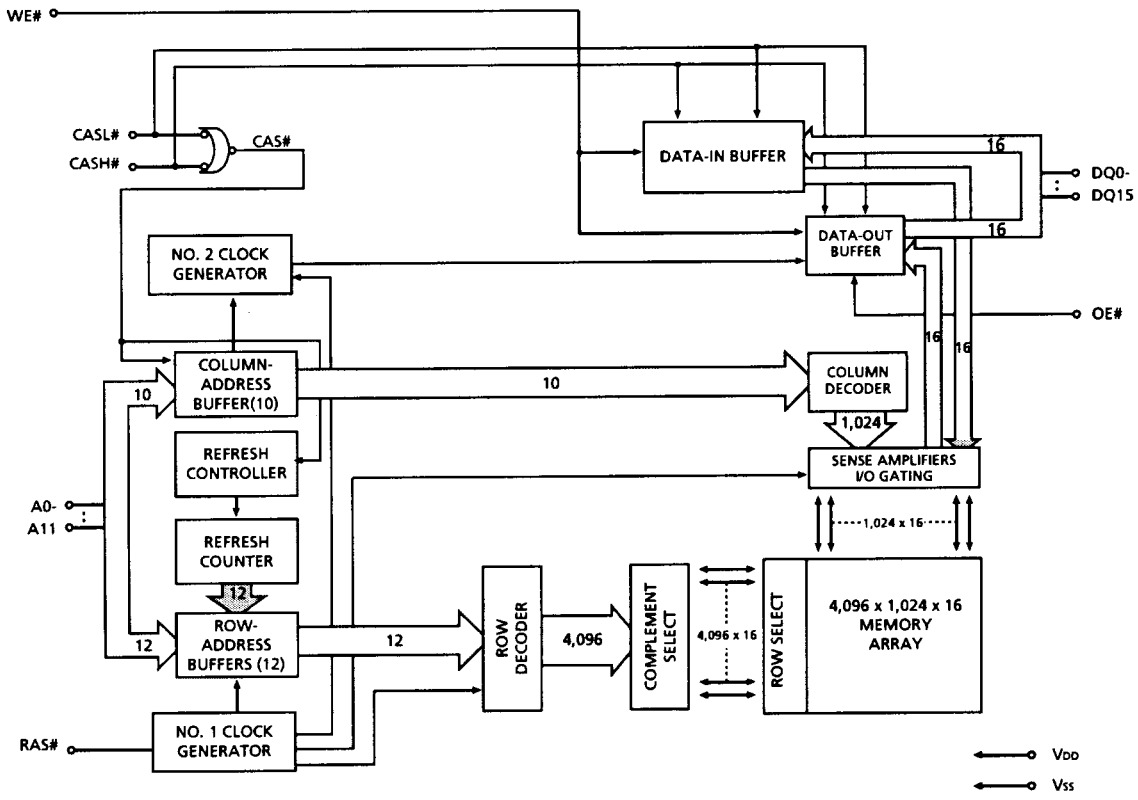
FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The 4 Meg x 16 DRAM is a high-speed CMOS, dynamic random-access memory device containing 67,108,864 bits and designed to operate from 3V to 3.6V. The device is functionally organized as 4,194,304 locations containing 16 bits each. The 4,194,304 memory locations are arranged in 4,096 rows by 1,024 columns. During READ or WRITE cycles, each location is uniquely addresses via the address bits: 12 row-address bits (A0 - A11) and 10 column-address bits (A0 - A9). In addition, both byte and word accesses are supported via the two CAS\ pins (CASL\ and CASH\).

The CAS\ functionality and timing related to address and control functions (e.g., latching column addresses or selecting CBR REFRESH) is such that the internal CAS\ signal is determined by the first external CAS\ signal (CASL\ or CASH\) to transition LOW and the last to transition back HIGH. The CAS\ functionality and timing related to driving or latching data is such that each CAS\ signal independently controls the associated either DQ pins.

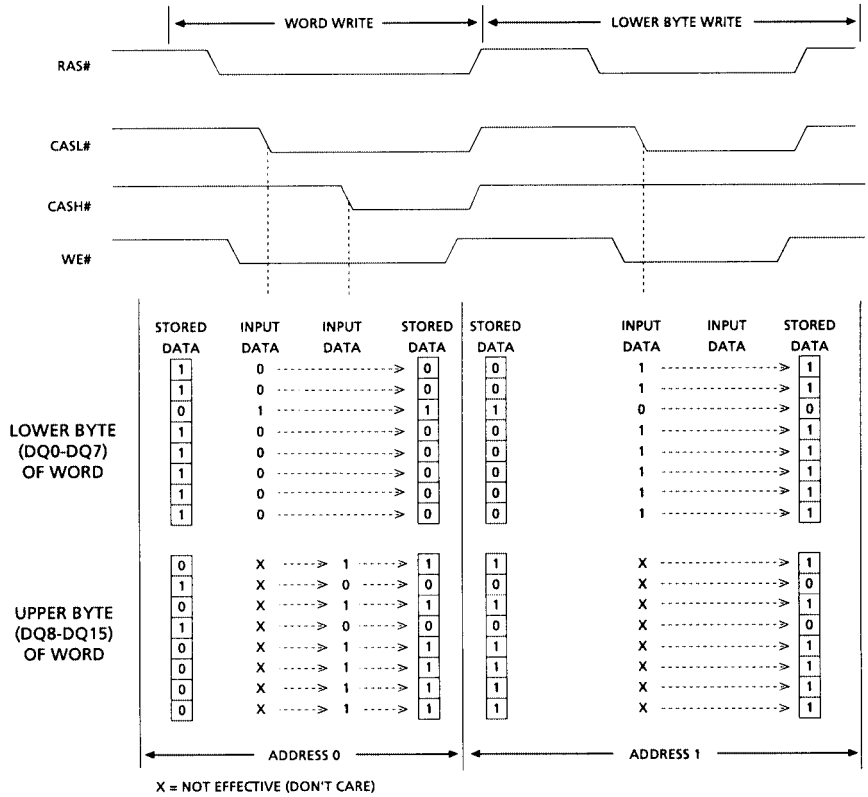
The row address is latched by the RAS\ signal, then the column address is latched by CAS\. This device provides EDO-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The 4 Meg x 16 DRAM must be refreshed periodically in order to retain stored data.

DRAM ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. Use of both CAS\ signals resulted in a word access via the 16 I/O pins (DQ0 - DQ15). Using only one of the two signals results in a BYTE access cycle. CASL\ transitioning LOW selects an access cycle for the lower byte (DQ0 - DQ7), and CASH\ transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15). General byte and word access timing is shown in Figures 1 and 2.

FIGURE 1: WORD and BYTE WRITE Example



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DRAM ACCESS (continued)

A logic HIGH on WE\ dictates read mode, while a logic LOW on WE\ dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS\ (CASL\ or CASH\), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either CAS\ falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after CAS\ (CASL\ or CASH\) is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE\. During LATE WRITE or READ-MODIFY-WRITE cycles, OE\ must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE\ LOW, no write will occur, and the data outputs will drive read data from the accessed location.

Additionally, both bytes are active. A CAS\ precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS\ precharge has been satisfied, are permissible.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS\. If CAS\ went HIGH and OE\ was LOW (active), the output buffers would be disabled. The 64MB EDO DRAM offers an accelerated page mode cycle by eliminating output disable from CAS\ HIGH. This option is called EDO, and it allows CAS\ precharge time (t_{CP}) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates like any DRAM READ or FAST-PAGE-MODE READ, except data is held valid after CAS\ goes HIGH, as long as RAS\ and OE\ are held LOW and WE\ is held HIGH. OE\ can be brought LOW or HIGH while CAS\ and RAS\ are LOW, and the DQs will transition between valid data and High-Z. Using OE\, there are two methods to disable the outputs and

FIGURE 2: WORD and BYTE READ Example

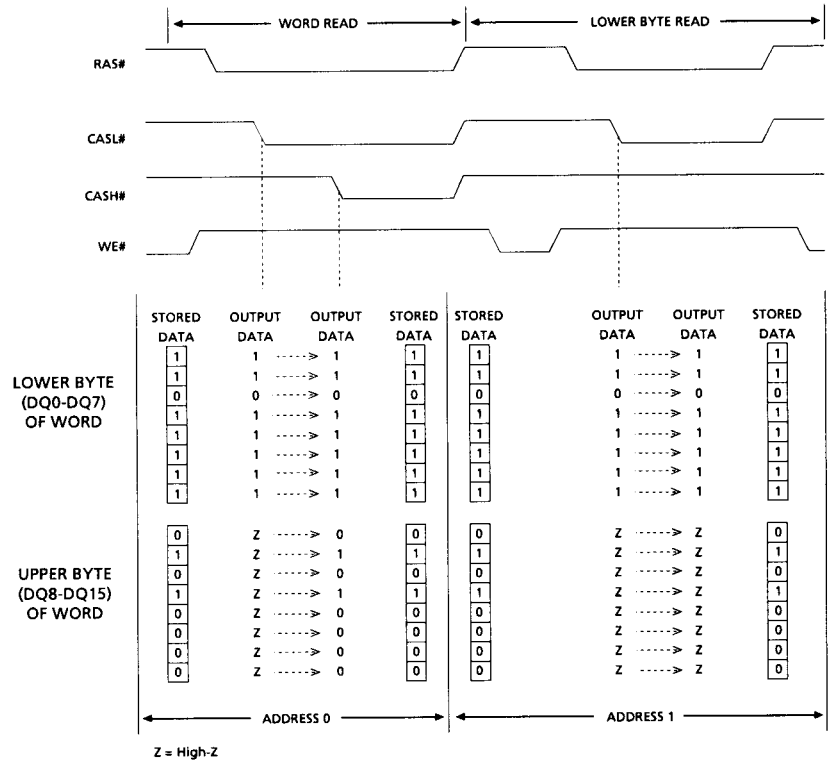

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FIGURE 3: OE\ Control of DQs

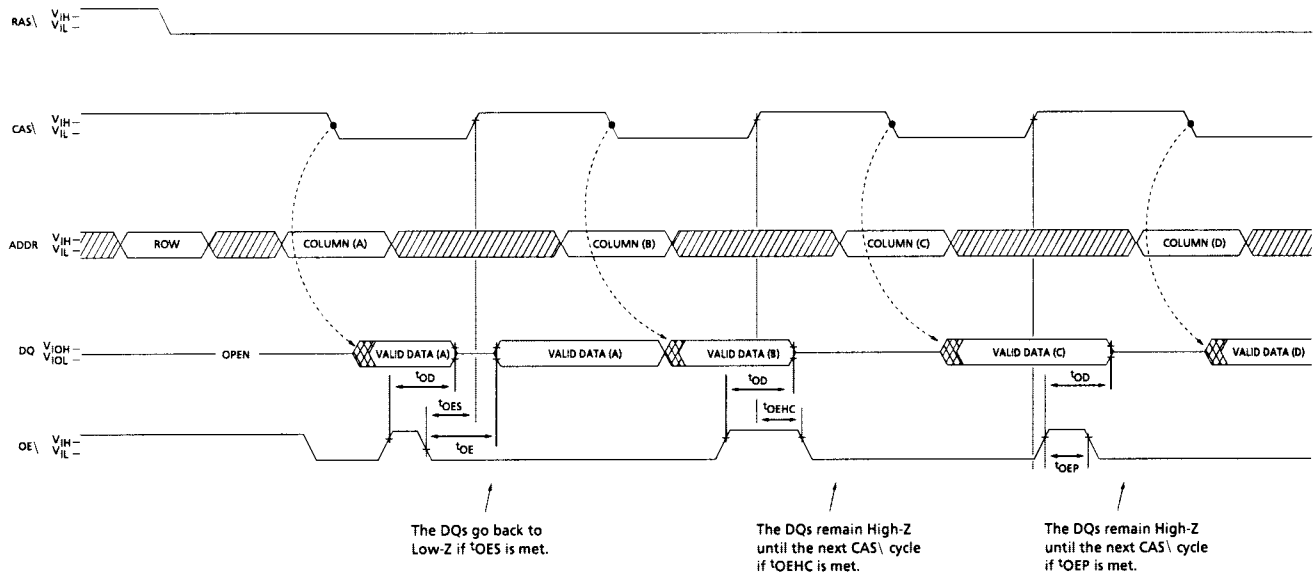
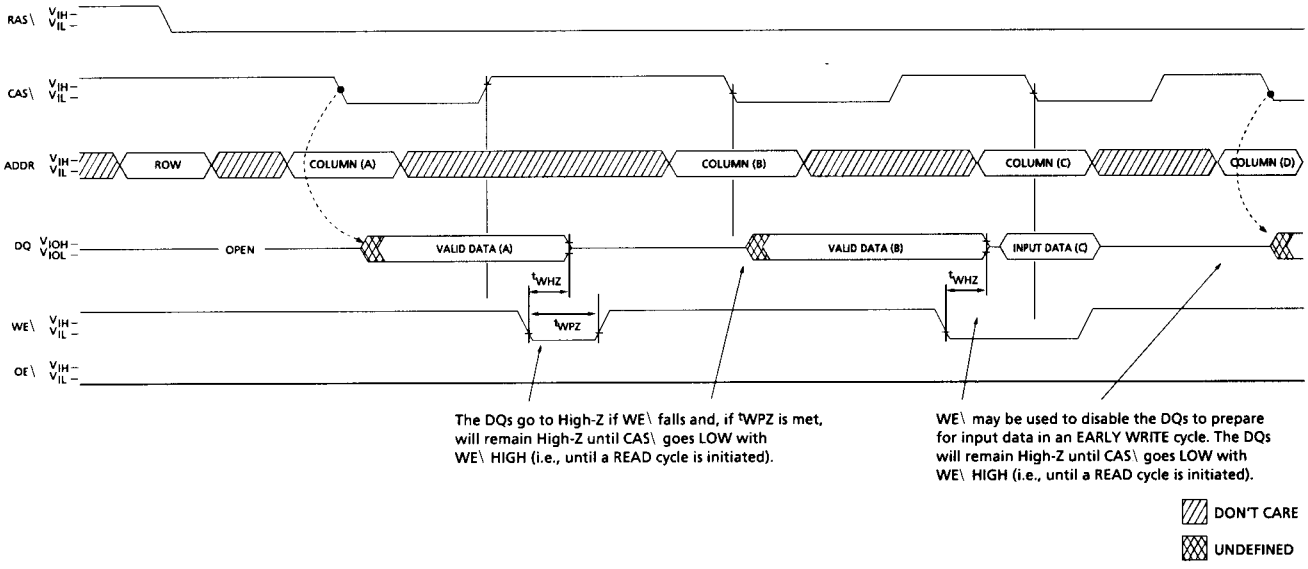


FIGURE 4: WE\ Control of DQs



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EDO PAGE MODE (Continued)

two methods to disable the outputs and keep them disabled during the CAS\ HIGH time. The first method is to have OE\ HIGH when CAS\ transitions HIGH and keep OE\ HIGH for tOEHC thereafter. This will disable the DQs, and they will remain disabled (regardless of the state of OE\ after that point) until CAS\ falls again. The second method is to have OE\ LOW when CAS\ transitions HIGH and then bring OE\ HIGH for a minimum of t_{OEP} anytime during the CAS\ HIGH period. This will disable the DQs, and they will remain disabled (regardless of the state of OE\ after that point) until CAS\ falls again (see Figure 3). During other cycles, the outputs are disabled at t_{OFF} time after RAS\ and CAS\ are HIGH or at t_{WHZ} after WE\ transitions LOW. The t_{OFF} time is referenced from the rising edge of RAS\ or CAS\, whichever occurs last. WE\ can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 4.

EDO-PAGE-MODE operations are always initiated with a row address strobed in by the RAS\ signal, followed by a column address strobed in by CAS\, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS\ while holding RAS\ LOW and entering new column addresses with each CAS\ cycle. Returning RAS\ HIGH terminates the EDO-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all rows in the 4 Meg x 16 DRAM array at least once every 64ms* (4,096 rows). The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms*. The DRAM refreshes one row for every CBR cycle. For this device, executing 4,096 CBR cycles will refresh the entire device. The CBR REFRESH will invoke the internal refresh counter for automatic RAS\ addressing. Alternatively, RAS\-ONLY REFRESH capability is inherently provided. However, with this method, only one row is refreshed on each cycle. JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR Refresh cycle and holding RAS\ low for the specified t_{RASS}. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 31.25µs per cycle, when using a distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS\ HIGH for a minimum time of t_{RPS}. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS\ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh, however, if the controller is using RAS\ only or burst CBR refresh then a burst refresh using t_{RC} (MIN) is required.

NOTES:

*64ms for IT version, 32ms for XT version.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} .....-1V to +4.6V
Voltage on NC, Inputs or I/O Pins
Relative to V_{SS}.....-1V to +4.6V
Power Dissipation.....1W
Operating temperature range, T_A (ambient).....-55°C to 125°C
Storage temperature (plastic).....-55°C to 150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS[1]

(V_{CC} = +3.3V ±0.3V)

PARAMETERS	SYM	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{CC}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	V_{CC} + 0.3	V	35
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-0.3	0.8	V	35
INPUT LEAKAGE CURRENT: Any input at V_{IN} (0V ≤ V_{IN} ≤ V_{CC} +0.3V); All other pins not under test = 0V	I_I	-2	2	µA	36
OUTPUT LEAKAGE CURRENT: Any input at V_{OUT} (0V ≤ V_{OUT} ≤ V_{CC} +0.3V); DQ is disabled and in High-Z state	I_{OZ}	-5	5	µA	
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	---	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	---	0.4	V	

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I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS[1,2,3,5,6]

(V_{CC} = +3.3V ±0.3V)

PARAMETERS	SYM	-5 MAX	-6 MAX	UNITS	NOTES
STANDBY CURRENT: TTL RAS\ = CAS\ = V_{IH}	I_{CC1}	1.5	1.5	mA	
STANDBY CURRENT: CMOS (RAS\ = CAS\ ≥ V_{CC} - 0.2V; DQs may be left open; Other inputs: V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS\, CAS\, address cycling: t_{RC} = t_{RC} [MIN])	I_{CC3}	165	150	mA	26
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS\ = V_{IL}, CAS\, address cycling: t_{PC} = t_{PC} [MIN])	I_{CC4}	125	120	mA	26
REFRESH CURRENT: RAS\-ONLY Average power supply current (RAS\ cycling, CAS\ = V_{IH}: t_{RC} = t_{RC} [MIN])	I_{CC5}	165	150	mA	22
REFRESH CURRENT: CBR Average power supply current (RAS\, CAS\, address cycling: t_{RC} = t_{RC} [MIN])	I_{CC6}	165	150	mA	4, 7, 23
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS\ = 0.2V or CBR cycling; RAS\ = t_{RAS} (MIN); WE\ = V_{CC} - 0.2V; A0 - A10, OE\ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); t_{RC} = 125µS	I_{CC7}	1	1	mA	4, 7, 23, 37
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS\ ≥ t_{RASS} (MIN) and CAS\ held LOW; WE\ = V_{CC} - 0.2V; A0 - A10, OE\ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	1	1	mA	4, 7, 37

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CAPACITANCE[2]

PARAMETER	SYM	MAX	UNIT
Input Capacitance: Address Pins	C_{I1}	5	pF
Input Capacitance: RAS\, CAS\, WE\, OE\	C_{I2}	7	pF
Input/Output Capacitance: DQ	C_{I0}	7	pF

AC ELECTRICAL CHARACTERISTICS[5,6,7,8,9,10,11,12]

(V_{CC} = +3.3V ±0.3V)

DESCRIPTION		-5		-6			
	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	t_{AA}		25		30	ns	
Column-address setup to CAS\ precharge	t_{ACH}	12		15		ns	
Column-address hold time (referenced to RAS\)	t_{AR}	38		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	28
Row-address setup time	t_{ASR}	0		0		ns	28
Column address to WE\ delay time	t_{AWD}	42		49		ns	18
Access time from CAS\	t_{CAC}		13		15	ns	29
Column-address hold time	t_{CAH}	8		10		ns	28
CAS\ pulse width	t_{CAS}	8	10,000	10	10,000	ns	30, 32
CAS\ LOW to "Don't Care" during Self Refresh	t_{CHD}	15		15		ns	
CAS\ hold time (CBR Refresh)	t_{CHR}	8		10		ns	4, 31
Last CAS\ going LOW to first CAS\ to return HIGH	t_{CLCH}	5		5		ns	31
CAS\ to output in Low-Z	t_{CLZ}	0		0		ns	29
Data output hold after CAS\ LOW	t_{COH}	3		3		ns	
CAS\ precharge time	t_{CP}	8		10		ns	13, 33
Access time from CAS\ precharge	t_{CPA}		28		35	ns	29
CAS\ to RAS\ precharge time	t_{CRP}	5		5		ns	31
CAS\ hold time	t_{CSH}	38		45		ns	31
CAS\ setup time (CBR Refresh)	t_{CSR}	5		5		ns	4, 28
CAS\ to WE\ delay time	t_{CWD}	28		35		ns	18, 28
WRITE command to CAS\ lead time	t_{CWL}	8		10		ns	31
Data-in hold time	t_{DH}	8		10		ns	19, 29
Data-in setup time	t_{DS}	0		0		ns	19, 29
Output disable	t_{OD}	0	12	0	15	ns	24, 25
Output enable time	t_{OE}		12		15	ns	20
OE\ hold time from WE\ during READ-MODIFY-WRITE cycle	t_{OEH}	8		10		ns	25
OE\ HIGH hold time from CAS\ HIGH	t_{OEHC}	5		10		ns	
OE\ HIGH pulse width	t_{OEP}	5		5		ns	
OE\ LOW to CAS\ HIGH setup time.	t_{OES}	4		5		ns	
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	17, 24, 29
OE\ setup prior to RAS\ during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	

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AC ELECTRICAL CHARACTERISTICS (Continued)[5,6,7,8,9,10,11,12]

(V_{CC} = +3.3V ±0.3V)

DESCRIPTION		-5		-6			
	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	47		56		ns	34
Access time from RAS\	t_{RAC}		50		60	ns	
RAS\ to column-address delay time	t_{RAD}	9		12		ns	15
Row address hold time	t_{RAH}	7		10		ns	
RAS\ pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS\ pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000*	60	125,000*	ns	
RAS\ pulse width during Self Refresh	t_{RASS}	80		80		µs	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS\ to CAS\ delay time	t_{RCD}	11		14		ns	14, 28
READ command hold time (referenced to CAS\)	t_{RCH}	0		0		ns	16, 30
READ command setup time	t_{RCS}	0		0		ns	28
Refresh period	t_{REF}		64/24**		64/24**	ms	22, 23
Refresh period ("S" version)	t_{REF}		100		100	ms	23, 38
RAS\ precharge time	t_{RP}	30		40		ns	
RAS\ to CAS\ precharge time	t_{RPC}	5		5		ns	
RAS\ precharge time exiting Self Refresh	t_{RPS}	90		105		ns	
READ command hold time (referenced to RAS\)	t_{RRH}	0		0		ns	16
RAS\ hold time	t_{RSH}	13		15		ns	35
READ-WRITE cycle time	t_{RWC}	116		140		ns	
RAS\ to WE\ delay time	t_{RWD}	67		79		ns	18
WRITE command to RAS\ lead time	t_{RWL}	13		15		ns	
Transitioin time (rise or fall)	t_{T}	2	25	2	25	ns	
WRITE command hold time	t_{WCH}	8		10		ns	35
WRITE command hold time (referenced to RAS\)	t_{WCR}	38		45		ns	
WE\ command setup time	t_{WCS}	0		0		ns	18, 28
WE\ to outputs in High-Z	t_{WHZ}		12		15	ns	
WRITE command pulse width	t_{WP}	5		5		ns	
WE\ pulse widths to disable outputs	t_{WPZ}	10		10		ns	
WE\ hold time (CBR Refresh)	t_{WRH}	8		10		ns	
WE\ setup time (CBR Refresh)	t_{WRP}	8		10		ns	

NOTES:

*For XT Temp (-55°C to +125°C) tRASP (MAX) = 80,000ns for -5 and -6 speed.
**64ms Refresh for IT Temp, 24ms Refresh for XT Temp.

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NOTES:

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz; T_A = 25°C.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS\ refresh cycles (RAS\-ONLY or CBR with WE\ HIGH), before proper device operation is ensured. The eight RAS\ cycle wake-ups should be repeated any time the t_{REF} refresh requirements is exceeded.
7. AC characteristics assume t_T = 2.5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS\ and RAS\ = V_{IH}, data output is High-Z.
11. If CAS\ = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF; and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS\ is LOW at the falling edge of RAS\, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS\ must be pulsed HIGH for t_{CP}.
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With our without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA}, t_{RAC}, and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. t_{WCS}, t_{RWD}, t_{AWD}, and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. If $t_{WCS} > t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. t_{RWD}, t_{AWD}, and t_{CWD} define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE\ held HIGH and WE\ taken LOW after CAS\ goes LOW results in a LATE WRITE (OE\-controlled) cycle. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS\ leading edge in EARLY WRITE cycles and WE\ leading edge in LATE WRITE or READ-MODIFY-WRITE operations are not possible.
20. If OE\ is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE\ is LOW and OE\ is HIGH.
22. RAS\-ONLY REFRESH that all 4,096 rows of the device be refreshed at least once every 64ms.
23. CBR REFRESH for the device requires that at least 4,096 cycles be completed every 64ms.
24. The DQs go High-Z during READ cycles once t_{OD} or tOFF occur. If CAS\ stays LOW while OE\ is brought HIGH, the DQs will go High-Z. If OE\ is brought back LOW (CAS\ still LOW), the DQs will provide the previous read data.
25. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met (OE\ HIGH during write cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE\ is taken back LOW while CAS\ remains LOW, the DQs will remain open.
26. Column address changed once each cycle.
27. The first CAS\ edge to transition LOW.
28. Output parameter (DQx) is referenced to corresponding CAS\ input; DQ0 - DQ7 by CASL\ and DQ8 - DQ15 by CASH\.
29. Each CASx\ must meet minimum pulse width.
30. The last CASx\ edge to transition HIGH.
31. Last falling CASx\ edge to first rising CASx\ edge.
32. Last rising CASx\ edge to first falling CASx\ edge.
33. Last rising CASx\ edge to next cycles last rising CASx\ edge.
34. Last CASx\ to go LOW.

Notes continued on next page.

*64ms for IT version, 32ms for XT version.

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NOTES (Continued):

35. V_{IH} overshoot: V_{IH} (MAX) - V_{CC} + 2V for a pulse width £ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width £ 3ns, and the pulse width cannot be greater then one third of the cycle rate.
36. NC pins are assumed to be left floating and are not tested for leakage.
37. Self refresh and extended refresh for the device requires that at least 4,096 cycles be completed every 128ms.
38. Self refresh version on IT temp parts only.

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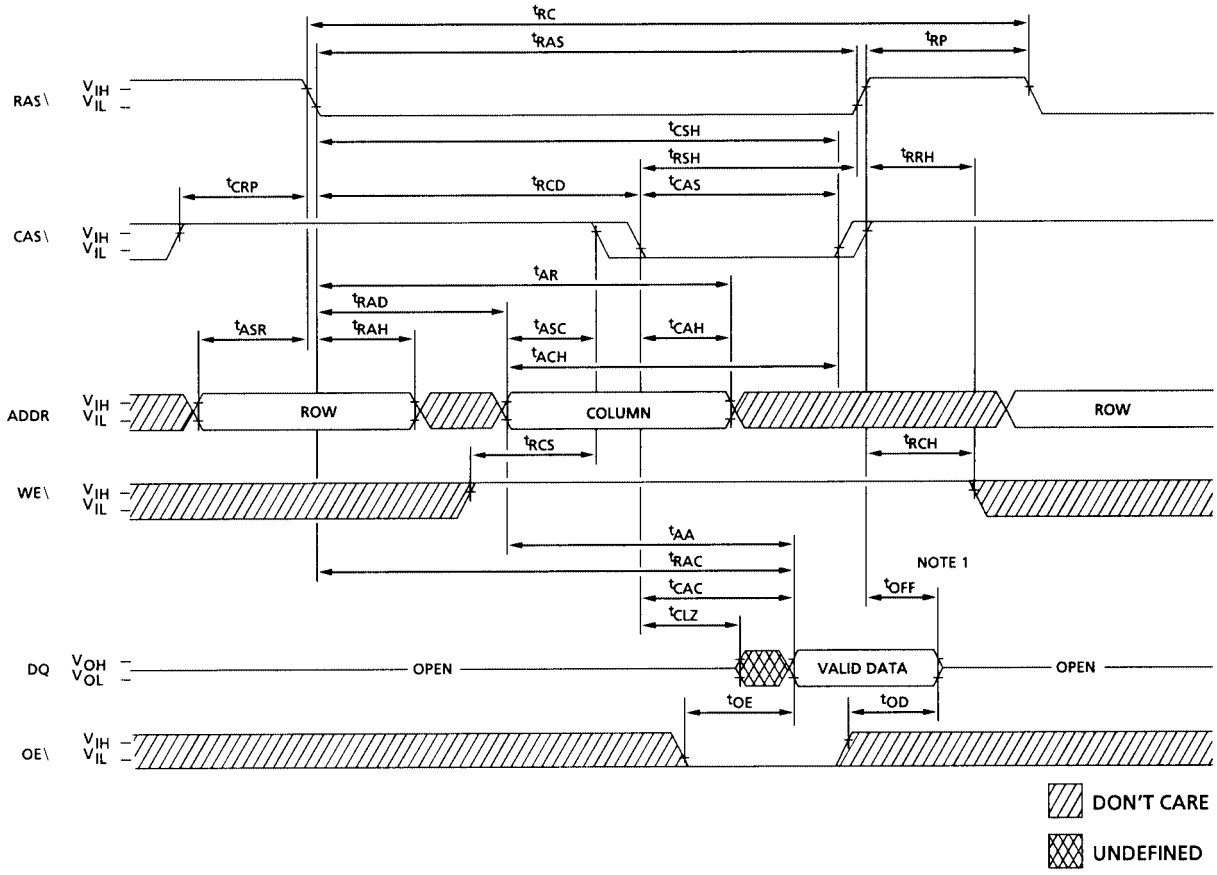
READ CYCLE



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

NOTES:

1. t_{OFF} is referenced from rising edge of RAS\ or CAS\, whichever occurs last.

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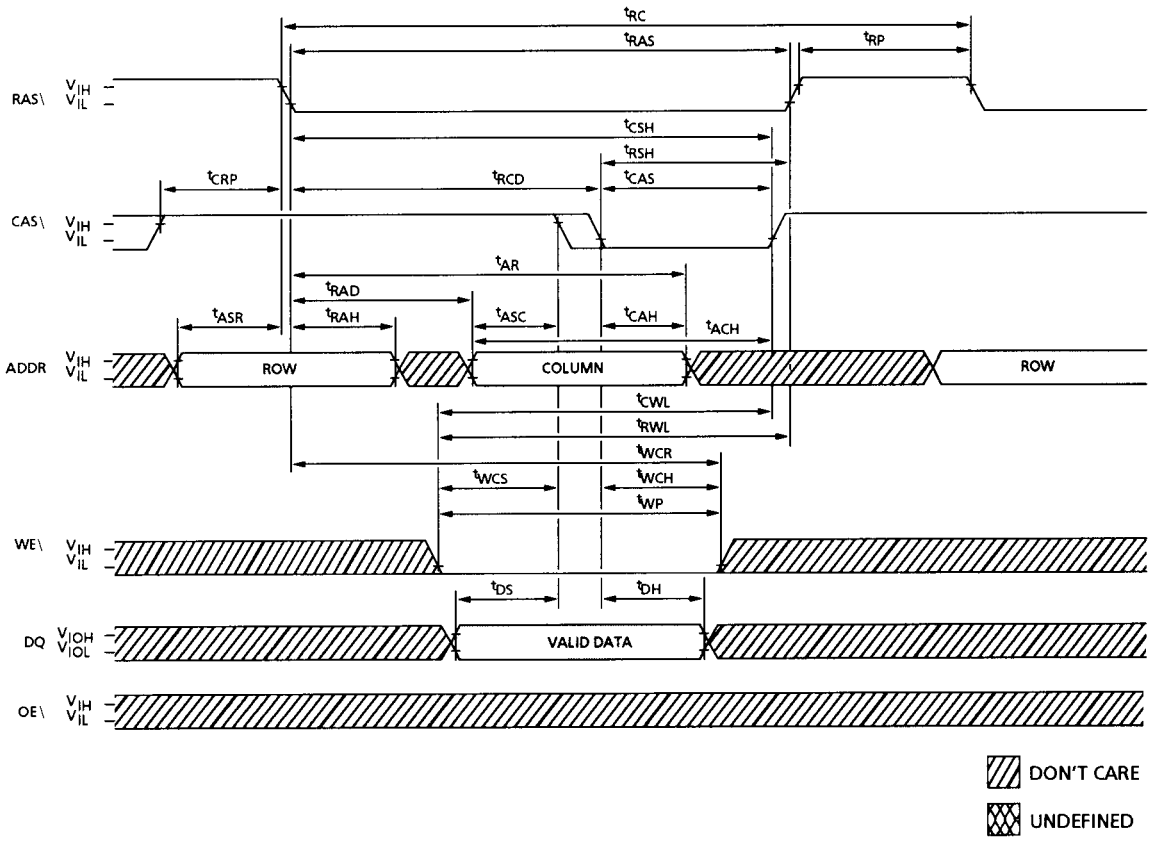
EARLY WRITE CYCLE



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAD	9		12		ns
tRAH	7		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

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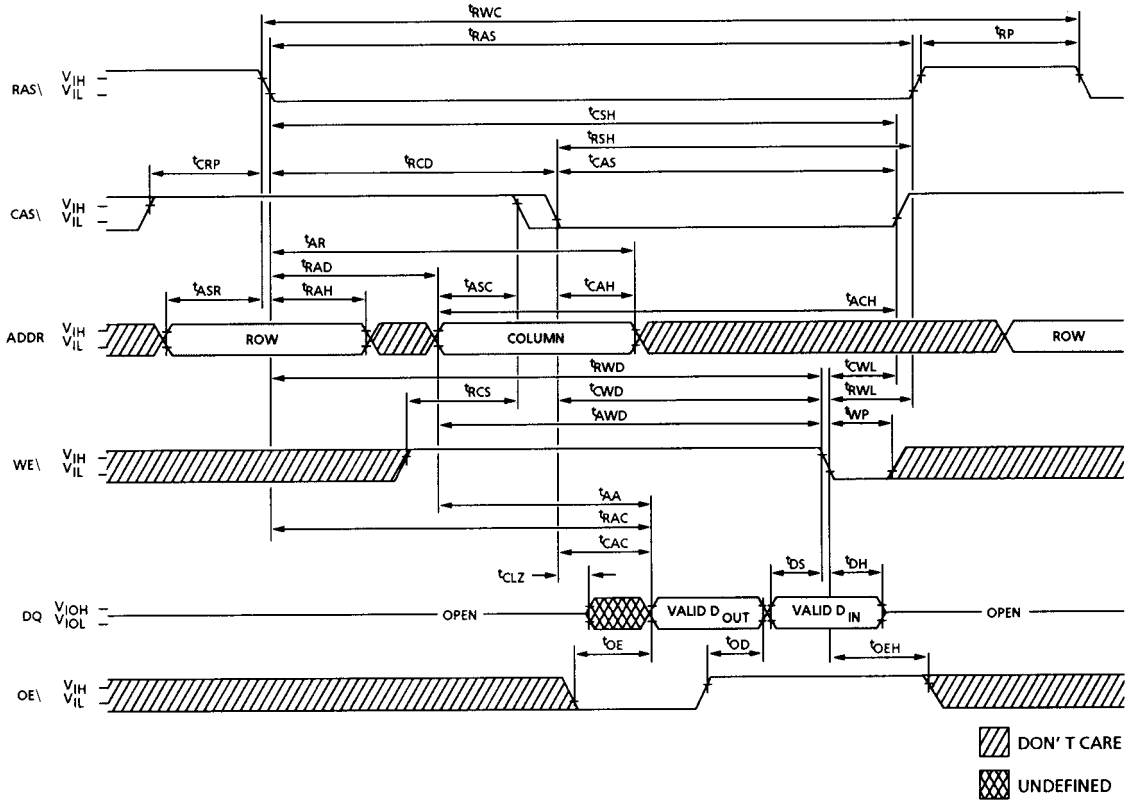
READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

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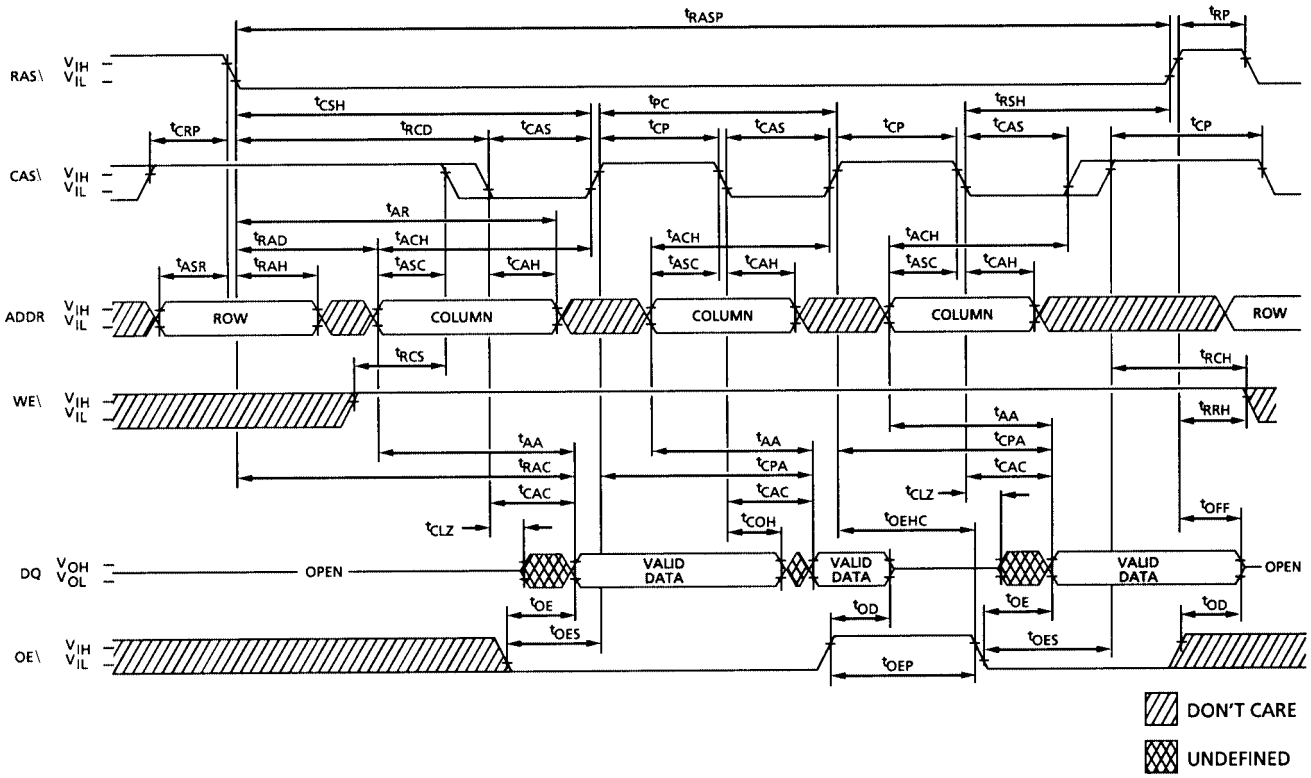
EDO-PAGE-MODE READ CYCLE



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRASP	50	125,000*	60	125,000*	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

NOTES:

* t_{RASP} (MAX) = 80,000ns for XT temperature version.

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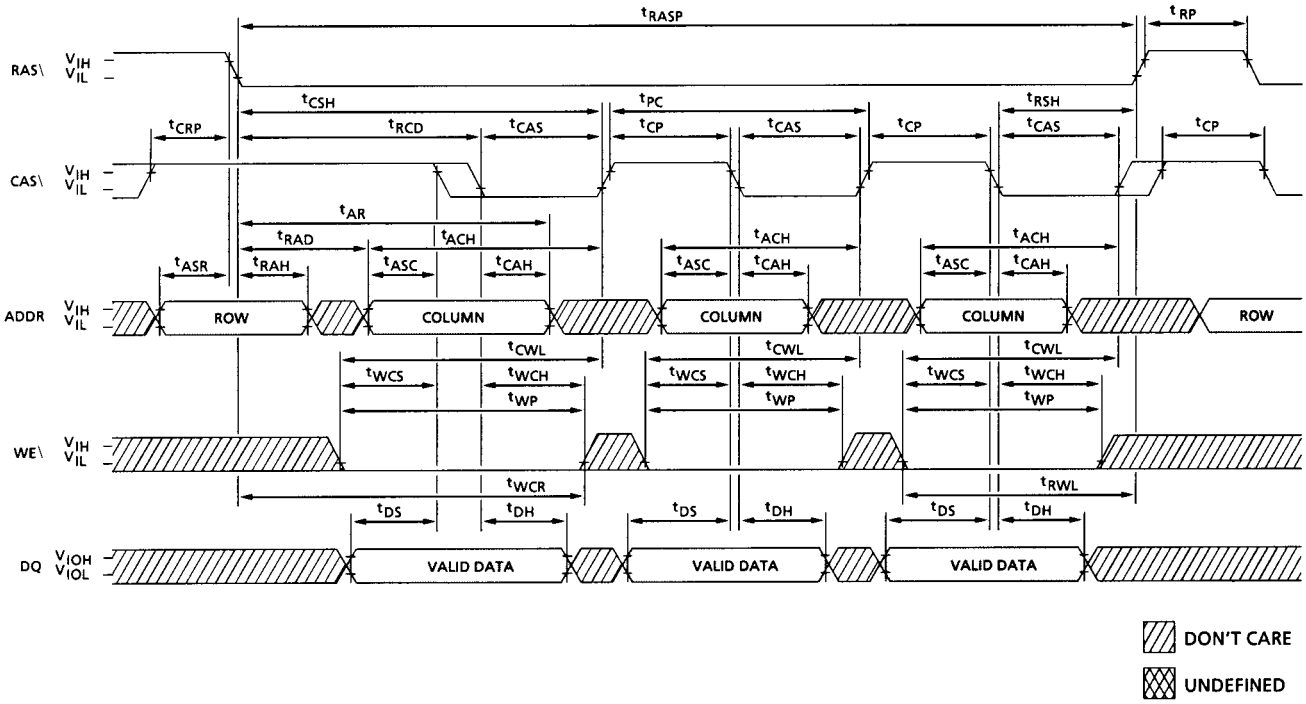
EDO-PAGE-MODE EARLY WRITE CYCLE



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC	20		25		ns
tRAD	9		12		ns
tRAH	7		10		ns
tRASP	50	125,000*	60	125,000*	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

NOTES:

* t_{RASP} (MAX) = 80,000ns for XT temperature version.

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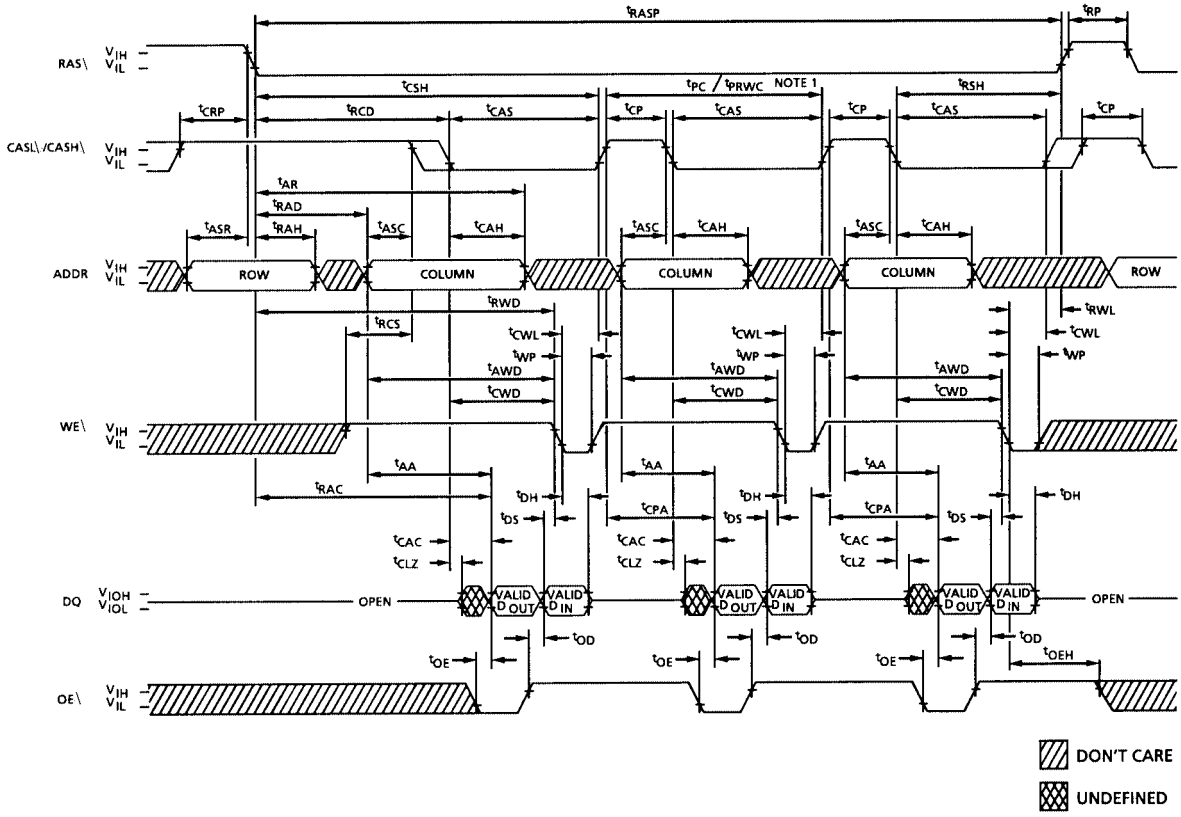
EDO-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tPC	20		25		ns
tPRWC	47		56		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRASP	50	125,000*	60	125,000*	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

NOTES:

* t_{RASP} (MAX) = 80,000ns for XT temperature version.

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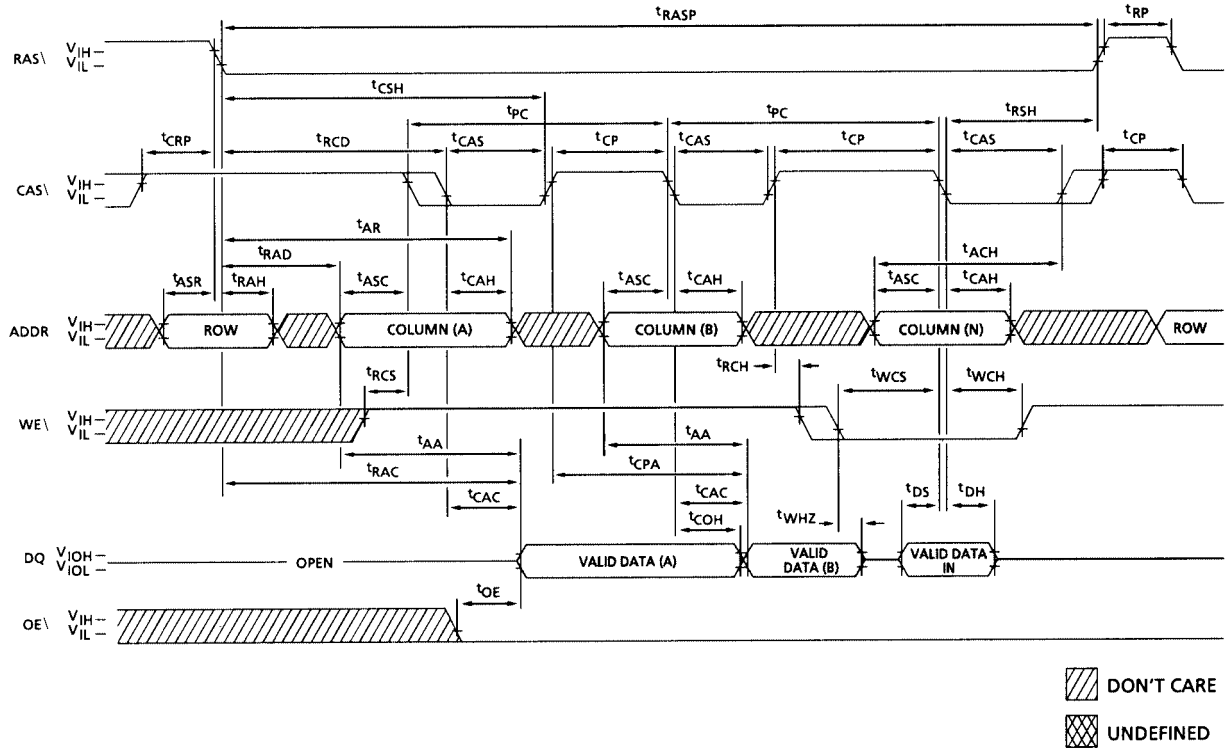
EDO-PAGE-MODE READ EARLY WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRASP	50	125,000*	60	125,000*	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ		12		15	ns

NOTES:

* t_{RASP} (MAX) = 80,000ns for XT temperature version.

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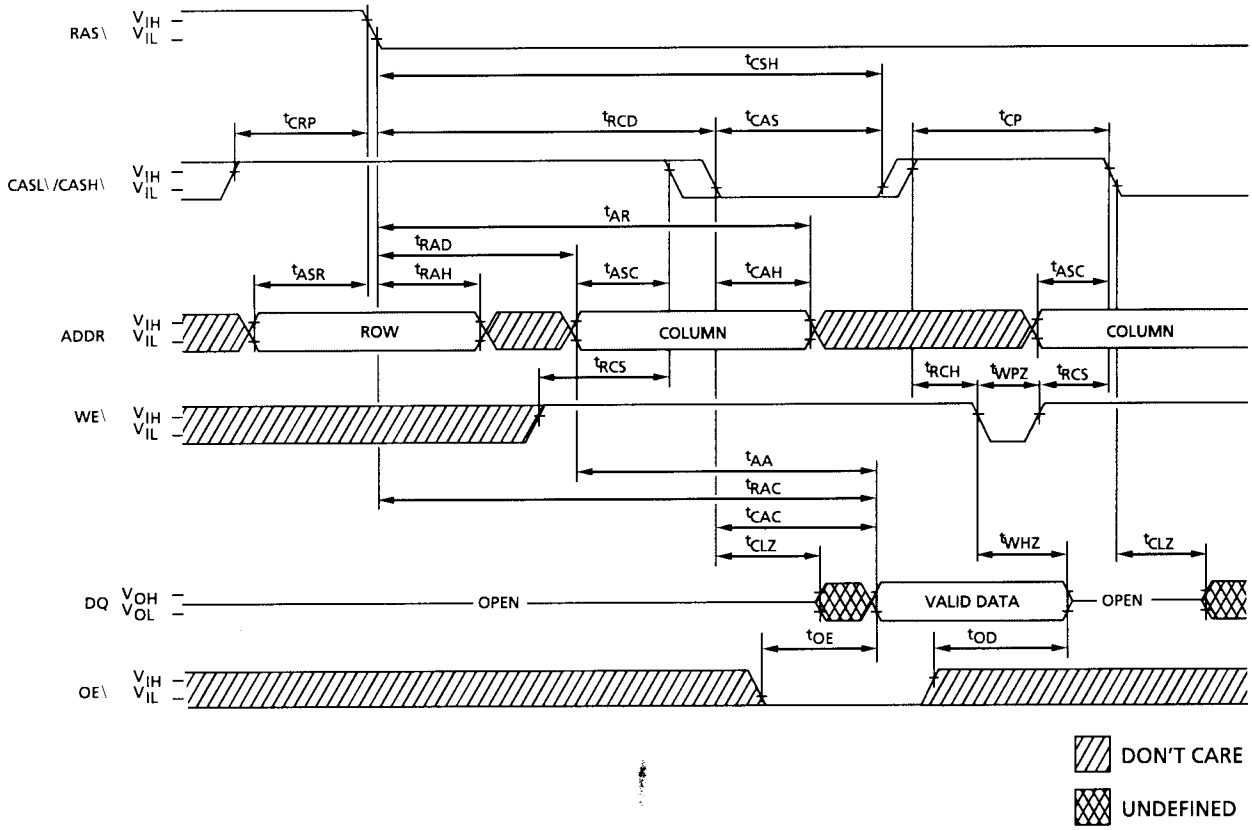
READ CYCLE
(with WE\-controlled disable)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ		12		15	ns
tWPZ	10		10		ns

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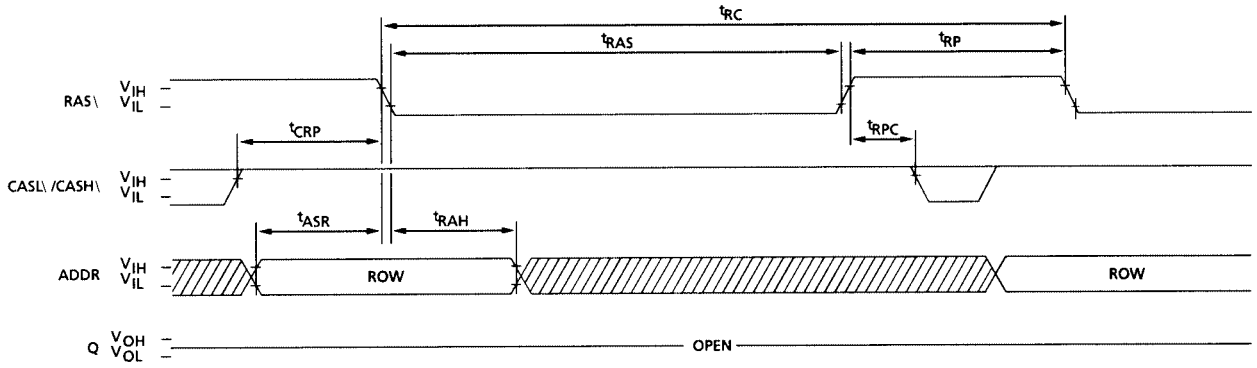
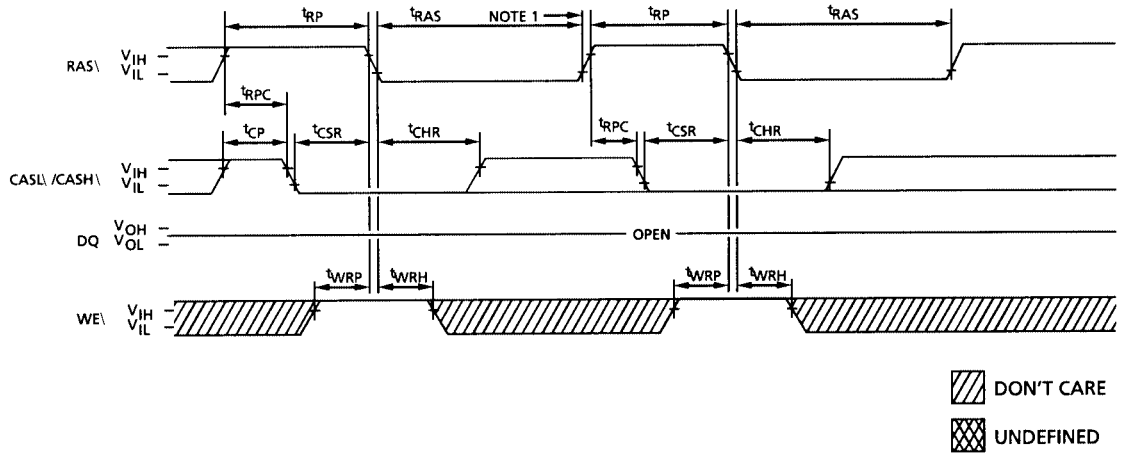
RAS\-ONLY REFRESH CYCLE

(OE\ and WE\ = DON'T CARE)



CBR REFRESH CYCLE

(Addresses and OE\ = DON'T CARE)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	7		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTES:

1. End of first CBR REFRESH cycle.

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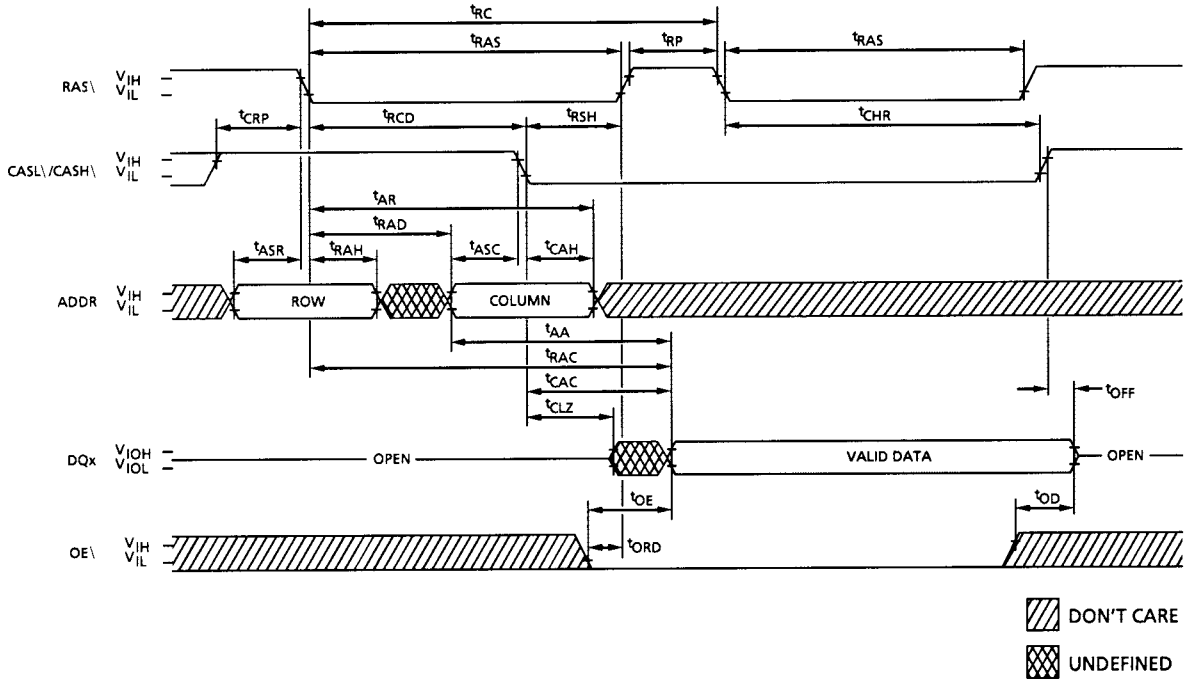
HIDDEN REFRESH CYCLE[1]

(WE\ = HIGH; OE\ = LOW)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	7		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

NOTES:

1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE\ is LOW and OE\ is HIGH.

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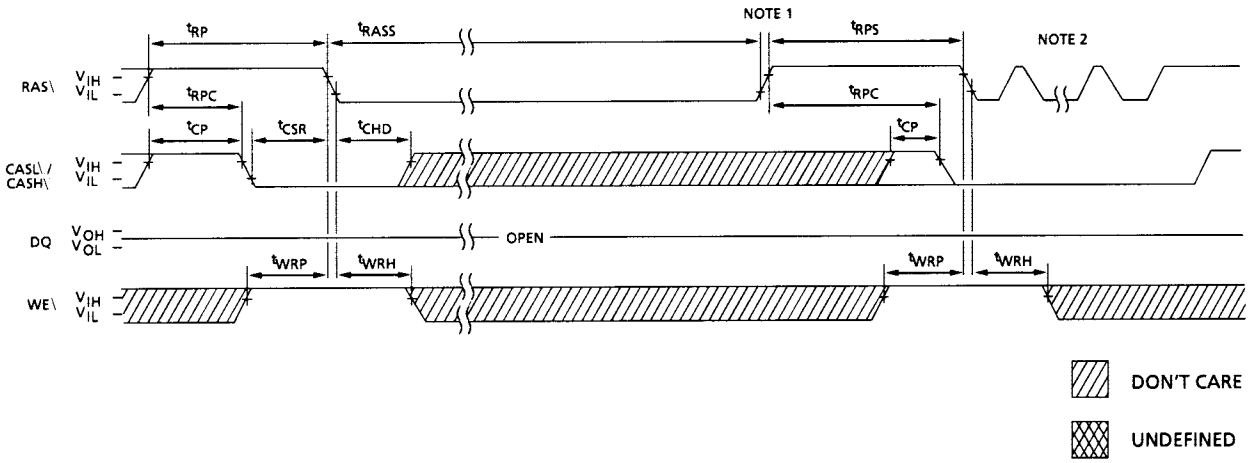
SELF REFRESH CYCLE

(Addresses and OE\ = DON'T CARE)



TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCHD	15		15		ns
tCLCH	5		5		ns
tCP	8		10		ns
tCSR	5		5		ns
tRASS	100		100		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRP	30		40		ns
tRPC	5		5		ns
tRPS	90		105		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTES:

1. Once t_{RASS} (MIN) is met and RAS\ remains LOW, the DRAM will enter self refresh mode.
2. Once t_{RPS} is satisfied, a complete burst of all rows should be executed if RAS\-only or burst CBR refresh is used.

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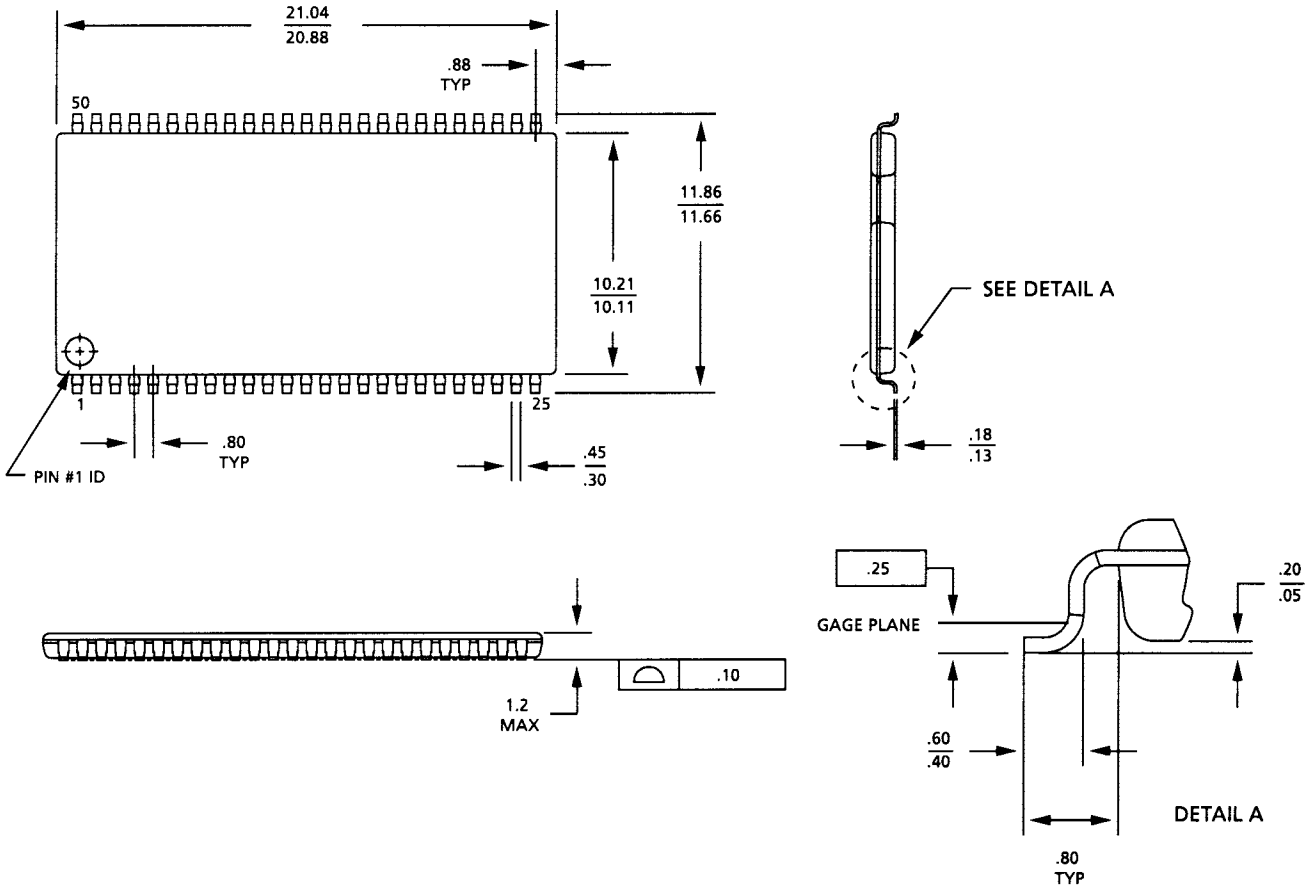
MECHANICAL DEFINITIONS

(Package Designator DG)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .25mm per side.

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ORDERING INFORMATION

EXAMPLE: AS4LC4M16DG-6S/XT

Device Number	Package Type	Speed ns	Options	Process
AS4LC4M16	DG	-5	S	/*
AS4LC4M16	DG	-6	S	/*

*AVAILABLE PROCESSES

XT = Industrial Temperature Range -55°C to +125°C
IT = Industrial Temperature Range -40°C to +85°C

OPTION DEFINITIONS

S = Self Refresh

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