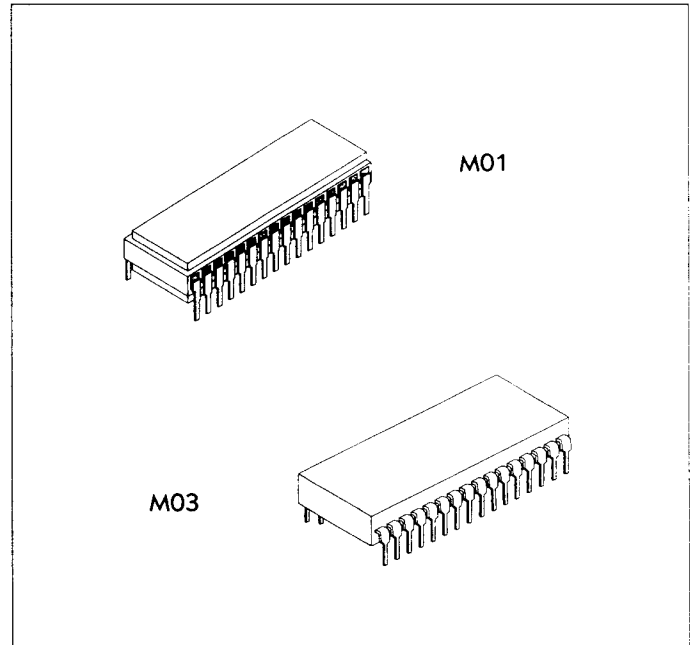


DESCRIPTION

The ELMO EMM02MS08 is a 262,144-word x 8-bit high speed BiCMOS static RAM module suitable for use in low power and high speed applications. It is available in several package and speed options, and operates from a single +5V supply.

FEATURES

- ❖ 262,144-word x 8-bit Organization
- ❖ Access Times of 55, 70 or 100ns
- ❖ Low Power Operation:
 - Standby: 15mW (Typ.)
 - Operating: 400mW (Typ.)
- ❖ Single +5V ($\pm 10\%$) Power Supply
- ❖ TTL Compatible Inputs and Outputs
- ❖ Fully Static Operation
- ❖ Available in MIL (-55 to +125°C) or Commercial (0 to +70°C) Temp. Range
- ❖ Available In:
 - 32 Pin 600-mil Sidebrazed DIP (JEDEC)
 - 32 Pin 600-mil Plastic DIP (JEDEC)



PACKAGE/SPEED OPTIONS

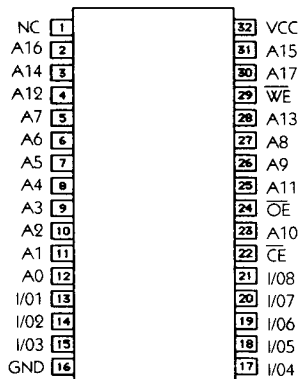
Package: 32 Pin 600-mil Sidebrazed DIP

Part Number	Speed
EMM02MS08M01 -055D	55ns
-070D	70ns
-100D	100ns

Package: 32 Pin 600-mil Plastic DIP

Part Number	Speed
EMM02MS08M03 -055C	55ns
-070C	70ns
-100C	100ns

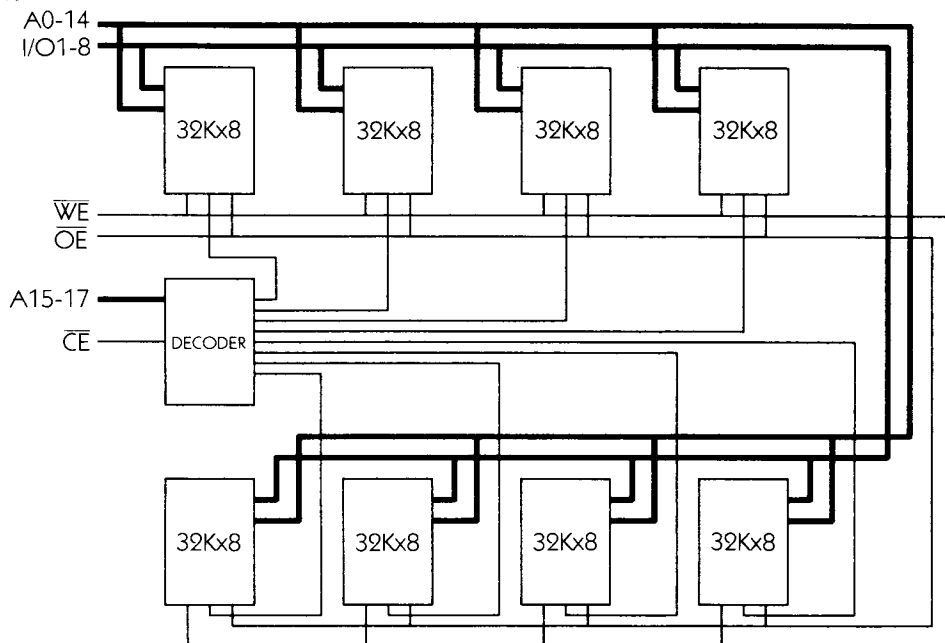
PIN CONFIGURATION



PIN NAMES

A0 to A17	Address Input
I/O1 to I/O8	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	+5V Power Supply
GND	Ground
NC	No Connect

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V _{cc}	-0.5 to +7.0	V
Input Voltage	V _{in}	-0.5 to V _{cc} +0.5	V
Input and Output Voltage	V _{i/o}	-0.5 to V _{cc} +0.5	V
Allowable Power Dissipation	P _d	1.0	W
Operating Temperature: Mil	T _{opr}	-55 to +125	°C
Comm.		0 to +70	°C
Storage Temperature	T _{stg}	-65 to +150	°C

TRUTH TABLE

CE	OE	WE	Mode	I/O1 TO I/O8	V _{cc} Current
H	X	X	Not Selected	High Z	ISB1, ISB2
L	H	H	Output Disable	High Z	ICC
L	L	H	Read	Data Out	ICC
L	X	L	Write	Data In	ICC

DC OPERATING CONDITIONS (T_a=T_{opr}.)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{cc}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2		V _{cc} +0.3	V
Input Low Voltage	V _{IL}	-0.3		0.8	V

DC OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = T_{opr.}$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	ILL	$V_{IN} = GND$ or V_{CC}	-10		10	μA
Output Leakage Current	IOL	$V_{I/O} = GND$ or V_{CC} , $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-10		10	μA
Average Operating Current	ICC	Min Cycle, $I_{out} = 0mA$		80	150	mA
Standby Current	ISB1	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		3	20	mA
	ISB2	$\overline{CE} = V_{IH}$, $V_{IN} = V_{IL}$ or V_{IH}			30	mA
Output High Voltage	VOH	$I_{OH} = -4.0mA$	2.4			V
Output Low Voltage	VOL	$I_{OL} = 8.0mA$			0.4	V

I/O CAPACITANCE ($T_a = 25^\circ C$, $f = 1MHz$)

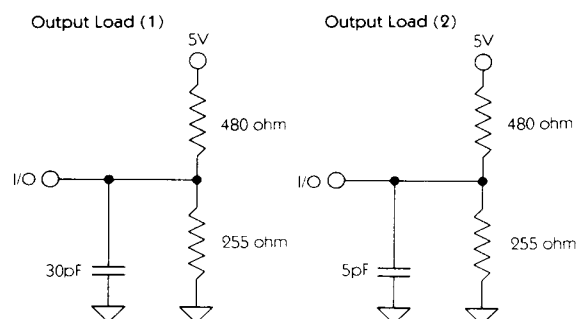
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	CIN	$V_{IN} = 0V$		65	80	pF
I/O Capacitance	CI/O	$V_{I/O} = 0V$		70	85	pF

Note) This parameter is sampled and is not 100% tested.

AC CHARACTERISTICS

AC test conditions ($V_{CC} = 5V \pm 10\%$, $T_a = T_{opr.}$)

Item	Condition
Input Pulse High Level	$V_{IH} = 3.0V$
Input Pulse Low Level	$V_{IL} = 0V$
Input Pulse Rise Time	$t_r = 5ns$
Input Pulse Fall Time	$t_f = 5ns$
Input and Output Timing Reference Level	1.5V
Output load	Fig.1



Note: Load capacitance includes scope and jig capacitances

Figure1

READ CYCLE

Item	Symbol	-55 Min.	Max.	-70 Min.	Max.	-100 Min.	Max.	Unit
Read Cycle Time	TAVAV	55		70		100		ns
Address Access Time	TAVQV		55		70		100	ns
Chip Enable Access Time	TELQV		55		70		100	ns
Output Enable to Output Valid	TGLQV		30		35		50	ns
Chip Enable to Output in High Z (1)	TEHQZ		25		30		35	ns
Chip Enable to Output in Low Z (1)	TELQX	25		30		35		ns
Enable to Output in High Z (1)	TGHQZ		25		30		35	ns
Enable to Output in Low Z (1)	TGLQX	5		5		5		ns
Output Hold from Address Change	TAVQX	5		5		15		ns

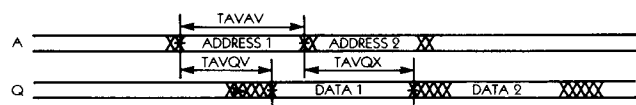
WRITE CYCLE

Item	Symbol	-55 Min.	Max.	-70 Min.	Max.	-100 Min.	Max.	Unit
Write Cycle Time	TAVAV	55		70		100		ns
Address Valid to End of Write	TAVWH	50		60		70		ns
Chip Enable to End of Write	TELWH	50		65		70		ns
	TWLEH	50		65		70		ns
Data to Write Time Overlap	TDVWH	25		30		35		ns
	TDVEH	25		30		35		ns
Data Hold Time from Write	TWHDX	0		0		0		ns
	TEHDX	10		15		20		ns
Write Pulse Width	TWLWH	40		55		60		ns
	TELEH	40		55		60		ns
Address Set-UpTime	TAVWL	20		20		20		ns
	TAVEL	0		0		0		ns
Write Recovery Time	TWHAX	5		5		5		ns
	TEHAX	5		5		5		ns
Write to Output in High Z (1)	TWLQZ		25		30		35	ns
Output Active from End of Write (1)	TWHQX	0		0		0		ns

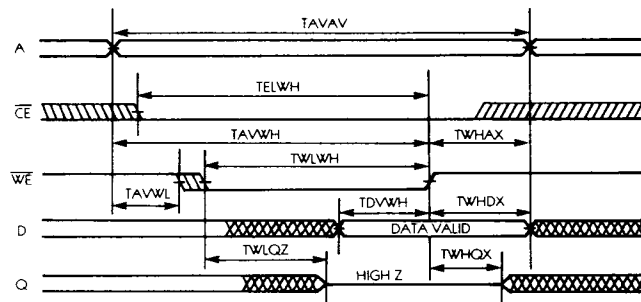
Note 1: Parameters tested on a sample basis only.

TIMING WAVEFORM

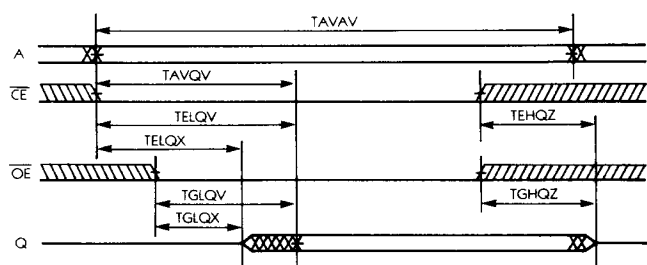
❖ Read Cycle (1): $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



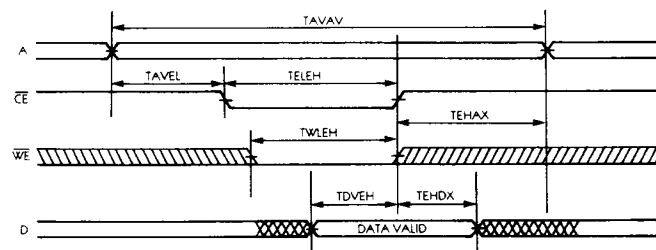
❖ Write Cycle (1): $\overline{WE}$ control



❖ Read cycle (2): $\overline{WE}=V_{IH}$

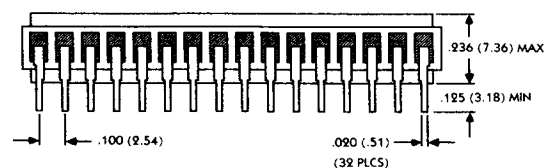
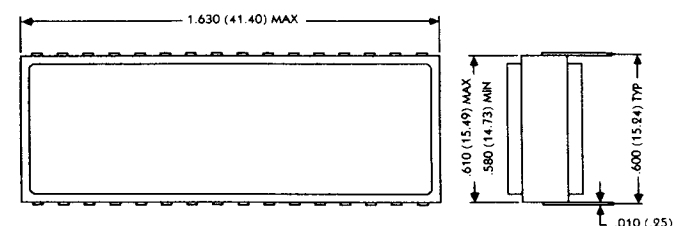


❖ Write Cycle (2): $\overline{CE}$ control

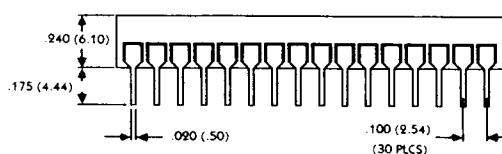
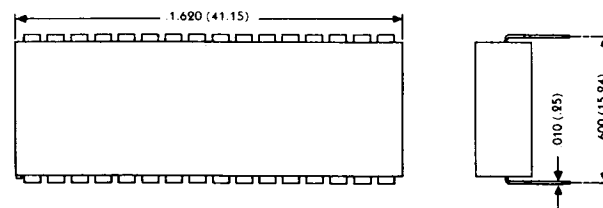


PACKAGE OUTLINE

Dimensions in Inches (Millimeters)



Package Type MO1, 32 Lead .600" Sidebrazed DIP



Package Type M03, 32 lead .600" Plastic DIP

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