THOMSON SEMICONDUCTEURS

ETC9420/21/22 • ETC9320/21/22
ETC9444/45 • ETC9344/45

SINGLE CHIP MICROCONTROLLERS

he ETC 9420, C 9421, C 9422, C 9320, C 9321, C 9322, and ETC 9445, C 344, C 9345 fully static single-chip CMOS microcontrollers are fully compable with the COPS® family, fabricated using double-poly, silicon gate omplementary MOS technology. These Controller Oriented Processors are omplete microcontrollers containing all system timing, internal logic, ROM, AM and I/O necessary to implement dedicated control functions in a variety f applications.

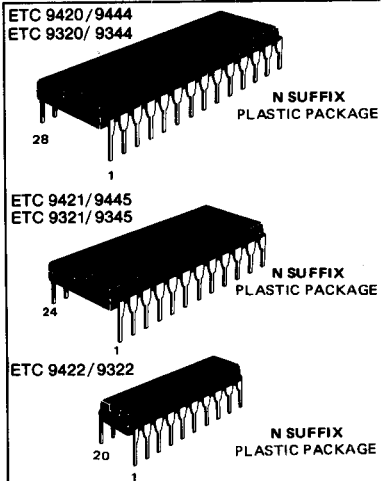eatures include single supply operation, a variety of output configuration ptions, with an instruction set, internal architecture and I/O scheme designed facilitate keyboard input, display output and BCD data manipulation. The TC 9420, C 9444 are 28-pin chips. The ETC 9421, C 9445 are 24-pin versions 4 inputs removed) and C 9422 is a 20-pin version with 15 I/O lines. Standard test procedures and reliable high-density fabrication techniques rovide the medium to large volume customers with a customized microcon-roller at a low end -product cost.

These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

- Lowest power dissipation (50 µW typical).
- Power saving IDLE state and HALT mode.
- Fully Static (can turn off the clock).
- 2 K x 8 ROM, 128 x 4 RAM (ETC 9444, C 9445).
- 1 K x 8 ROM, 64 x 4 RAM (ETC 9420, C 9421, C 9422).
- True vectored interrupt, plus restart.
- 3-level subroutine stack.
- 4 µsec intruction time, plus software selectable clocks.
- 23 I/O lines (ETC 9444, C 9420).
- Single supply operation (2.4 V to 5.5 V).
- Programmable read/write 8-bit timer/event counter.
- Internal binary counter register with MICROWIRE® serial I/O Capability.
- General purpose and tri-state® outputs.
- LSTTL/C MOS compatible.
- MICROBUS® compatible.
- Software/hardware compatible with other members of ET 9400 family.
- Extended temperature range devices ETC 9320/ETC 9321, ETC 9322 and ETC 9344/ETC 9345 (— 40° C to +85°C).
- Military devices (—55°C to +125°C) to be available.

CMOS

SINGLE CHIP MICROCONTROLLERS

ETC 9420/9444
ETC 9320/ 9344

N SUFFIX
PLASTIC PACKAGE

28
1

ETC 9421/9445
ETC 9321/9345

N SUFFIX
PLASTIC PACKAGE

24
1

ETC 9422/9322

N SUFFIX
PLASTIC PACKAGE

20
1

PIN ASSIGNMENTS
(See page 7)

GND	1	28	D0
CKO	2	27	D1
CKI	3	26	D2
RESET	4	25	D3
L7	5	24	G3
L6	6	23	G2
L5	7	22	G1
L4	8	21	G0
IN1	9	20	IN3
IN2	10	19	IN0
Vcc	11	18	SK
L3	12	17	SO
L2	13	16	SI
L1	14	15	L0

ETC 9420
ETC 9444
ETC 9320
ETC 9344

Ref. 00530-R1
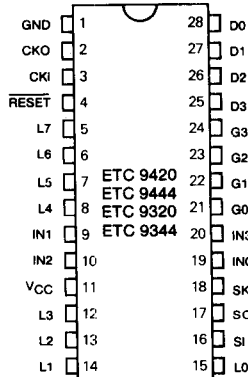
FIGURE 1 — BLOCK DIAGRAM (28-pin version)

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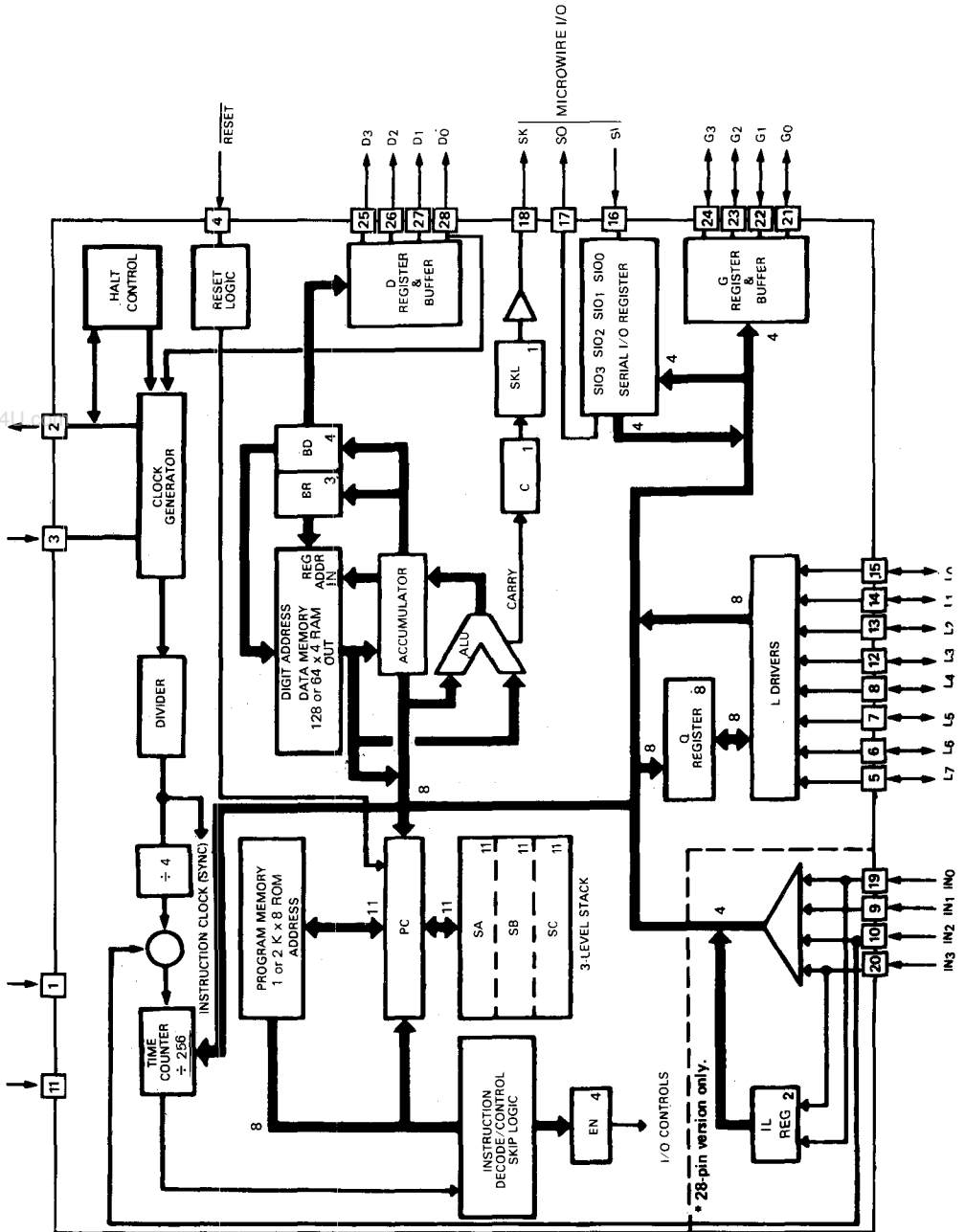
ETC 9420, ETC 9421, ETC 9422 ● ETC 9444, ETC 9445

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Vcc)	6 V
Voltage at any pin	−0.3 V to V_{CC} + 0.3 V
Total Allowable Source current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0° C to + 70° C
Storage Temperature Range	−65° C to + 150° C
Lead Temperature (soldering 10 seconds)	300° C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are note insured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +70°C(Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Note 5)	Peak to Peak	−	0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 2.4 V, tc = 64 μs	−	120	μA
	V_{CC} = 5.0 V, tc = 16 μs	−	700	μA
	V_{CC} = 5.0 V, tc = 4 μs	−	3000	μA
	(tc = instruction cycle time)			
Halt Mode Current (Note 2)	V_{CC} = 5.0 V, Fin = 0 kHz	−	40	μA
	V_{CC} = 2.4 V, Fin = 0 kHz	−	12	μA
Input Voltage levels				
RESET CKI (RC or crystal opt.)				
Do (Clock input)				
Logic High		0.9 V_{CC}	−	V
Logic Low			0.1 V_{CC}	V
All other inputs				
Logic High		0.7 V_{CC}	−	V
Logic Low		−	0.2 V_{CC}	V
Input Pull-up current	V_{CC} = 4.5 V, V_{IN} = 0	30	330	μA
HI-Z input leakage		−1	+1	μA
Input capacitance (Note 4)		−	7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0 V ± 5 %			
Logic High	I_{OH} = −100 μA	2.7	−	V
Logic Low	I_{OL} = 400 μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC}−0.2	−	V
Logic Low	I_{OL} = 10 μA		0.2	V
Output current Level (except CKO)				
Sink (Note 6)	V_{CC} = 4.5 V, Vout = V_{CC}	1.2	−	mA
	V_{CC} = 2.4 V, Vout = V_{CC}	0.2	−	mA
Source (standard option)	V_{CC} = 4.5 V, Vout = 0V	0.5	−	mA
	V_{CC} = 2.4 V, Vout = 0V	0.1	−	mA
Source (Low current option)	V_{CC} = 4.5 V, Vout = 0V	30	330	μA
	V_{CC} = 2.4 V, Vout = 0V	6	80	μA
CKO Current level (As clock out)				
Sink ÷ 4	V_{CC} = 4.5 V, CKI = V_{CC} V_{OUT} = V_{CC}	0.3	−	mA
÷ 8		0.6	−	mA
÷ 16		1.2	−	mA
Source ÷ 4	V_{CC} = 4.5 V, CKI = 0V, V_{OUT} = 0V	0.3	−	mA
÷ 8		0.6	−	mA
÷ 16		1.2	−	mA
Allowable Sink Source current per pin (Note 6)		−	5	mA
Allowable loading on CKO (as HALT)		−	100	pF
Current needed to over-ride HALT (Note 3)				
To continue	V_{CC} = 4.5 V, Vin = 0.2 V_{CC}	−	0.7	mA
To halt	V_{CC} = 4.5 V, Vin = 0.7 V_{CC}	−	1.6	mA
TRI-STATE or open drain Leakage current		−2.5	+ 2.5	μA

3/22

AC ELECTRICAL CHARACTERISTICS 0°C ≤ T$_A$ ≤ +70°C (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Instruction cycle time (tc)	V$_{CC}$≥ 4.5 V	4	DC	μs
	4.5 V > V$_{CC}$ ≥ 2.4 V	16	DC	μs
Operating CKI Frequency				
÷ 4 mode		DC	1.0	MHz
÷ 8 mode	V$_{CC}$≥ 4.5 V	DC	2.0	MHz
÷ 16 mode		DC	4.0	MHz
÷ 4 mode		DC	250	kHZ
÷ 8 mode	4.5 V > V$_{CC}$ ≥ 2.4 V	DC	500	kHZ
÷ 16 mode		DC	1.0	MHz
Duty cycle (Note 4)	F1 = 4 MHz	40	60	%
Rise time (Note 4)	F1 = 4 MHz ext. dock	–	60	ns
Fall time (Note 4)	F1 = 4 MHz ext. dock	–	40	ns
Instruction cycle time (RC oscillator) (Note 4)	R = 30 K V$_{CC}$ = 5 V C = 82 pF, (÷ 4 Mode)	8	16	μs
INPUTS (fig. 3)				
t$_{SETUP}$	G inputs	tc/4 +.7	–	μs
	SI input V$_{CC}$≥ 4.5 V	0.3	–	μs
	All others	1.7	–	μs
t$_{HOLD}$	V$_{CC}$≥ 4.5 V	0.25	–	μs
	4.5 V > V$_{CC}$ ≥ 2.4 V	1.0	–	μs
OUTPUT PROPAGATION DELAY	Vout = 1.5 V, CL = 100 pF, R$_L$ = 5 K			
t$_{PD1}$, t$_{PD0}$	V$_{CC}$≥ 4.5 V	–	1.0	μs
t$_{PD1}$, t$_{PD0}$	4.5 V > V$_{CC}$ ≥ 2.4 V	–	4.0	μs
MICROBUS® TIMING	C$_L$ = 50 pF, V$_{CC}$ = 5 V ± 5 %			μs
Read operation (fig. 4)				
Chip select stable before RD - t$_{CSR}$		65	–	ns
Chip select hold time for RD - t$_{RCS}$		20	–	ns
RD pulse width - t$_{RR}$		400	–	ns
Data delay from RD - t$_{RD}$		–	375	ns
RD to data floating - t$_{DF}$ (note 4)		–	250	ns
Write operation (fig. 5)				
Chip select stable before WR - t$_{CSW}$		65	–	ns
Chip select hold time for WR - t$_{WCS}$		20	–	ns
WR pulse width - t$_{WW}$		400	–	ns
Data set-up time for WR - t$_{DW}$		320	–	ns
Data hold time for WR - t$_{WD}$		100	–	ns
INTR transition time for WR - t$_{WI}$		–	700	ns

Note 1 : Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V$_{CC}$ with 20k resistors. See current drain equation on page 17.

Note 2 : The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions : all inputs tied to V$_{CC}$, L lines in TRI-STATE mode and tied to ground, all output low and tied to ground.

Note 3 : When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4 : This parameter is only sampled and not 100 % tested.

Note 5 : Voltage change must be less than 0.5 volt in a 1 ms period.

Note 6 : SO output sink current must be limited to keep V$_{OL}$ below 0.2 V$_{CC}$ when port is running in order to prevent entering test mode.

THOMSON SEMICONDUCTEURS

TC9320 , ETC9321 , ETC9322 ● ETC9344 , ETC9345

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 V
Voltage at any pin	−0.3 V to V_{CC} + 0.3 V
Total Allowable Source current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	−40° C to + 85° C
Storage Temperature Range	−65° C to + 150° C
Lead Temperature (soldering 10 seconds)	300° C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are note insured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS — 40° C ≤ T_A ≤ + 85° C (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Operating Voltage		3.0	5.3	V
Power Supply Ripple (Note 5)	Peak to Peak	−	0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC}=3.0 V, tc=64 µs	−	180	µA
	V_{CC}=5.0 V, tc=16 µs	−	800	µA
	V_{CC}=5.0 V, tc= 4 µs (tc = instruction cycle time)	−	3600	µA
Halt Mode Current (Note 2)	V_{CC}=5.0 V, Fin=0 kHz	−	60	µA
	V_{CC}=3.0 V, Fin=0 kHz	−	30	µA
Input Voltage levels				
RESET CKI (RC or crystal opt.)				
Do (Clock input)				
Logic High		0.9 V_{CC}	−	V
Logic Low		−	0.1 V_{CC}	V
All other inputs				
Logic High		0.7	−	
Logic Low		−	0.2 V_{CC}	V
Input Pull-up current	V_{CC}=4.5 V, V_{IN}=0	30	440	µA
HI-Z input leakage		−2	+2	µA
Input capacitance (Note 4)		−	7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC}=5.0 V ± 5 %			
Logic High	I_{OH} = −100 µA	2.7	−	V
Logic Low	I_{OL} = 400 µA	−	0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 µA	V_{CC}−0.2	−	V
Logic Low	I_{OL} = 10 µA	−	0.2	V
Output current Level (except CKO)				
Sink (Note 6)	V_{CC}=4.5 V, Vout=V_{CC}	1.2	−	mA
	V_{CC}=3.0 V, Vout=V_{CC}	0.2	−	mA
Source (standard option)	V_{CC}=4.5 V, Vout=0V	0.5	−	mA
	V_{CC}=3.0 V, Vout=0V	0.1	−	mA
Source (Low current option)	V_{CC}=4.5 V, Vout=0V	30	440	µA
	V_{CC}=3.0 V, Vout=0V	8	200	µA
CKO Current level (As clock out)				
Sink ÷ 4		0.3	−	mA
÷ 8	V_{CC}=4.5 V, CKI=V_{CC}, Vout=V_{CC}	0.6	−	mA
÷ 16		1.2	−	mA
Source ÷ 4		0.3	−	mA
÷ 8	V_{CC}=4.5 V, CKI=0V, Vout=0V	0.6	−	mA
÷ 16		1.2	−	mA
Allowable Sink / Source current per pin (Note 6)		−	5	mA
Allowable loading on CKO (as HALT)		−	100	pF
Current needed to over-ride HALT (Note 3)				
To continue	V_{CC}=4.5 V, Vin=0.2 V_{CC}	−	0.9	mA
To halt	V_{CC}=4.5 V, Vin=0.7 V_{CC}	−	2.1	mA
TRI-STATE or open drain Leakage current		−5	+5	µA

5/22

THOMSON SEMICONDUCTEURS

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AC ELECTRICAL CHARACTERISTICS – -40°C < T$_A$ < + 85°C (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Instruction cycle time (tc)	V$_{CC}$ ≥ 4.5 V	4	DC	μs
	4.5 V > V$_{CC}$ ≥ 3.0 V	16	DC	μs
Operating CKI Frequency				
÷ 4 mode		DC	1.0	MHz
÷ 8 mode	V$_{CC}$ ≥ 4.5 V	DC	2.0	MHz
÷ 16 mode		DC	4.0	MHz
÷ 4 mode		DC	250	kHZ
÷ 8 mode	4.5 V > V$_{CC}$ ≥ 3.0 V	DC	500	kHZ
÷ 16 mode		DC	1.0	MHz
Duty cycle (Note 4)	F1 = 4 MHz	40	60	%
Rise time (Note 4)	F1 = 4 MHz ext. clock	–	60	ns
Fall time (Note 4)	F1 = 4 MHz ext. clock	–	40	ns
Instruction cycle time (RC oscillator) (Note 4)	R = 30 K, V$_{CC}$ = 5 V C = 82 pF, (÷ 4 Mode)	8	16	μs
INPUTS (fig. 3)				
t$_{SETUP}$	G inputs	(tc/4) + .7	–	μs
	SI input ⎰ V$_{CC}$ ≥ 4.5 V	0.3	–	μs
	All others	1.7	–	μs
t$_{HOLD}$	V$_{CC}$ ≥ 4.5 V	0.25	–	μs
	4.5 V > V$_{CC}$ ≥ 3.0 V	1.0	–	μs
OUTPUT				
PROPAGATION DELAY	Vout = 1.5 V, CL = 100 pF, RL = 5k			
tpD1 , tpD0	V$_{CC}$ ≥ 4.5 V	–	1.0	μs
tpD1 , tpD0	4.5 V > V$_{CC}$ ≥ 3.0 V	–	4.0	μs
MICROBUS® TIMING	C$_L$ = 50 pF, V$_{CC}$ = 5 V ± 5 %			
Read operation (fig. 4)				
Chip select stable before RD - t$_{CSR}$		65	–	ns
Chip select hold tome for RD - t$_{RCS}$		20	–	ns
RD pulse width - t$_{RR}$		400	–	ns
Data delay from RD - t$_{RD}$		–	375	ns
RD to data floating - t$_{DF}$(note 4)		–	250	ns
Write operation (fig. 5)				
Chip select stable before WR - t$_{CSW}$		65	–	ns
Chip select hold time for WR - t$_{WCS}$		20	–	ns
WR pulse width - t$_{WW}$		400	–	ns
Data set-up time for WR - t$_{DW}$		320	–	ns
Data hold time for WR - t$_{WD}$		100	–	ns
INTR transition time for WR - t$_{WI}$		–	700	ns

Note 1 : Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V$_{CC}$ with 20k resistors. See current drain equation on page 17

Note 2 : The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions : all inputs tied to V$_{CC}$, L lines in TRI-STATE mode and tied to ground, all output low and tied to ground.

Note 3 : When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.
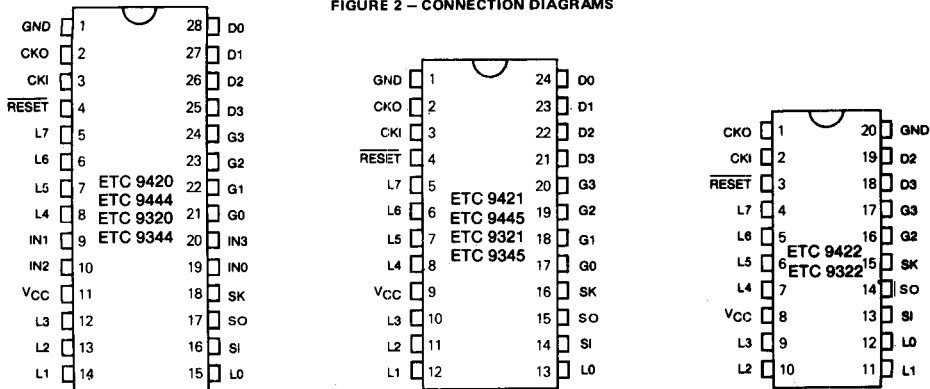
Note 4 : This parameter is only sampled and not 100 % tested.

Note 5 : Voltage change must be less than 0.5 volt in a 1 ms period.

Note 6 : SO output sink current must be limited to keep V$_{OL}$ below 0.2 V$_{CC}$ when port is running in order to prevent entering test mode.

6/22

THOMSON SEMICONDUCTEURS

FIGURE 2 – CONNECTION DIAGRAMS

ETC 9420 / ETC 9444 / ETC 9320 / ETC 9344 (28-pin)

Pin	Signal		Pin	Signal
1	GND		28	D0
2	CKO		27	D1
3	CKI		26	D2
4	RESET		25	D3
5	L7		24	G3
6	L6		23	G2
7	L5		22	G1
8	L4		21	G0
9	IN1		20	IN3
10	IN2		19	IN0
11	Vcc		18	SK
12	L3		17	SO
13	L2		16	SI
14	L1		15	L0

ETC 9421 / ETC 9445 / ETC 9321 / ETC 9345 (24-pin)

Pin	Signal		Pin	Signal
1	GND		24	D0
2	CKO		23	D1
3	CKI		22	D2
4	RESET		21	D3
5	L7		20	G3
6	L6		19	G2
7	L5		18	G1
8	L4		17	G0
9	Vcc		16	SK
10	L3		15	SO
11	L2		14	SI
12	L1		13	L0

ETC 9422 / ETC 9322 (20-pin)

Pin	Signal		Pin	Signal
1	CKO		20	GND
2	CKI		19	D2
3	RESET		18	D3
4	L7		17	G3
5	L6		16	G2
6	L5		15	SK
7	L4		14	SO
8	Vcc		13	SI
9	L3		12	L0
10	L2		11	L1

L_7-L_0	8 bit bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bit bidirectional I/O ports
D_3-D_1	3 bit general purpose outputs
D_0	General purpose output or oscillator input
IN_3-IN_0	4-bit input port (ETC 9420 or 9444 only)
SI	Serial input
SO	Serial output
SK	Logic-controlled clock or general purpose output
CKI	System oscillator input
CKO	System oscillator output (or general purpose Input or Halt I/O Port)
RESET	System reset input
V_{CC}	Power supply
GND	Ground

FUNCTIONAL DESCRIPTION

For ease of reading only the ETC 9420/9421/9422/9444/9445 are referenced. However, all such references apply equally to ETC 9320/9321/9322/9344/9345.

The internal architecture is shown in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" when it is reset, it is a logic "0".

Program memory

Program Memory consists of ROM, 1024 bytes for the ETC 9420/C 9421/ C 9422 and 2048 bytes for the ETC 9444/C 9445. These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

Data memory

Data memory consists of a 512-bit RAM for the ETC 9444/C 9445, organized as 8 data registers of 16 × 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the ETC 9420/C 9421/C 9422, organized as 4 data registers of 16 × 4 bits digits. The B register is 6 bits long. Upper 2 bis (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch, to input 4 bits of a ROM word, L I/O ports data, input 4 bits of G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be operated in two modes depending on a mask-programmable option : as a timer or as an external event counter. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in *Figure 10 a*.

Four general-purpose inputs, IN_3-IN_0, are provided. IN1, IN2 and IN3 may be selected, by a mask-programmable option as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode. D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be mask-programmed as an output for MICROBUS applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS® option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurence of a write strobe from the host CPU.

7/22

THOMSON SEMICONDUCTEURS

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS® | option allows L I/O port data to be latched into the Q register.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

The "EN register is an internal 4-bit register loaded under programm control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

0. The least significant bit of the enable register, EN_0. selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN_0 set, SIO is as asynchronous binary counter, DECREMENTING its value by one upon each low going pulse ("1" to "0") occuring on the SI input. Each pulse must be at least 2 (two) ins-

truction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO, SO can be enabled to output the most significant bit of SIO each instruction cycle time. The SK output SKL ANDed with the instruction cycle clock.

1. With EN_1 set interrupt is enabled. Immediatly following an interrupt, EN_1 is reset to disable further interrupts.

2. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high impedance input state.

3. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set(binary counter option selected), SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected, disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".
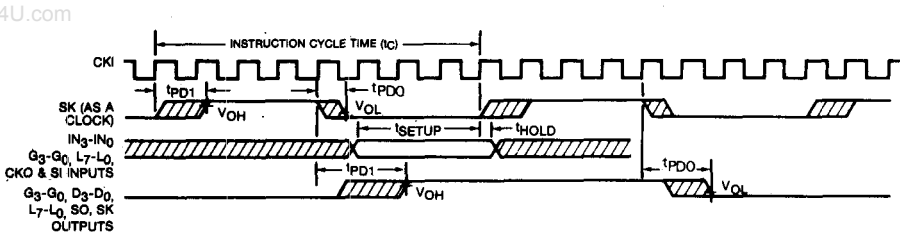

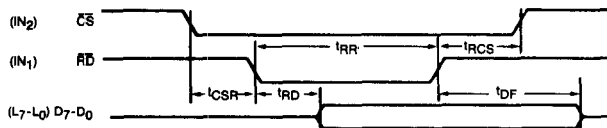FIGURE 3 — INPUT/OUTPUT TIMING DIAGRAMS (Divide-by-8 Mode)

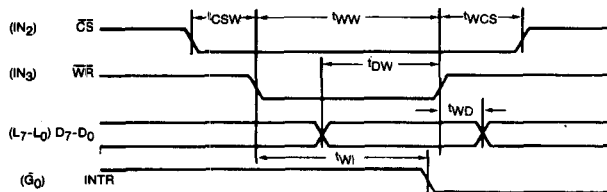FIGURE 4 — MICROBUS READ OPERATION TIMING

FIGURE 5 — MICROBUS WRITE OPERATION TIMING

THOMSON SEMICONDUCTEURS

FUNCTIONAL DESCRIPTION (continued)

TABLE 1 – ENABLE REGISTER MODES – BITS EN_0 AND EN_3

EN_0	EN_3	SIO	SI	SO	SK after XAS
0	0	Shift Register	Input to shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary counter	Input to Counter	0	SK = SLK
1	1	Binary counter	Input to Counter	1	SK = SKL

Interrupt

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address OFF (the last word of page 3) and EN_1 is reset.

b. An interrupt can be acknowledged only after the following conditions are met :

1. EN_1 has been set.

2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.

3. A currently executing instruction has been completed.

4. ALL successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon "popping" of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address OFF. At the end of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. **Subroutines should not be nested within the interrupt servicing routine** since their "popping" of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction at hex address OFF must be a NOP.

e. A LEI instruction may be put immediately before the RET to re-enable interrupts.

MICROBUS interface

The ETC 9420/C 9444 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from to a host microprocessor (μP). IN_1, IN_2 and IN_3 general purposes input become **MICROBUS INTERFACE** read-strobe, chip-select, and write-strobe lines, respectively. IN_1 become $\overline{RD}$ — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. IN_2 becomes $\overline{CS}$ — a logic "0" on this line selects the ETC 9420/C 9444 as the μP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN_3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the ETC 9420/C 9444. G_0 becomes $\overline{INTR}$, a "ready" output, reset by a write pulse from the μP on the $\overline{WR}$ line, providing the "hand-shaking" capability necessary for asynchronous data transfer between the host CPU and the ETC 9420/C 9444.

This option has been designed for compatibility with MICRO-BUS a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication). The functioning and timing relationships between the signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figure 4 and 5). Connection of the ETC 9420/C 9444 to the MICROBUS is shown in figure 6.
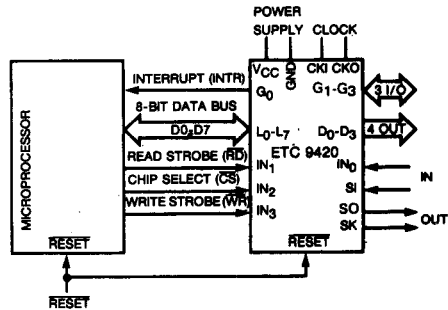

FIGURE 6 – MICROBUS® OPTION INTERCONNECT

Initialization

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency of CKI is greater than 32 kHz, otherwise the external RC network shown in Figure 7 must be connected to the $\overline{RESET}$ pin. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, providing it stays low for at least three instruction cycle times.

NOTE : if CKI clock is less than 32 kHz, the internal reset logic (option = 29 = 1) must be disabled and the external RC circuit must be used.
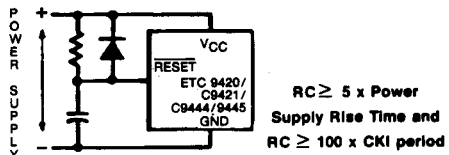

RC ≥ 5 x Power Supply Rise Time and RC ≥ 100 x CKI period

FIGURE 7 – POWER-UP CIRCUIT

9/22

FUNCTIONAL DESCRIPTION (continued)

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL Latch is set, this enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

Timer

There are two modes selected by mask option :

a. Time-base counter. In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The prescaler is cleared during execution of a CAMT instruction and on reset.

For example, using a 4 MHz crystal with a divide-by-16 option, the instruction cycle frequency of 250 kHz increments the 10-bit timer every 4 µs. By presetting the counter and detecting overflow, accurate timeouts between 16 µs (4 counts) and 4.096 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

b. External event counter. In this mode, a low-going pulse ("1" to "0") at least 2 instruction cycles wide on the IN2 input will increment the 8-bit T counter.

**Note** : The IT instruction is not allowed in this mode.

Halt mode

The ETC 9420/9421/C 9422/C 9444/C 9445 is a FULLY STATIC circuit ; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may be also halted by the HALT instruction or by forcing CKO high when it is used as an HALT/I/O port. Once in the HALT mode, the internal circuitry does not receive any clocksignal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The chip may be awakened by one of the two different methods.

1. Continue function — by forcing CKO low, if it is mask-programmed as an HALT I/O port, the system clock is reenabled and the circuit continues to operate from the point where it was stopped.

2. Restart — by forcing the $\overline{RESET}$ pin low (see initialization).

The HALT mode is the mininum power dissipation state.

NOTE : If the user has selected dual clock with D0 as external oscillator (option 30 = 2) AND the ETC 9444/C 9420 is running with the D0 clock, the HALT mode — either hardware or software — will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the D0 clock to minimize power.
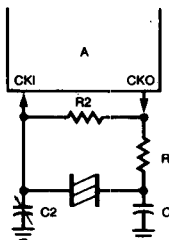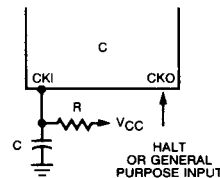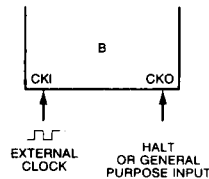

R/C controlled Oscillator

R	C	Cycle time	V_{CC}
15 k	82 pF	4 to 9 µs	≥ 4.5 V
30 k	82 pF	8 to 16 µs	≥ 4.5 V
60 k	100 pF	16 to 32 µs	2.4 to 4.5 V

Note : 15 k ≤ R ≤ 150 k ; 50 pF ≤ C ≤ 150 pF

Crystal or resonator

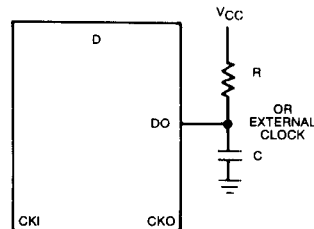| Crystal value	Component Values			
	R1	R2	C1 (pF)	C2 (pF)
32 kHz	220 k	20 M	30	6-36
455 kHz	5 k	10 M	80	40
2.086 MHz	2 k	1 M	30	6-36
4.0 MHz	1 k	1 M	30	6-36

FIGURE 8 – OSCILLATOR COMPONENTS VALUES

This circuit and these values are for indication only. As the oscillation characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application.

10/22

FUNCTIONAL DESCRIPTION (continued)

CKO Pin Options

· Two-pin oscillator — (Crystal). See *Figure 9A*.

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. The HALT mode may be entered by program control (HALT instruction) which forces CKO high, thus inhibiting the crystal network. The circuit can be awakened only by forcing the RESET pin to a logic "0" (restart).

b. One-pin oscillator — (RC or external). See *Figure 9B*.

If a one-pin oscillator system is chosen, two options are available for CKO :

● CKO can be selected as the HALT I/O port. In that case, it is an I/O flip-flop which is an indicator of the HALT status. An external signal can over-ride this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and CKO output will stay high to keep the chip stopped if the external driver returns to high impedance state.

By forcing a low level to CKO, the chip will continue and CKO will stay low.

● As another option, CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

Oscillator options

There are four basic clock oscillator configuration available as shown by *Figure 8*.

a. Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency optionally divided by 4, 8 or 16.

b. External Oscillator. The external frequency is optionally divided by 4, 8 or 16 to give the instruction cycle time. CKO is the HALT I/O port or a general purpose input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port or a general purpose input.

d. Dual oscillator. By selecting the dual clock option, pin D0 is now a single pin oscillator input. Two configurations are available : RC controlled Schmitt trigger oscillator or external oscillator.

The user may software select between the D0 oscillator (in that case, the instruction cycle time equals the D0 oscillation frequency divided by 4) by setting the D0 latch high or the CKI (CKO) oscillator by resetting D0 Latch low. Note that even in dual clock mode, the counter, if mask-programmed as a time-base counter, is always connected to the CKI oscillator.

For example, the user may connect up to a 1 MHz RC circuit to D0 for faster processing and a 32 kHz watch crystal to CKI and CKO for minimum current drain and time keeping.

Note : CTMA instructions is not allowed when chip is running from D0 clock.

Figures 10A and *10B* show the clock and timer diagrams with and without Dual clock.

ETC 9445/C 9421 24-Pin package option

If the ETC 9444/C 9420 is bonded in a 24-pin pckage, it becomes the ETC 9445/C 9421 illustrated in *Figure 2*. Connection diagrams. Note that the ETC 9445/C 9421 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, ocourse, use of th IN optons, interrupt feature, external event counter feature, and the MICROBUS option which uses IN_1-IN_3. All other options are available for the ETC 9445/C 9421.

Note : If user selects 24-pin package, options 9, 10, 19 and 20 must be selected as a "0" (load to V_{CC} on the IN intputs). See option list.
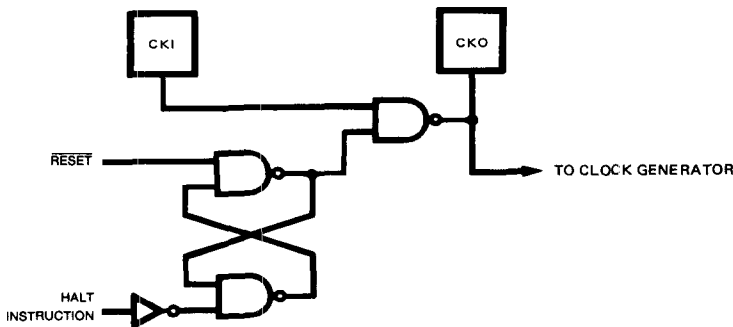
BLOCK DIAGRAMS

FIGURE 9 A – HALT MODE - TWO-PIN OSCILLATOR
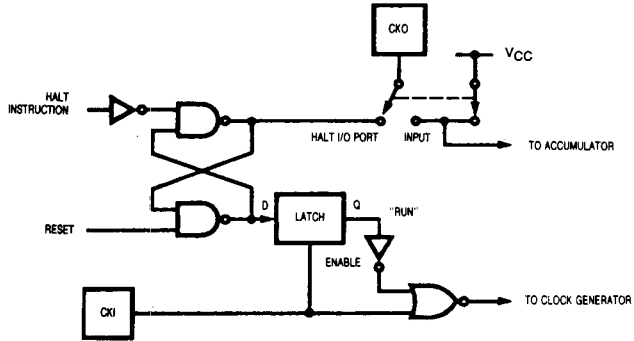
THOMSON SEMICONDUCTEURS

FIGURE 9 B — HALT MODE - ONE PIN OSCILLATOR
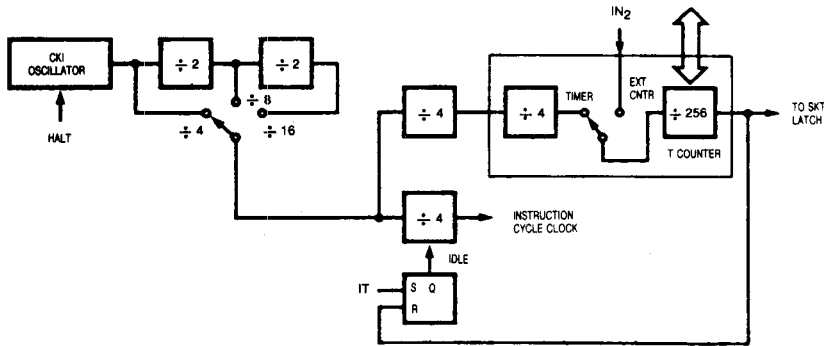

FIGURE 10 A — CLOCK AND TIMER BLOCK DIAGRAM WITHOUT DUAL-CLOCK
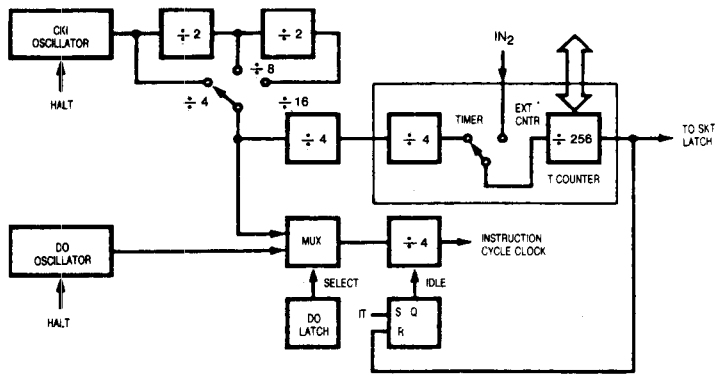
FIGURE 10 B — CLOCK AND TIMER BLOCK DIAGRAM WITH DUAL-CLOCK

THOMSON SEMICONDUCTEURS

INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

TABLE 2 – INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
Internal Architecture Symbols	
A	4-bit Accumulator
B	7-bit RAM address register (6-bit for ETC 9420)
Br	Upper 3 bits of B (register address) (2-bit for ETC 9420)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry register
D	4-bit Data output port
EN	4-bit Enable register
G	4-bit General purpose I/O port
IL	Two 1-bit (IN_0 and IN_3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/Oport
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q.	8-bit latch for L port
SA, SB, SC	11-bit 3-level subroutine stack
SIO	4 bit Shift register and counter
SK	Logic-controlled clock output
SKL	1-bit lach for SK output
T	8-bit timer

Instruction operand symbols

d	4-bit operand field, 0-15 binary (RAM digit select)
r	3(2)-bit operand field, 0-7(3)binary (RAM register select)
a	11-bit operand field, 0-2047 (1023)
y	4-bit Operand field, 0-15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x

Operational Symbols

+	Plus
—	Minus
→	Replaces
↔	is exchanged with
=	is equal to
$\overline{A}$	one's complement of A
⊕	exclusive-or
;	range of values

TABLE 3 – ETC 9444/C 9420 INSTRUCTION SET

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	[0 0 1 1|0 0 0 0]	$A + C + RAM(B) \rightarrow A$ Carry → C	Carry	Add with CARRY. Skip on Carry
ADD		31	[0 0 1 1|0 0 0 1]	$A + RAM(B) \rightarrow A$	None	Add RAM to A
ADT		4A	[0 1 0 0|1 0 1 0]	$A + 10_{10} \rightarrow A$	None	Add TEN TO A
AISC	y	5—	[0 1 0 1| y]	$A + y \rightarrow A$	Carry	Add Immediate Skip on Carry (y ≠ 0)
CASC		10	[0 0 0 1|0 0 0 0]	$\overline{A} + RAM(B) + C \rightarrow A$ Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	[0 0 0 0|0 0 0 0]	$0 \rightarrow A$	None	Clear A
COMP		40	[0 1 0 0|0 0 0 0]	$\overline{A} \rightarrow A$	None	Ones complement of A to A
NOP		44	[0 1 0 0|0 1 0 0]	None	None	No Operation
RC		32	[0 0 1 1|0 0 1 0]	$0 \rightarrow C$	none	Reset C
SC		22	[0 0 1 0|0 0 1 0]	$1 \rightarrow C$	None	Set C
XOR		02	[0 0 0 0|0 0 1 0]	$A \oplus RAM(B) \rightarrow A$	None	Exclusive-OR RAM with A

THOMSON SEMICONDUCTEURS

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	$\lvert1\,1\,1\,1\rvert1\,1\,1\,1\rvert$	$ROM(PC_{10:8},A,M) \rightarrow PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6 -	$\lvert0\,1\,1\,0\,0\rvert a_{10:8}\rvert$	$a \rightarrow PC$	None	Jump
		. .	$\lvert\quad a_{7:0}\quad\rvert$			
JP	a	. .	$1\rvert\quad a_{6:0}\quad$ (pages 2, 3, only)	$a \rightarrow PC_{6:0}$	None	Jump within Page (Note 4)
			or			
		. .	$\lvert1\,1\rvert\quad a_{5:0}\quad$ (all other pages)	$a \rightarrow PC_{5:0}$		
JSRP	a	. .	$\lvert1\,0\rvert\quad a_{5:0}\quad$	$PC + 1 \rightarrow SA \rightarrow SB \rightarrow SC$	None	Jump to Subroutine Page
				$00010 \rightarrow PC_{10:6}$		(Note 5)
				$a \rightarrow PC_{5:0}$		
JSR	a	6 -	$\lvert0\,1\,1\,0\,1\rvert a_{10:8}\rvert$	$PC + 1 \rightarrow SA \rightarrow SB \rightarrow SC$	None	Jump to Subroutine
			$\lvert\quad a_{7:0}\quad\rvert$	$a \rightarrow PC$		
RET		48	$\lvert0\,1\,0\,0\rvert1\,0\,0\,0\rvert$	$SC \rightarrow SB \rightarrow SA \rightarrow PC$	None	Return from Subroutine
RETSK		49	$\lvert0\,1\,0\,0\rvert1\,0\,0\,1\rvert$	$SC \rightarrow SB \rightarrow SA \rightarrow PC$	Always Skip on Return	Return from Subroutine then Skip
HALT		33	$\lvert0\,0\,1\,1\rvert0\,0\,1\,1\rvert$		None	HALT processor
		38	$\lvert0\,0\,1\,1\rvert1\,0\,0\,0\rvert$			
IT		33	$\lvert0\,0\,1\,1\rvert0\,0\,1\,1\rvert$			IDLE till timer
		39	$\lvert0\,0\,1\,1\rvert1\,0\,0\,1\rvert$		None	Overflows then continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33	$\lvert0\,0\,1\,1\rvert0\,0\,1\,1\rvert$	$A \rightarrow T_{7:4}$		
		3F	$\lvert0\,0\,1\,1\rvert1\,1\,1\,1\rvert$	$RAM(B) \rightarrow T_{3:0}$	None	Copy A, RAM to T
CTMA		33	$\lvert0\,0\,1\,1\rvert0\,0\,1\,1\rvert$	$T_{7:4} \rightarrow RAM(B)$		
		2F	$\lvert0\,0\,1\,0\rvert1\,1\,1\,1\rvert$	$T_{3:0} \rightarrow A$	None	Copy T to RAM, A (Note 9)
CAMQ		33.	$\lvert0\,0\,1\,1\rvert0\,0\,1\,1\rvert$	$A \rightarrow Q_{7:4}$	None	Copy A, RAM to Q
		3C	$\lvert0\,0\,1\,1\rvert1\,1\,0\,0\rvert$	$RAM(B) \rightarrow Q_{3:0}$		
CQMA		33	$\lvert0\,0\,1\,1\rvert0\,0\,1\,1\rvert$	$Q_{7:4} \rightarrow RAM(B)$	None	Copy Q to RAM, A
		2C	$\lvert0\,0\,1\,0\rvert1\,1\,0\,0\rvert$	$Q_{3:0} \rightarrow A$		
LD	r	. 5	$\lvert0\,0\rvert r\rvert0\,1\,0\,1\rvert$	$RAM(B) \rightarrow A$	None	Load RAM into A
			$(r = 0\ 3)$	$Br \oplus r \rightarrow Br$		Exclusive-OR Br with r
LDD	r d	23	$\lvert0\,0\,1\,0\rvert0\,0\,1\,1\rvert$	$RAM(r\ d) \rightarrow A$	None	Load A with RAM pointed
			$\lvert0\rvert r\rvert\quad d\quad\rvert$			to directly by r d
LQID		BF	$\lvert1\,0\,1\,1\rvert1\,1\,1\,1\rvert$	$ROM(PC_{10:8},A,M) \rightarrow Q$	None	Load Q Indirect (Note 3)
RMB	0	4C	$\lvert0\,1\,0\,0\rvert1\,1\,0\,0\rvert$	$0 \rightarrow RAM(B)_0$	None	Reset RAM Bit
	1	45	$\lvert0\,1\,0\,0\rvert0\,1\,0\,1\rvert$	$0 \rightarrow RAM(B)_1$		
	2	42	$\lvert0\,1\,0\,0\rvert0\,0\,1\,0\rvert$	$0 \rightarrow RAM(B)_2$		
	3	43	$\lvert0\,1\,0\,0\rvert0\,0\,1\,1\rvert$	$0 \rightarrow RAM(B)_3$		

14/23

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SMB	0	4D	0 1 0 0 1 1 0 1	$1 \to RAM(B)_0$	None	Set RAM Bit
	1	47	0 1 0 0 0 1 1 1	$1 \to RAM(B)_1$		
	2	46	0 1 0 0 0 1 1 0	$1 \to RAM(B)_2$		
	3	4B	0 1 0 0 1 0 1 1	$1 \to RAM(B)_3$		
STII	y	7 -	0 1 1 1 Y	$y \to RAM(B)$	None	Store Memory Immediate
				$Bd \oplus 1 \to Bd$		and increment Bd
X	r	- 6	0 0 r 0 1 1 0	$RAM(B) \leftrightarrow A$	None	Exchange RAM with A,
			(r = 0:3)	$Br \oplus r \to Br$		Exclusive-OR Br with r
XAD	r,d	23	0 0 1 0 0 0 1 1	$RAM(r,d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r, d
		--	1 r d			
XDS	r	- 7	0 0 r 0 1 1 1	$RAM(B) \leftrightarrow A$	Bd	Exchange RAM with A
			(r = 0:3)	$Bd - 1 \to Bd$	decrements	and Decrement Bd.
				$Br \oplus \to Br$	past 0	Exclusive-Or Br with r
XIS	r	- 4	0 0 r 0 1 0 0	$RAM(B) \leftrightarrow A$	Bd	Exchange RAM with A
			(r = 0:3)	$Bd + 1 \to Bd$	increments	and Increment Bd,
				$Br \oplus r \to Br$	past 15	Exclusive-Or Br with r

REGISTER REFERENCE INSTRUCTIONS

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
CAB		50	0 1 0 1 0 0 0 0	$A \to Bd$	None	Copy A to Bd
CBA		4E	0 1 0 0 1 1 1 0	$Bd \to A$	None	Copy Bd to A
LBI	r,d	- -	0 0 r (d-1)	$r,d \to B$	Skip until	Load B immediate with r,d
			(r = 0:3)		not a LBI	(Note 6)
			(d = 0,9:15) or			
		33	0 0 1 1 0 0 1 1			
		- -	1 r d			
			(any r, any d)			
LEI	y	33	0 0 1 1 0 0 1 1	$y \to EN$	None	Load EN Immediate (Note 7)
		6 -	0 1 1 0 y			
XABR		12	0 0 0 1 0 0 1 0	$A \leftrightarrow Br$	None	Exchange A with Br (Note 8)

TEST INSTRUCTIONS

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SKC		20	0 0 1 0 0 0 0 0		C = "1"	Skip if C is True
SKE		21	0 0 1 0 0 0 0 1		A = RAM(B)	Skip if A Equals RAM
SKGZ		33	0 0 1 1 0 0 1 1		$G_{3:0} = 0$	Skip if G is Zero
		21	0 0 1 0 0 0 0 1			(all 4 bits)
SKGBZ		33	0 0 1 1 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 0 0 0 1		$G_0 = 0$	
	1	11	0 0 0 1 0 0 0 1	2nd byte	$G_1 = 0$	
	2	03	0 0 0 0 0 0 1 1		$G_2 = 0$	
	3	13	0 0 0 1 0 0 1 1		$G_3 = 0$	

THOMSON SEMICONDUCTEURS

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SKMBZ	0	01	0 0 0 0 0 0 0 1		RAM $(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0 0 0 1 0 0 0 1		RAM $(B)_1 = 0$	
	2	03	0 0 0 0 0 0 1 1		RAM $(B)_2 = 0$	
	3	13	0 0 0 1 0 0 1 1		RAM $(B)_3 = 0$	
SKT		41	0 1 0 0 0 0 0 1		A time-base counter carry has occured since last test	Skip on Timer (Note 3)

INPUT/OUTPUT INSTRUCTIONS

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ING		33	0 0 1 1 0 0 1 1	$G \rightarrow A$	None	Input G Ports to A
		2A	0 0 1 0 1 0 1 0			
ININ		33	0 0 1 1 0 0 1 1	$IN \rightarrow A$	None	Input IN inputs to A
		28	0 0 1 0 1 0 0 0			(Note 2)
INIL		33	0 0 1 1 0 0 1 1	IL_3, CKO, "0", $IL_0 \rightarrow A$	None	Input IL Latches to A
		29	0 0 1 0 1 0 0 1			(Note 3)
INL		33	0 0 1 1 0 0 1 1	$L_{7:4} \rightarrow RAM(B)$	None	Input L Ports to RAM, A
		2E	0 0 1 0 1 1 1 0	$L_{3:0} \rightarrow A$		
OBD		33	0 0 1 1 0 0 1 1	$Bd \rightarrow D$	None	Output Bd to D Outputs
		3E	0 0 1 1 1 1 1 0			
OGI		33	0 0 1 1 0 0 1 1	$y \rightarrow G$	None	Output to G Ports
		5 -	0 1 0 1 y			Immediate
OMG		33	0 0 1 1 0 0 1 1	$RAM(B) \rightarrow G$	None	Output RAM to G Ports
		3A	0 0 1 1 1 0 1 0			
XAS		4F	0 1 0 0 1 1 1 1	$A \rightarrow SIO$ $C \rightarrow SKL$	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.

Note 3 : For additional on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine page 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d=0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9(1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register)

Note 8 : For 2K ROM devices. A $\leftrightarrow$ Br (0 $\rightarrow$ A3). For 1K ROM devices. A $\leftrightarrow$ Br (0,0 $\rightarrow$ A3, A2).

Note 9 : Do not use CTMA instruction when dual - option is selected and part is running from D0 Clocks.

DESCRIPTION OF SELECTED INSTRUCTIONS

Xas Instruction

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows : A → PC(7:4), RAM(B) → PC(3:0), leaving PC(10), PC(9) and PC(8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program excecution. Since LQID pushes SB → SC, the previous contents of SC are lost.

Note : LQID uses 2 instruction cycles if executed, one if skipped.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10, PC9 and PC8 are not affected by JID.

Note : JID uses 2 instruction cycles if executed, one if skipped.

SKT Instruction

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

Note : If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter :

CAMT ; load T counter
SKT : skip if overflow flag is set and reset it
NOP

IT Instruction

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. Upon overflow, the processor will restart with a delay shorter than one cycle time. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped. IT instruction is not allowed if the T counter is mask-programmed as an external event counter (option # 31 = 1).

INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occured on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO INTO A2. If CKO has not been so programmed, a "1" will be placed in A2. A 0 is input into A1. IL latches are cleared on reset. IL latches are not available on the ETC 9445/C 9421.

Instruction set notes

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example : a JP Located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note : The ETC 9420/C 9421/C 9422 needs only 10 bits to address its ROM. Therefore, the eleventh bit (10) is ignored.

POWER DISSIPATION

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. For example, a 500 kHz crystal input will typical draw 100 μA more than a square-wave input. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the ETC 9444/C 9445 operating current drain.

$$I_{CO} = I_Q + V \times 40 \times Fi + V \times 1400 \times Fi/Dv$$

where I_{CO} = chip operating current drain in microamps
I_Q = quiescent leakage current (from curve)
Fi = CKI frequency in MegaHertz
V = chip V_{CC} in volts
Dv = divide by option selected.

For example at 5 volts V_{CC} and 400 kHz (divide by 4)
$I_{CO} = 20 + 5 \times 40 \times 0.4 + 5 \times 1400 \times 0.4/4$
$I_{CO} = 20 + 80 + 700 = 800 \mu A$

At 2.4 volts V_{CC} and 30 kHz (divide by 4)
$I_{CO} = 6 + 2.4 \times 40 \times 0.03 + 2.4 \times 1400 \times 0.03/4$
$I_{CO} = 6 + 2.88 + 25.2 = 34.08 \mu A$

THOMSON SEMICONDUCTEURS

POWER DISSIPATION (continued)

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation :

$$Ici = I_Q + V \times 40 \times Fi$$

For example, at 5 volts V_{CC} and 400 kHz

$$Ici = 20 + 5 \times 40 \times 0.4 = 100 \, \mu A$$

The total average current will then be the weighted average of the operation current and the idle current :

$$Ita = I_{CO} \times \frac{To}{To + Ti} + Ici \times \frac{Ti}{To + Ti}$$

where : Ita = total average current
I_{CO} = operating current
Ici = idle current
To = operating time
Ti = idle time

I/O options

ETC 9444/C 9445 outputs have the following optional configurations, illustrated in *Figure 11* :

a. Standard—A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current—This is the same configuration as a. above except that the sourcing current is much less.

c. Open Drain—An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Ouput—A CMOS output buffer similar to a. witch may be disabled by program control.

e. Low-Current TRI-STATE L Output—This is the same as d. above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L. Output—This has the N-channel device to ground only.

All inputs have the following options :

g. Input with on chip load device to V_{CC}.

h. Hi-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available : Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT} curves are given in *Figure 12* for each of these devices to allow the designer to effectively use these I/O configurations.
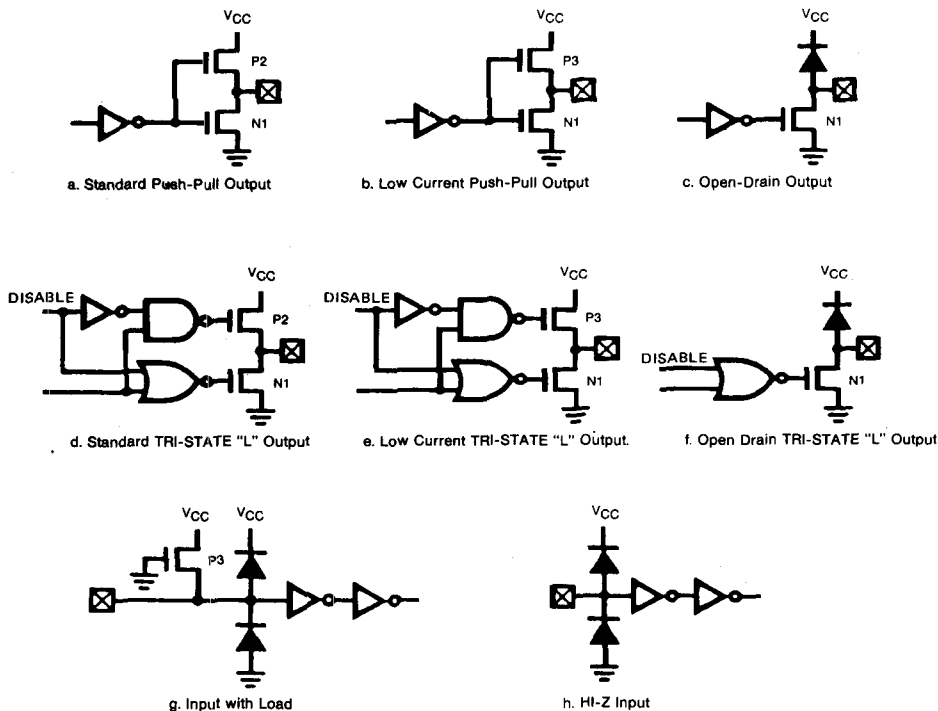

a. Standard Push-Pull Output

b. Low Current Push-Pull Output

c. Open-Drain Output

d. Standard TRI-STATE "L" Output

e. Low Current TRI-STATE "L" Output.
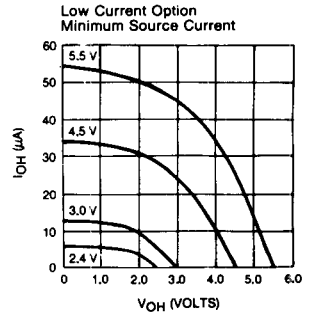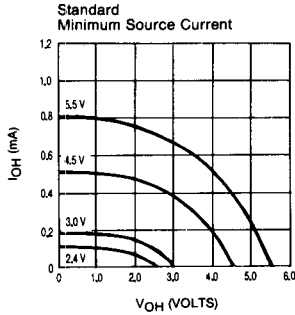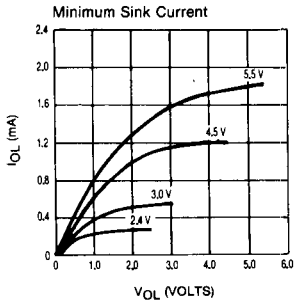
f. Open Drain TRI-STATE "L" Output

g. Input with Load

h. Hi-Z Input

FIGURE 11 — INPUT/OUTPUT CONFIGURATIONS

18/22

THOMSON SEMICONDUCTEURS

POWER DISSIPATION (continued)

Minimum Sink Current

Standard
Minimum Source Current

Low Current Option
Minimum Source Current
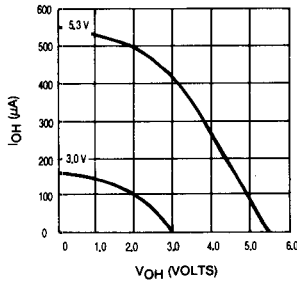
ETC 9420/ETC9444
ETC9421/ETC9445
ETC9422
Low Current Option
Maximum Source Current
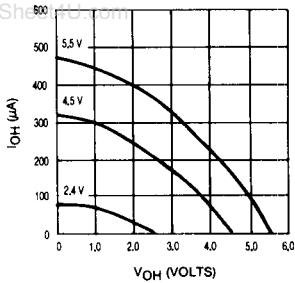
ETC9320/ETC9344
ETC9321/ETC9345
ETC9322
Low Current Option
Maximum Source Current
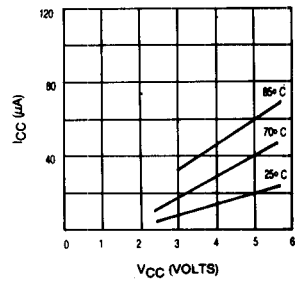
Maximum Quiescent Current

FIGURE 12 -- INPUT/OUTPUT CHARACTERISTICS

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OPTION LIST

The ETC 9444/C 9420/C 9445/C 9421/C 9422 mask-programmable options are assigned numbers which correspond with the ETC 9344/C 9320/C 9345/C 9321/C 9322 pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0 : Ground Pin — no option available.

Option 2 : CKO Pin
= 0 : clock generator output to crystal/resonator
= 1 : HALT I/O port
= 2 : general purpose input with load device to v_{CC}
= 3 : general purpose input, high-Z

Option 3 : CKI input
= 0 : Crystal controlled oscillator input divide by 4
= 1 : Crystal controlled oscillator input divide by 8
= 2 : Crystal controlled oscillator input divide by 16
= 4 : Single-pin RC controlled oscillator (divide by 4)
= 5 : External oscillator input divide by 4
= 6 : External oscillator input divide by 8
= 7 : External oscillator input divide by 16

Option 4 : RESET input
= 0 : load device to v_{CC}
= 1 : Hi-Z input

Option 5 : L7 Driver
= 0 : Standard TRI-STATE push-pull output
= 1 : Low-current TRI-STATE push-pull output
= 2 : Open-drain TRI-STATE output

Option 6 : L6 Driver — (same as option 5)

Option 7 : L5 Driver — (same as option 5)

Option 8 : L4 Driver — (same as option 5)

Option 9 : IN1 input
= 0 : load device to v_{CC}
= 1 : Hi-Z input

Option 10 : IN2 input — (same as option 9)

Option 11 = 0 : v_{CC} Pin — no option available

Option 12 : L3 Driver — (same as option 5)

Option 13 : L2 Driver — (same as option 5)

Option 14 : L1 Driver — (same as option 5)

Option 15 : L0 Driver — (same as option 5)

Option 16 : Si Input — (same as option 9)

Option 17 : SO Driver
= 0 : Standard push-pull output
= 1 : Low-current push-pull output
= 2 : Open-drain output

Option 18 : SK Driver — (same as option 17)

Option 19 : IN0 Input — (same as option 9)

Option 20 : IN3 Input — (same as option 9)

Option 21 : G0 I/O Port — (same as option 17)

Option 22 : G1 I/O Port — (same as option 17)

Option 23 : G2 I/O Port — (same as option 17)

Option 24 : G3 I/O Port — (same as option 17)

Option 25 : D3 Output — (same as option 17)

Option 26 : D2 Output — (same as option 17)

Option 27 : D1 Output — (same as option 17)

Option 28 : D0 Output — (same as option 17)

Option 29 : Internal Initialization Logic
= 0 : Normal operation
= 1 : No internal initialization logic

Option 30 : Dual Clock
= 0 : Normal operation
= 1 : Dual Clock. D0 RC oscillator } (opt. #28 must = 2)
= 2 : Dual Clock. D0 ext. clock input }

Option 31 : Timer
= 0 : Time-base counter
= 1 : External event counter

Option 32 : MICROBUS
= 0 : Normal
= 1 : MICROBUS (opt. #31 must = 0)

Option 33 : Chip bonding
(1 K and 2 K Microcontroller)
= 0 : 28 - pin package
= 1 : 24 - pin package
= 2 : Same die purchased in both 24 and 28 pin version
(1 K Microcontroller only)
= 3 : 20 - pin package
= 4 : 28- and 20- pin package
= 5 : 24- and 20- pin package
= 6 : 28-, 24- and 20- pin package

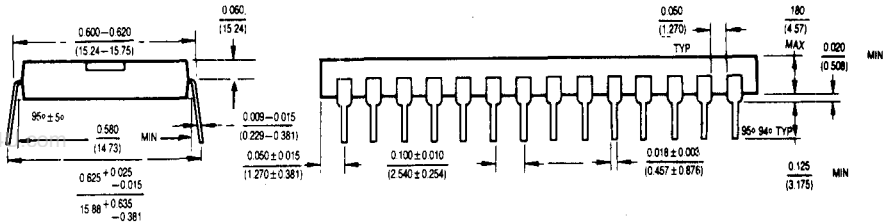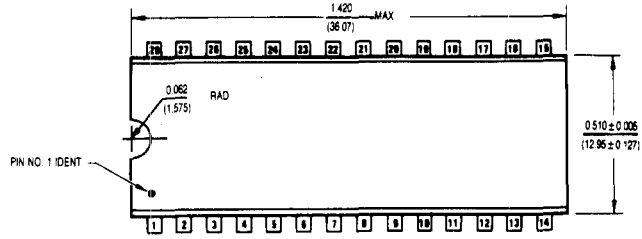**Note :** - If opt # 33 = 2 then opt # 9, 10, 19, 20 and 32 must = 0
- If opt # 33 = 3, 4, 5 or 6 then opt # 9, 10, 19, 20, 21, 22, 30 and 32 must = 0

CROSS REFERENCE	
THOMSON SC	NS
ETC 9420	COP 424 C
ETC 9421	COP 425 C
ETC 9422	COP 426 C
ETC 9444	COP 444 C
ETC 9445	COP 445 C

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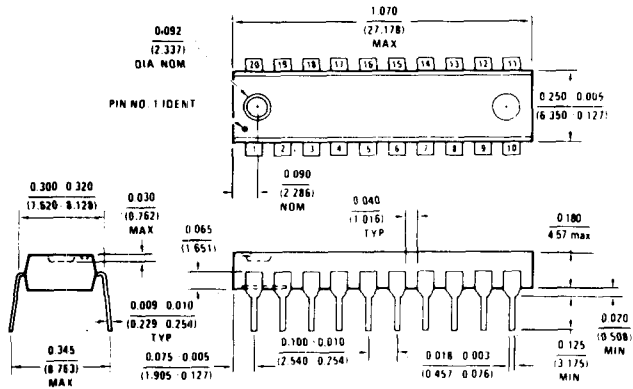**PHYSICAL DIMENSIONS** inches (millimeters) (continued)

28 - LEAD CAVITY DUAL-IN-LINE PACKAGE (N)
ETC9420 / C 9320 / C 9444 / C 9344 / N

DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION
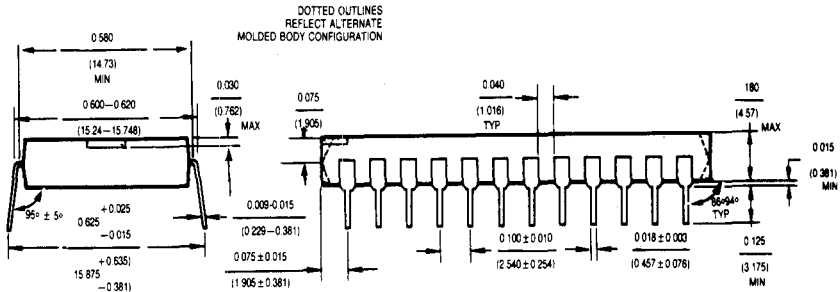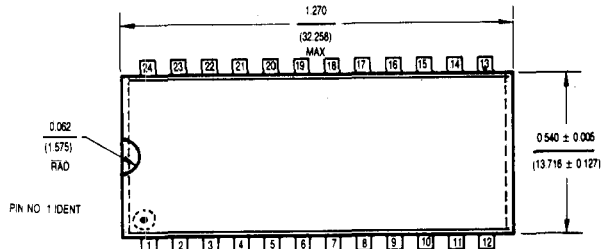
24 - LEAD MOLDED DUAL-IN-LINE PACKAGE (N)
ETC9421 / C 9445 / C 9321 / C 9345 / N

21/22

THOMSON SEMICONDUCTEURS

PHYSICAL DIMENSIONS inches (millimeters) (continued)

MOLDED DUAL-IN-LINE PACKAGE (N)
ETC 9422 / C 9322 / N

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

22/22

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