Integrated Device Technology, Inc.

IDT79R3051 FAMILY OF INTEGRATED RISControllers™

PRELIMINARY

IDT 79R3051™, 79R3051E
IDT 79R3052™, 79R3052E

T-49-17-32

FEATURES:

- Instruction set compatible with IDT79R3000A and IDT79R3001 MIPS RISC CPUs
- High level of integration minimizes system cost, power consumption
  - 79R3000A /79R3001 RISC Integer CPU
  - R3051 features 4kB of Instruction Cache
  - R3052 features 8kB of Instruction Cache
  - All devices feature 2kB of Data Cache
  - "E" Versions (Extended Architecture) feature full function Memory Management Unit, including 64-entry Translation Lookaside Buffer (TLB)
  - 4-deep write buffer eliminates memory write stalls
  - 4-deep read buffer supports burst refill from slow memory devices
  - On-chip DMA arbiter
  - Bus Interface Minimizes Design Complexity
- Single clock input with 40%-60% duty cycle
- Direct interface to R3720/21/22 RISChipset™
- 35 MIPS, over 64,000 Dhrystones at 40 MHz
- Low cost 84-pin PLCC packaging with optional thermal slug
- Flexible bus interface allows simple, low cost designs
- 20, 25, 33, and 40 MHz operation
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point Software
  - Page Description Languages

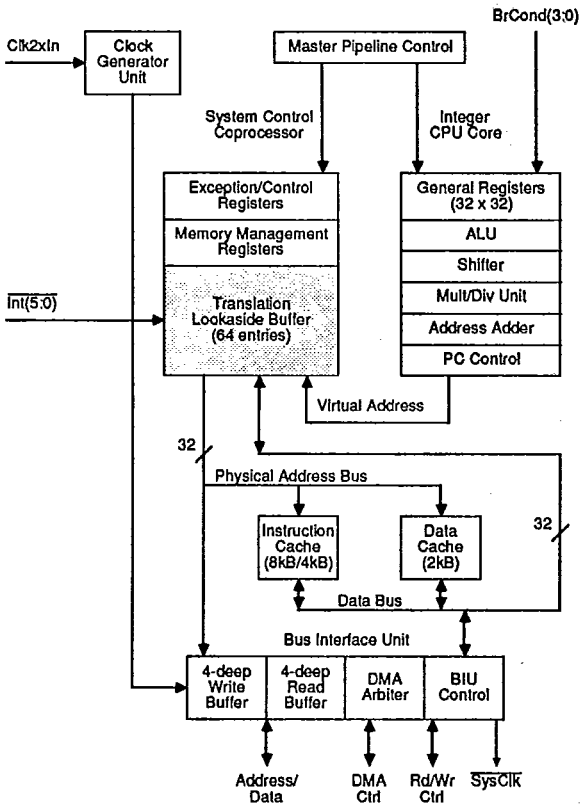

Figure 1. R3051 Family Block Diagram

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INTRODUCTION

The IDT R3051 Family is a series of high-performance 32-bit microprocessors featuring a high level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost, without significantly degrading system performance. Thus, the R3051 family is able to offer 35 MIPS of integer performance at 40 MHz without requiring external SRAM or caches.

Further, the R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging for devices up to 25 MHz. The R3051 family allows customer applications to bring maximum performance at minimum cost.

Figure 1 shows a block level representation of the functional units within the R3051 family. The R3051 family could be viewed as the embodiment of a discrete solution built around the IDT 79R3000A or 79R3001. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Currently, there are four members of the R3051 family family. All devices are pin and software compatible: the differences lie in the amount of instruction cache, and in the memory management capabilities of the processor:

- The R3052"E" incorporates 8kB of Instruction Cache, and features a full function memory management unit (MMU) including a 64-entry fully-associative Translation Lookaside Buffer (TLB). This is the same memory management unit incorporated in the IDT 79R3000A and 79R3001.
- The R3052 also incorporates 8kB of Instruction Cache. However, the memory management unit is a much simpler subset of the capabilities of the enhanced versions of the architecture, and in fact does not use a TLB.
- The R3051"E" incorporates 4kB of Instruction Cache. Additionally, this device features the same full function MMU (including TLB file) as the R3052"E", and R3000A.
- The R3051 incorporates 4kB of Instruction Cache, and uses the simpler memory management model of the R3052.

An overview of the functional blocks incorporated in these devices follows.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3051 family implements the MIPS ISA. In fact, the execution engine of the R3051 family is the same as the execution engine of the R3000A (and R3001). Thus, the R3051 family is binary compatible with those CPU engines.

The execution engine of the R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the R3051 family pipeline.

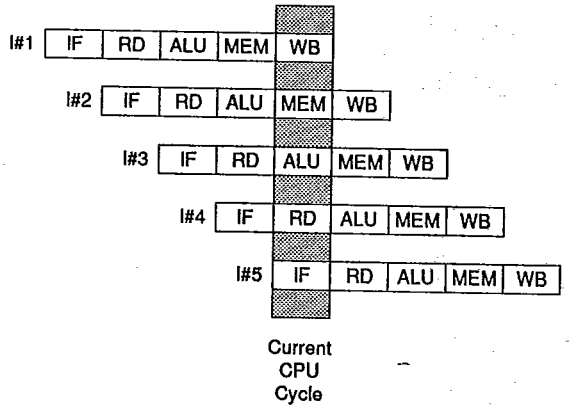

Figure 2. R3051 Family 5-Stage Pipeline

System Control Co-Processor

The R3051 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the R3051 family, as well as the virtual to physical mapping of the R3051 family.

There are two versions of the R3051 family architecture: the Extended Architecture Versions (the R3051E and R3052E) contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard mapped to physical addresses, and kernel and user segments which are mapped on a page basis by the TLB into anywhere within the 4GB physical address space. In this TLB, 8 page translations can be "locked" by the kernel to insure deterministic response in real-time applications. These versions thus use the same MMU structure as that found in the IDT 79R3000A and 79R3001. Figure 3 shows the virtual to physical address mapping found in the Extended Architecture versions of the processor family.

The Extended Architecture devices allow the system designer to implement kernel software to dynamically manage User task utilization of memory resources, and also allow the Kernel to effectively "protect" certain resources from user tasks. These capabilities are important in a number of embedded applications, from process control (where resource protection may be extremely important) to X-Window display systems (where virtual memory management is extremely important), and can also be used to simplify system debugging.

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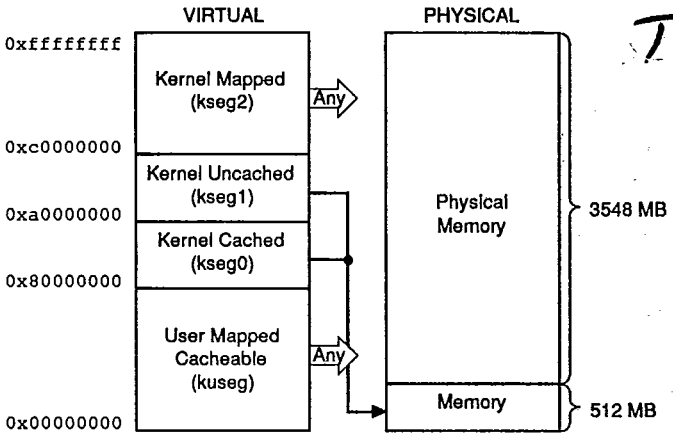

Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

The base versions of the architecture (the R3051 and R3052) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. The base processors support distinct kernel and user mode operation without requiring page management software, leading to a simpler software model. The memory mapping used by these devices is illustrated in figure 4. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

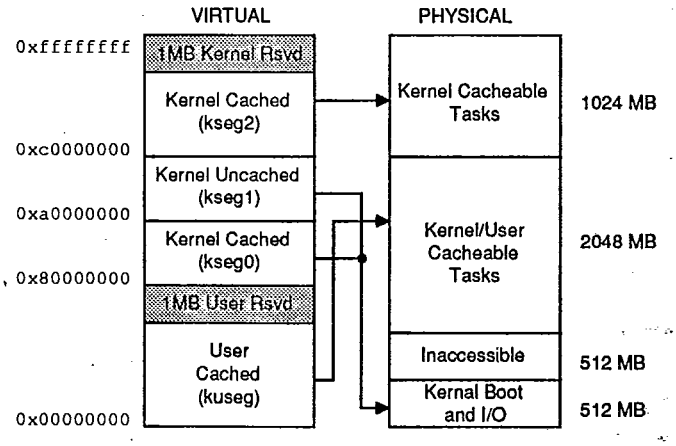

Figure 4. Virtual to Physical Mapping of Base Architecture Versions

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Clock Generation Unit

The R3051 family is driven from a single input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A and R3001 based applications.

Instruction Cache

The current family includes two different instruction cache sizes: the R3051 family (the R3051 and R3051E) feature 4kB of instruction cache, and the R3052 and R3052E each incorporate 8kB of Instruction Cache. For all four devices, the instruction cache is organized as a line size of 16 bytes (four words). This relatively large cache achieves a hit rate well in excess of 95% in most applications, and substantially contributes to the performance inherent in the R3051 family. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

Data Cache

All four devices incorporate an on-chip data cache of 2kB, organized as a line size of 4 bytes (one word). This relatively large data cache achieves hit rates well in excess of 90% in most applications, and contributes substantially to the performance inherent in the R3051 family. As with the Instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE signal to de-multiplex the A/D bus, and simple handshake signals to process processor read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3051 family incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and presents it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3051/52 read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving), if desired, in high-performance systems, or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches. Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize the read buffer to process quad word reads from slower memory systems.

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SYSTEM USAGE

The IDT R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application specific peripherals. These systems may also typically contain large, slow static RAMs, although the IDT R3051 family has been designed to not specifically require the use of external SRAMs.

Figure 5 shows a typical system block diagram. Transparent latches are used to de-multiplex the R3051/52 address and data busses from the A/D bus. The data paths between the memory system elements and the R3051 family A/D bus is managed by simple octal devices. A small set of simple PALs can be used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Alternately, the memory interface can be constructed using the IDT R3051 family RISChipset, which includes DRAM control, data path control for interleaved memories, and other general memory and system interface control functions. These devices are described in separate data sheets. Figure 6 illustrates a simple system constructed using the R3051 RISChipset.

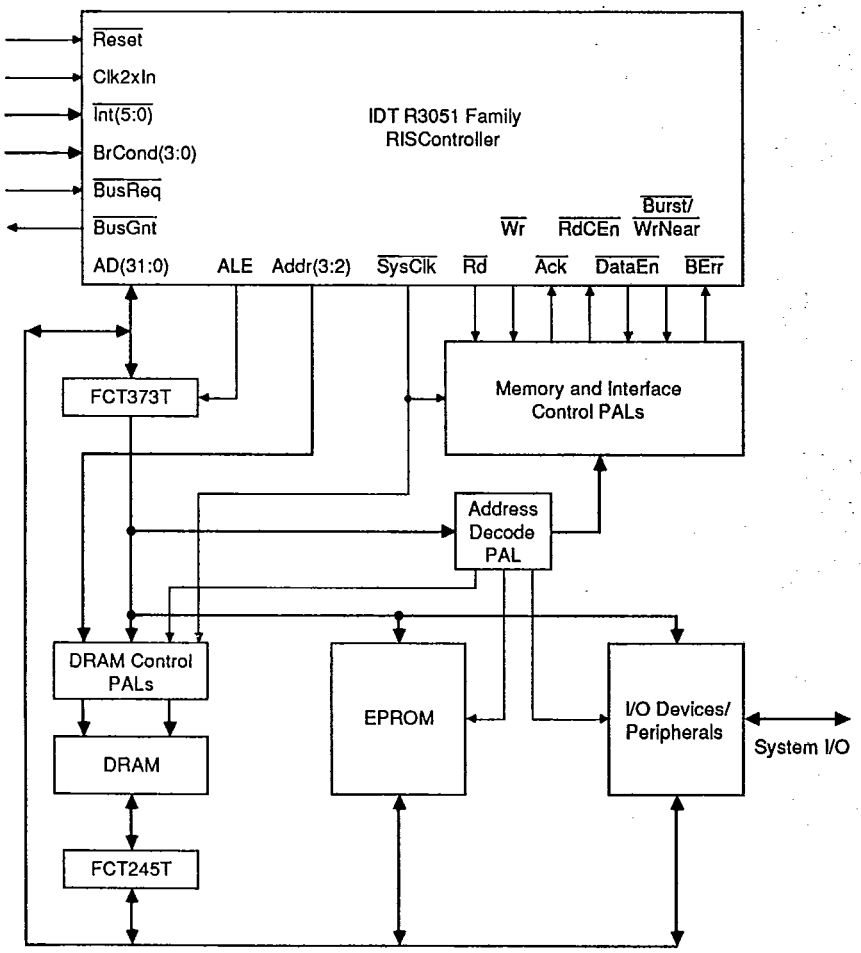

Figure 5. Typical R3051 Family Based System

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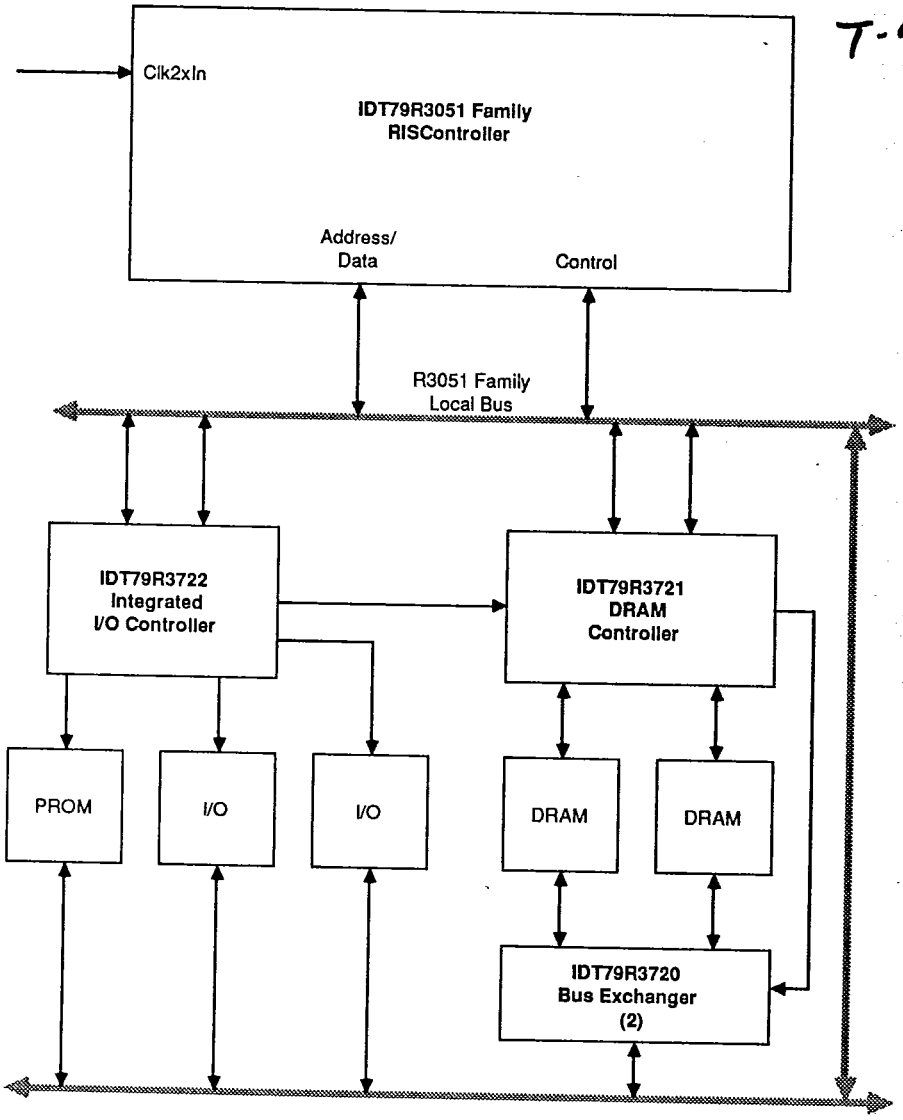

Figure 6. R3051 Family Chip Set Based System

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through prom monitor support, logic analysis tools, and sub-system modules.

Figure 7 is an overview of the system development process typically used when developing R3051 family-based applications. The R3051 family is supported by powerful tools through all phases of project development. These tools allow timely, parallel development of hardware and software for R3051/52 based applications, and include tools such as:

- A program, Cache-3051, which allows the performance of an R3051 family based system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- IDT Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, which has been integrated into the compiler toolchain to allow software floating point to replace hardware floating point without modifying the original source code.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT Prom Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT R3051 family.
- The IDT Prom Monitor, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- An In-Circuit Emulator, developed and sold by Embedded Performance, Inc.

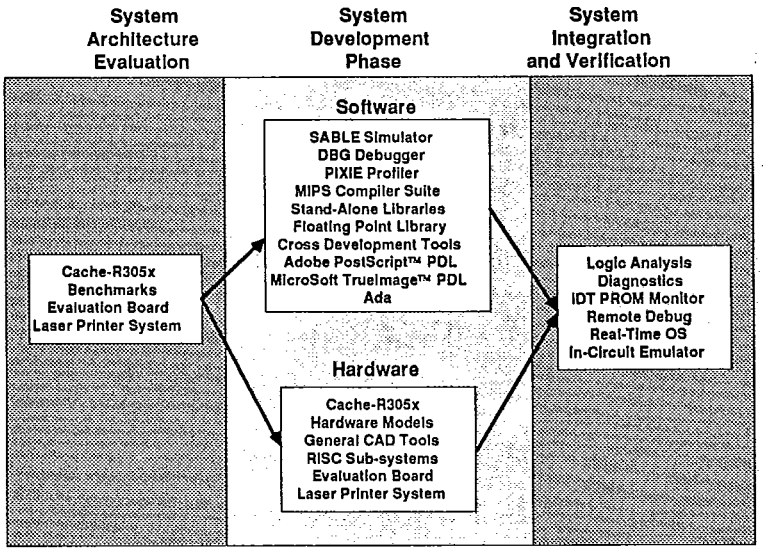

Figure 7. R3051 Family Development Toolchain

PERFORMANCE OVERVIEW

The R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations at a single cycle rate, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 MIPS performance when operating out of cache.
- **Large on-chip caches.** The R3051 family contains caches which are substantially larger than those on the majority of today's embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate.
- **Autonomous multiply and divide operations.** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3051 family to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The R3051 family features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve 35 MIPS integer performance, and over 64,000 dhrystones at 40 MHz without the use of external caches or zero wait-state memory devices.

SELECTABLE FEATURES

The R3051 family allows the system designer to configure some aspects of operation. These aspects are established when the device is reset, and include:

- BigEndian vs. LittleEndian operation: The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communications between various types of processors and databases.
- Data cache refill of one or four words: The memory system must be capable of performing 4 word transfers to satisfy cache misses. This option allows the system designer to choose between one and four word refill on data cache misses, depending on the performance each option brings to his application.

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THERMAL CONSIDERATIONS

The R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the R3051 family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package, coupled with the power reduction techniques employed in the design of the R3051 family, allows operation at speeds to 25MHz. However, at higher speeds, additional thermal care must be taken.

Thus, the R3051 family is also available in the "PH" package, which is basically a cavity down PLCC with an embedded exposed thermal slug. The thermal slug makes direct contact with the back of the die, allowing efficient thermal transfer between the die and the case of the part. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The PH package is available at all frequencies, and is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

Finally, the R3051 family is also available in a cavity down PGA with integral thermal slug. As with the PH package, this package is highly thermally efficient, and is appropriate for use in more extreme temperature conditions, such as military applications.

The members of the R3051 family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\emptyset_{CA}$) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \emptyset_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $\emptyset_{CA}$ at various airflows are shown in Table 1 for the various packages.

	Airflow (ft/min)					
$\emptyset_{CA}$	0	200	400	600	800	1000
"J" Package	29	26	21	18	16	15
"PH" Package*	22	8	3	2	1.5	1
PGA Package	22	8	3	2	1.5	1

Table 1. Thermal Resistance ($\emptyset_{CA}$) at Various Airflows (*estimated: final values tbd)

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PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0):** These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss.The value of this pin at this time in other than read cycles is undefined. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers

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PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Burst}}$/ $\overline{\text{WrNear}}$	O	**Burst Transfer/Write Near:** On read transactions, the $\overline{\text{Burst}}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected at device reset time. On write transactions, the $\overline{\text{WrNear}}$ output tells the external memory system that the bus interface unit performing back-to-back write transactions to an address within the same 256 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{\text{Rd}}$	O	**Read:** An output which indicates that the current bus transaction is a read.
$\overline{\text{Wr}}$	O	**Write:** An output which indicates that the current bus transaction is a write.
$\overline{\text{Ack}}$	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.
$\overline{\text{RdCEn}}$	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{\text{SysClk}}$	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
$\overline{\text{BusReq}}$	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{\text{BusGnt}}$	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a $\overline{\text{BusReq}}$ has been detected, and that the bus is relinquished to the external master.
SBrCond(3:2) BrCond(1:0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously.
$\overline{\text{BErr}}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{\text{Int}}$(5:3) $\overline{\text{SInt}}$(2:0)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{\text{Int}}$(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the $\overline{\text{SInt}}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
Clk2xIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
$\overline{\text{Reset}}$	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{\text{Reset}}$.
Rsvd(4:0)	I/O	**Reserved:** These five signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins.

C

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
VIN	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed Vcc +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

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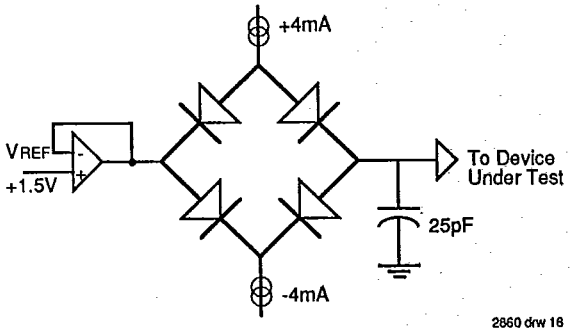
Grade	Temperature	GND	Vcc
Military	-55°C to +125°C (Case)	0V	5.0 ±10%
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

OUTPUT LOADING FOR AC TESTING



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DC ELECTRICAL CHARACTERISTICS — (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	350	—	400	—	500	—	600	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-100	—	-100	—	-100	—	-100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-100	100	-100	100	-100	100	-100	100	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xIn and $\overline{Reset}$.
3. V_{IH} should not be held above V_{CC} + 0.5 volts.
4. Guaranteed by design.

2860 tbl 10

C

T-49-17-32

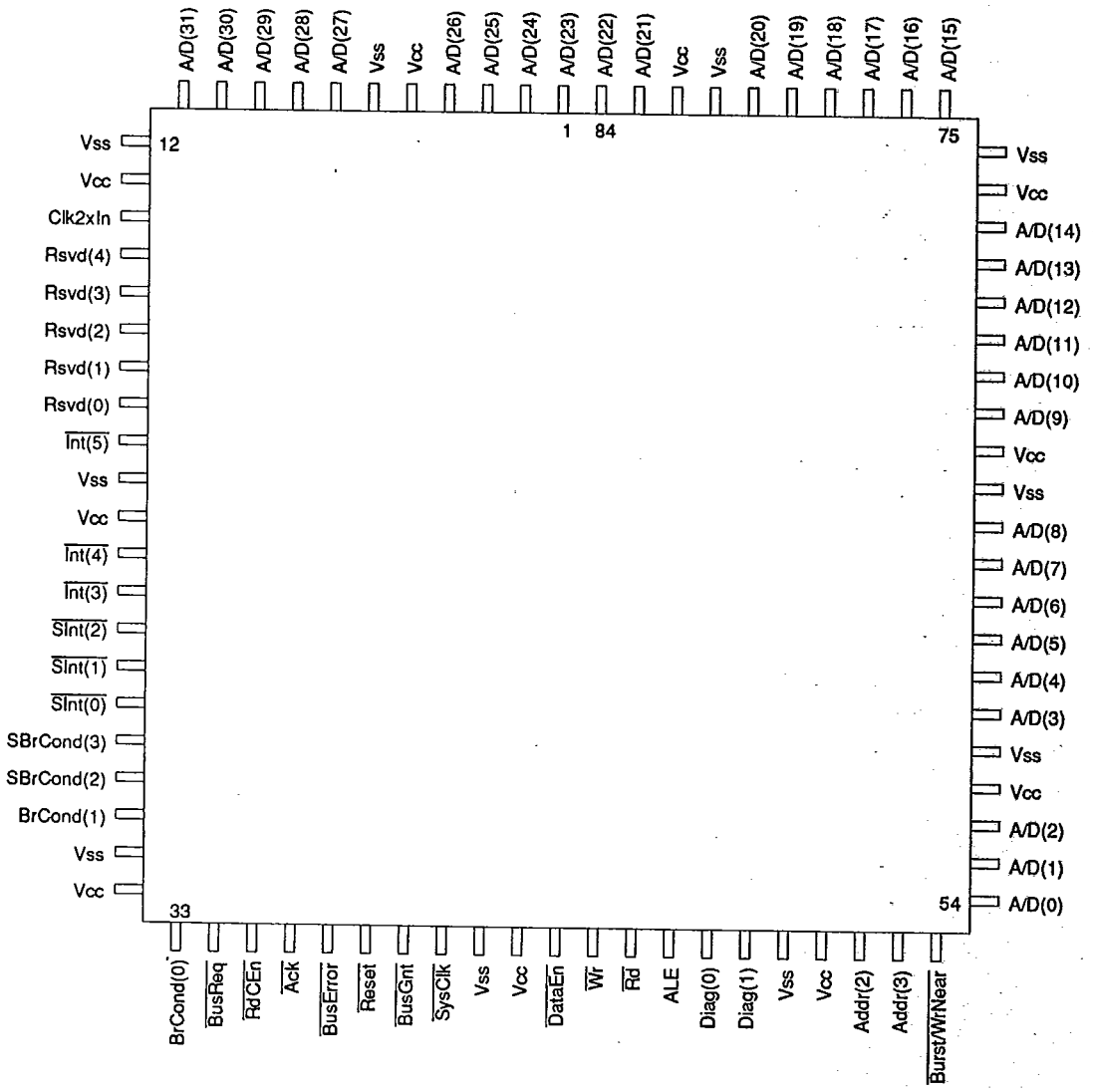
AC ELECTRICAL CHARACTERISTICS (1, 2, 3) — (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{SInt}$, $\overline{RdCEn}$, $\overline{Int}$, BrCond, SBrCond	Set-up to $\overline{SysClk}$ rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to $\overline{SysClk}$ falling	7	—	6	—	5	—	4	—	ns
t2	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{SInt}$, $\overline{RdCEn}$, $\overline{Int}$, BrCond, SBrCond	Hold from $\overline{SysClk}$ rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Tri-state from $\overline{SysClk}$ rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Driven from $\overline{SysClk}$ falling	—	10	—	10	—	10	—	10	ns
t5	$\overline{BusGnt}$	Asserted from $\overline{SysClk}$ rising	—	8	—	7	—	6	—	5	ns
t6	$\overline{BusGnt}$	Negated from $\overline{SysClk}$ falling	—	8	—	7	—	6	—	5	ns
t7	$\overline{Wr}$, $\overline{Rd}$, $\overline{Burst/WrNear}$, A/D	Valid from $\overline{SysClk}$ rising	—	5	—	5	—	4	—	3	ns
t8	ALE	Asserted from $\overline{SysClk}$ rising	—	4	—	4	—	3	—	2	ns
t9	ALE	Negated from $\overline{SysClk}$ falling	—	4	—	4	—	3	—	2	ns
t10	A/D	Hold from ALE negated(4)	2	—	2	—	1.5	—	1.5	—	ns
t11	$\overline{DataEn}$	Asserted from $\overline{SysClk}$ falling	—	15	—	15	—	13	—	12	ns
t12	$\overline{DataEn}$	Asserted from A/D tri-state(4)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{SysClk}$ rising(4)	0	—	0	—	0	—	0	—	ns
t15	$\overline{Wr}$, $\overline{Rd}$, $\overline{DataEn}$, $\overline{Burst/WrNear}$	Negated from $\overline{SysClk}$ falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from $\overline{SysClk}$	—	6	—	6	—	5	—	4	ns
t17	Diag	Valid from $\overline{SysClk}$	—	7	—	7	—	6	—	5	ns
t18	A/D	Tri-state from $\overline{SysClk}$ falling	—	10	—	10	—	9	—	8	ns
t19	A/D	$\overline{SysClk}$ falling to data out	—	10	—	10	—	9	—	8	ns
t20	Clk2xIn	Pulse Width High	10	—	8	—	6.5	—	5	—	ns
t21	Clk2xIn	Pulse Width Low	10	—	8	—	6.5	—	5	—	ns
t22	Clk2xIn	Clock Period	25	—	20	—	15	—	12.5	—	ns
t23	$\overline{Reset}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	$\overline{Reset}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	$\overline{Reset}$	Set-up to $\overline{SysClk}$ falling	6	—	5	—	4	—	3	—	ns
t26	$\overline{Int}$	Mode set-up to $\overline{Reset}$ rising	6	—	5	—	4	—	3	—	ns
t27	$\overline{Int}$	Mode hold from $\overline{Reset}$ rising	2	—	2	—	1	—	1	—	ns
t28	$\overline{SInt}$, SBrCond	Set-up to $\overline{SysClk}$ falling	6	—	5	—	4	—	3	—	ns
t29	$\overline{SInt}$, SBrCond	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	ns
t30	$\overline{Int}$, BrCond	Set-up to $\overline{SysClk}$ falling	6	—	5	—	4	—	3	—	ns
t31	$\overline{Int}$, BrCond	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	ns
tsys	$\overline{SysClk}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	$\overline{SysClk}$	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 1	t22 + 1	t22 - 1	t22 + 1	ns
t33	$\overline{SysClk}$	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 1	t22 + 1	t22 - 1	t22 + 1	ns
tderate	All outputs	Timing deration for loading over 25pf(4, 5)	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

NOTES:
1. All timings referenced to 1.5 Volts.
2. All outputs tested with 25 pF loading.
3. The AC values listed here reference timing diagrams contained in the R3051 Family Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25 pF over the specified test load condition.

PIN CONFIGURATIONS

T-49-17-32



84-Pin PLCC with or without Integral Thermal Slug
Top View

Note:
Reserved Pins must not be connected.

PIN CONFIGURATIONS (CONTINUED)

T-49-17-32

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Clk2xIn	Rsvd (4)	Rsvd (2)	Rsvd (0)	Vss	$\overline{\text{Int}}$ (4)	$\overline{\text{Int}}$ (3)	$\overline{\text{SInt}}$ (1)	S BrCond (3)	S BrCond (2)	BrCond (0)
L	A/D (28)	A/D (30)	Vcc	Rsvd (3)	Rsvd (1)	$\overline{\text{Int}}$ (5)	Vcc	$\overline{\text{SInt}}$ (2)	$\overline{\text{SInt}}$ (0)	BrCond (1)	Vss	$\overline{\text{RdCEn}}$
K	A/D (27)	A/D (29)	A/D (31)							Vcc	$\overline{\text{BusReq}}$	$\overline{\text{Ack}}$
J	Vcc	Vss									$\overline{\text{Bus Error}}$	$\overline{\text{Reset}}$
H	A/D (25)	A/D (26)									$\overline{\text{BusGnt}}$	$\overline{\text{SysClk}}$
G	A/D (23)	A/D (24)									Vcc	Vss
F	A/D (21)	A/D (22)									$\overline{\text{Wr}}$	$\overline{\text{DataEn}}$
E	Vcc	Vss									$\overline{\text{ALE}}$	$\overline{\text{Rd}}$
D	A/D (20)	A/D (19)									Diag (1)	Diag (0)
C	A/D (18)	A/D (16)	Vss							$\overline{\text{Burst}}$/ $\overline{\text{WrNear}}$	Addr (2)	Vss
B	A/D (17)	Vcc	A/D (14)	A/D (11)	A/D (9)	A/D (8)	A/D (6)	A/D (4)	Vss	A/D (1)	Addr (3)	Vcc
A	A/D (15)	A/D (13)	A/D (12)	A/D (10)	Vcc	Vss	A/D (7)	A/D (5)	A/D (3)	Vcc	A/D (2)	A/D (0)

R3051
84-Pin Ceramic Pin Grid Array
(Cavity Down)

Bottom View

84-Pin PGA with Integral Thermal Slug
BottomView

Note:
Reserved Pins must not be connected.

T-49-17-32

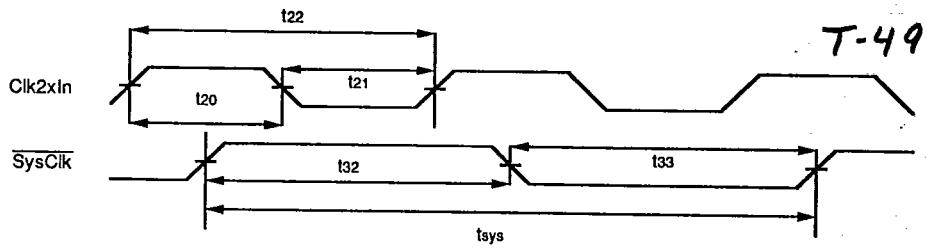


Figure 8. R3051 Family Clocking

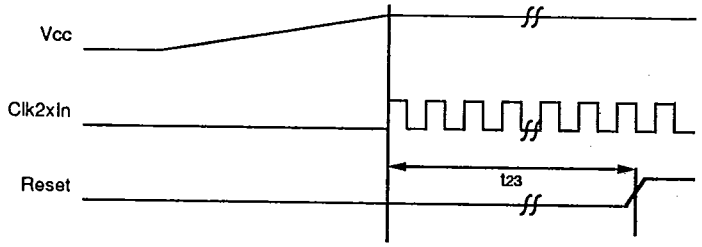


Figure 9. Power-On Reset Sequence

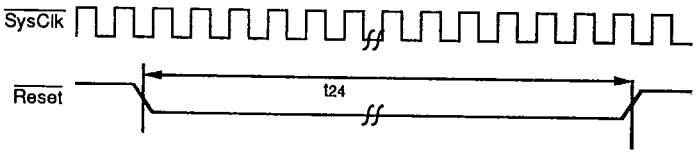


Figure 10. Warm Reset Sequence

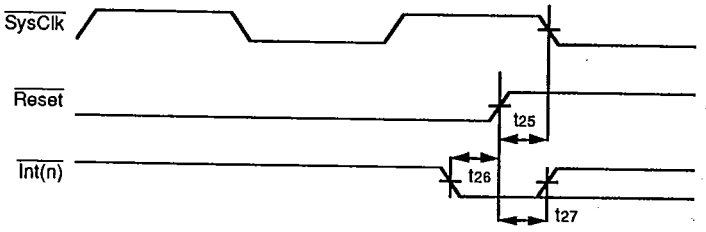


Figure 11. Mode Selection and Negation of Reset

T-49-17-32

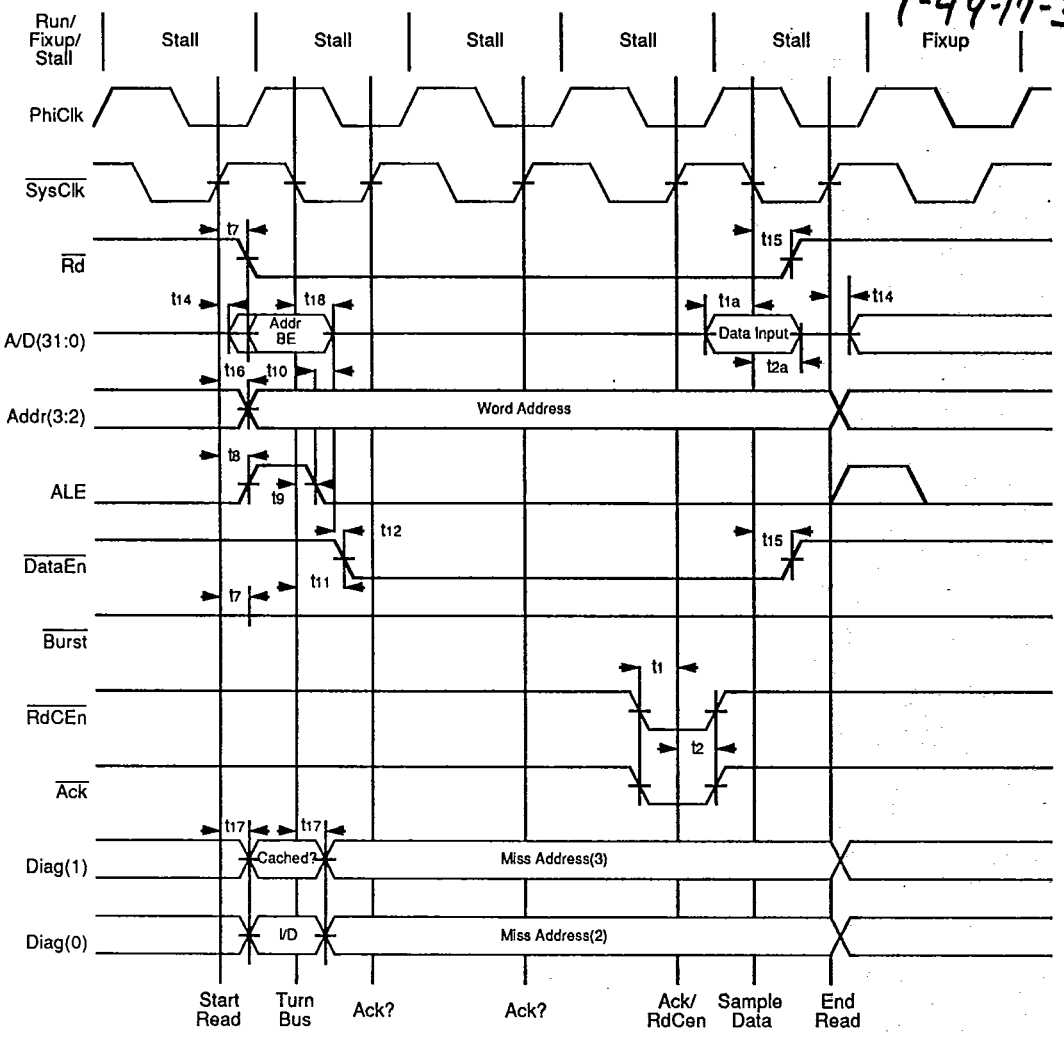


Figure 12. Single Datum Read In R3051 Family

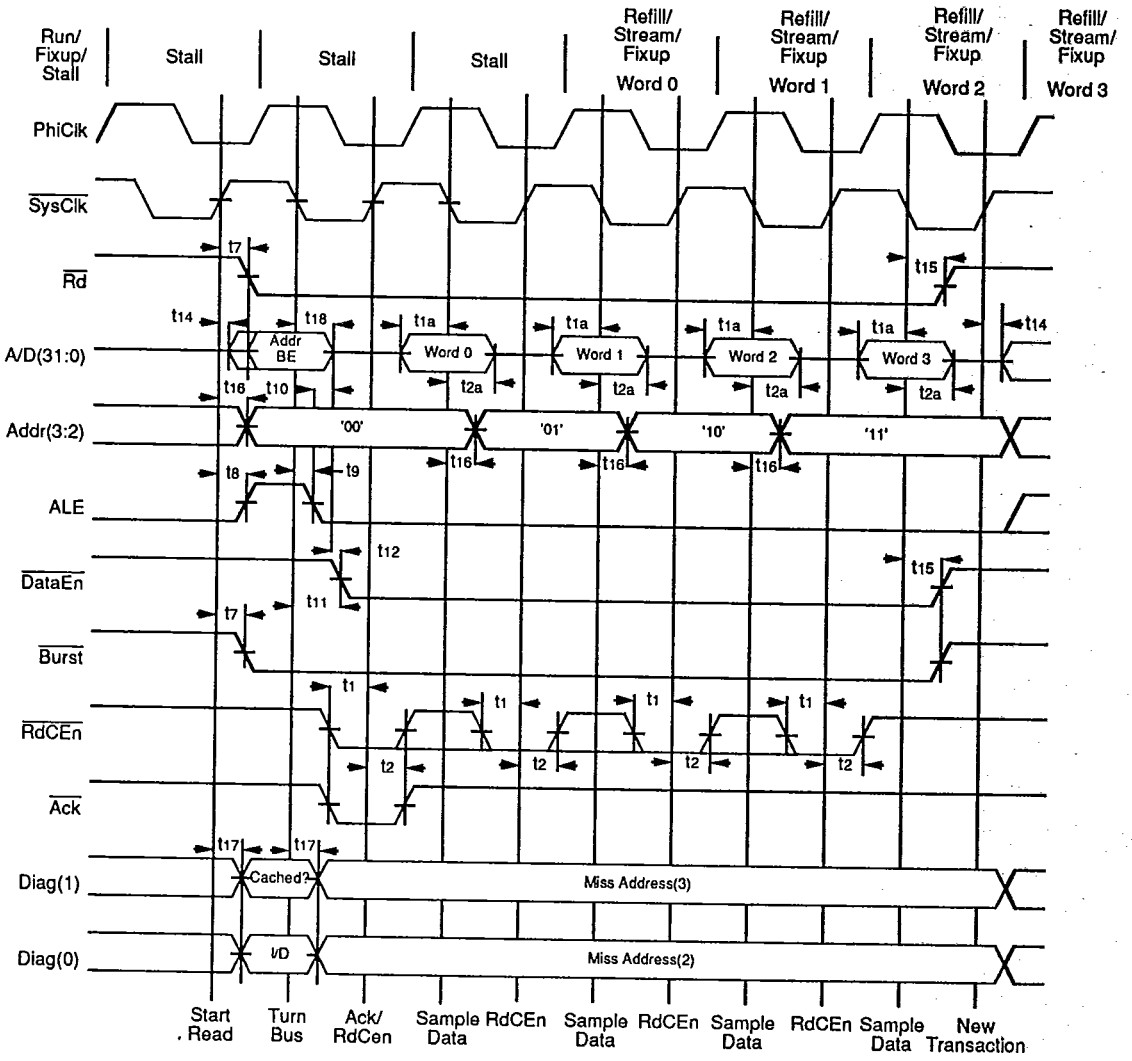


Figure 13. R3051 Family Burst Read

T-49-17-32

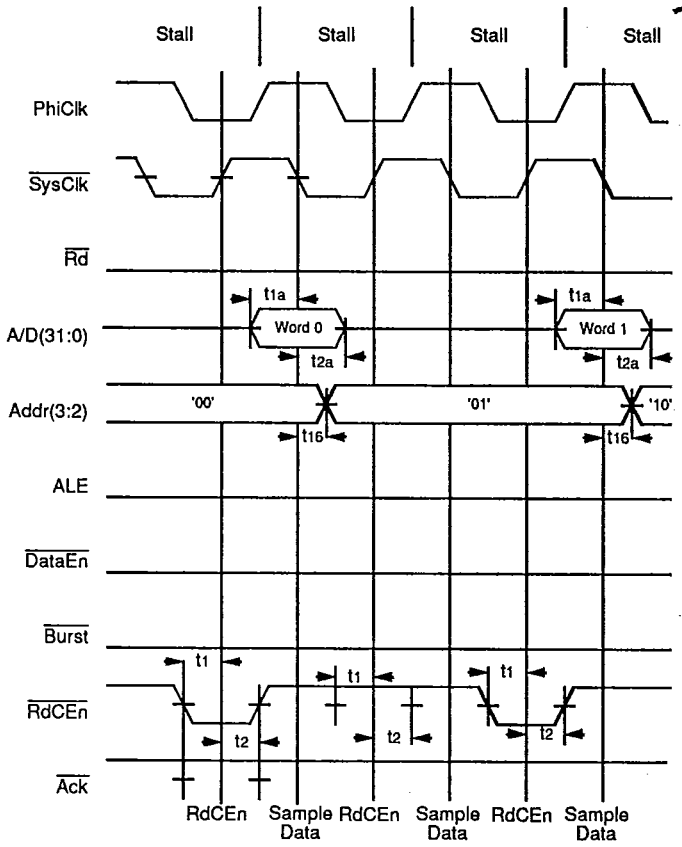


Figure 14 (a). Start of Throttled Quad Read

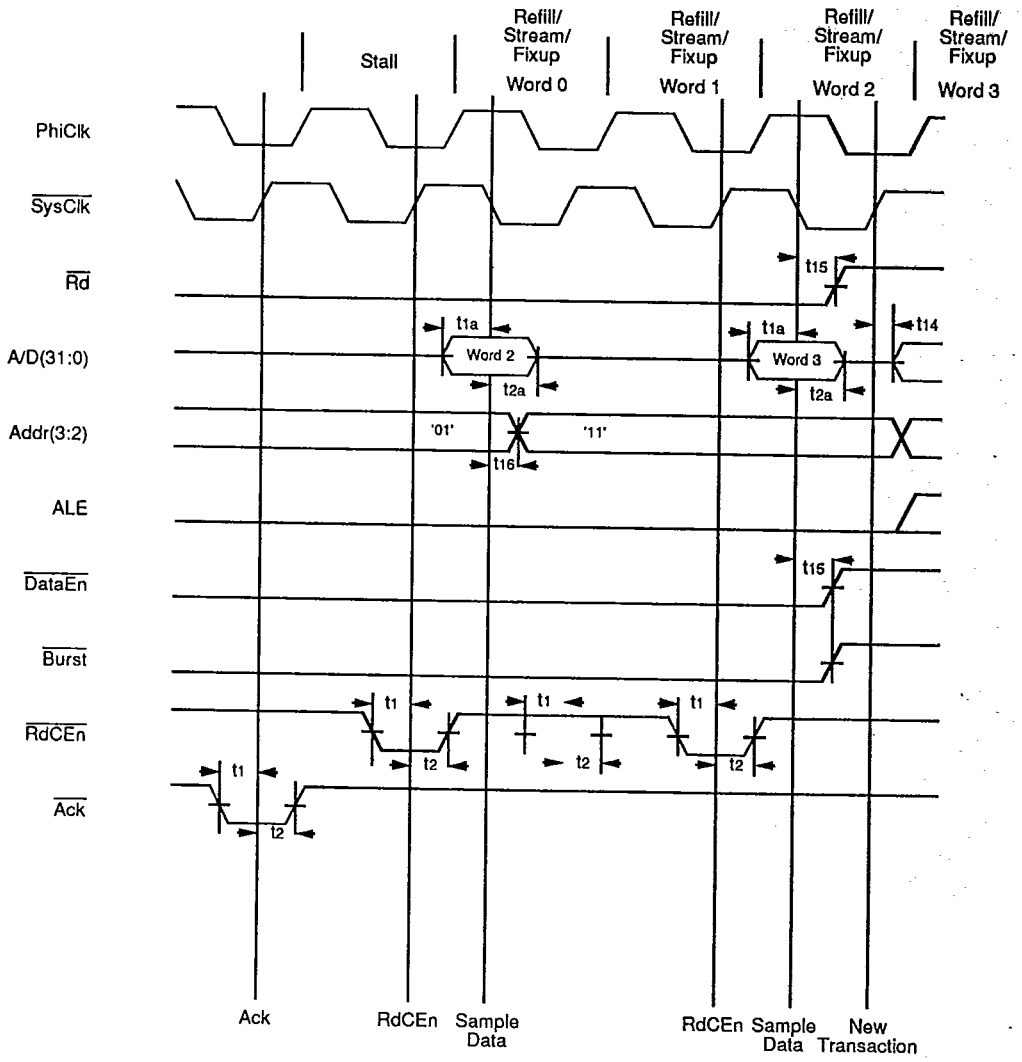


Figure 14 (b). End of Throttled Quad Read

T-49-17-32

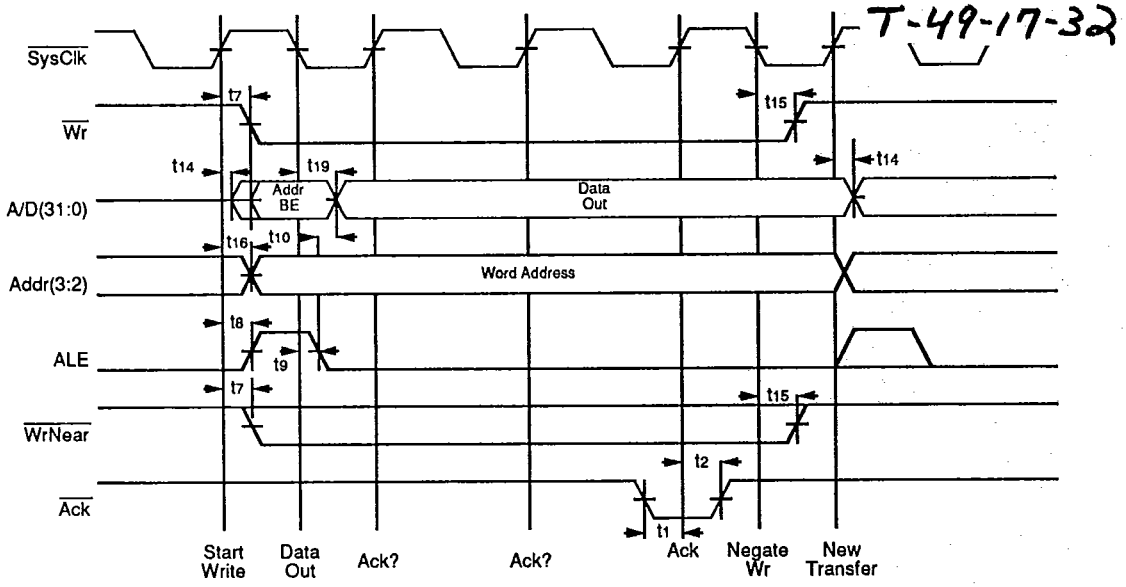


Figure 15. R3051 Family Write Cycle

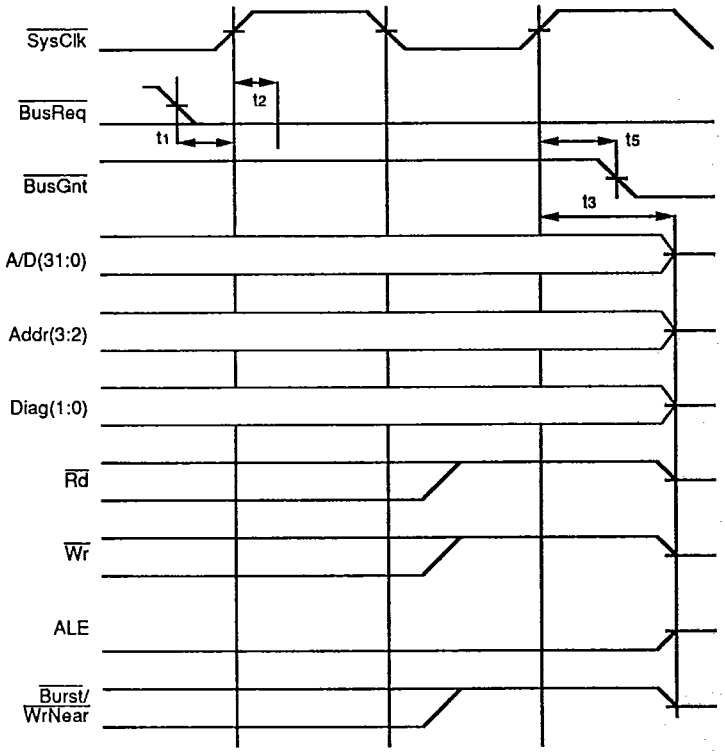


Figure 16. Request and Relinquish of R3051 Family Bus to External Master

T-49-17-32

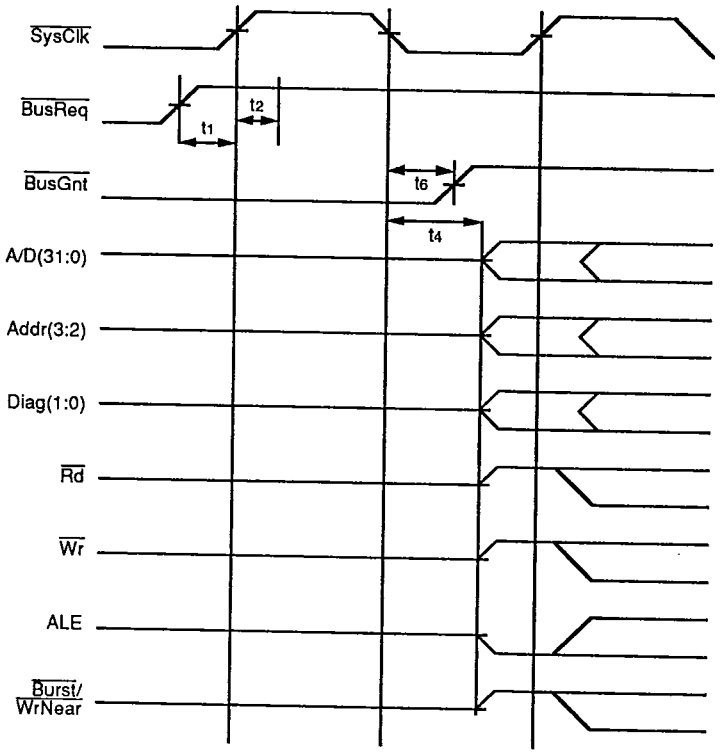


Figure 17. R3051 Family Regaining Bus Mastership

C

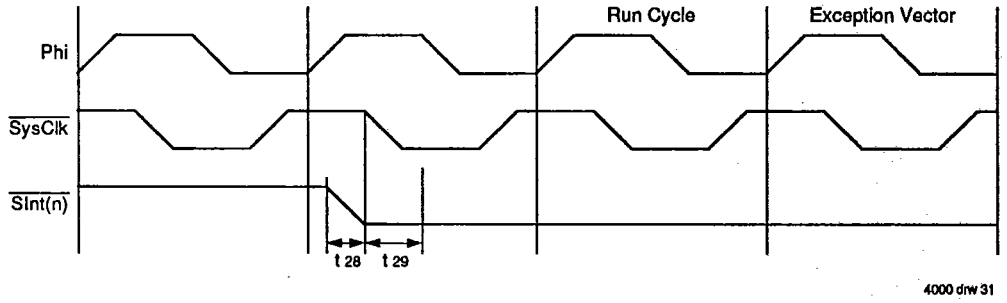


Figure 18. Synchronized Interrupt Input Timing

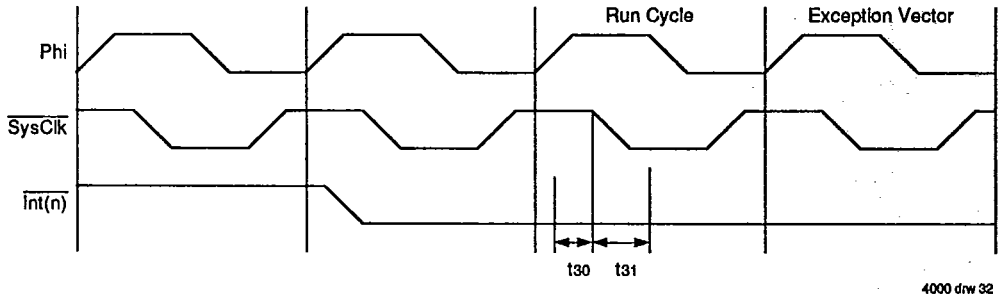


Figure 19. Direct Interrupt Input Timing

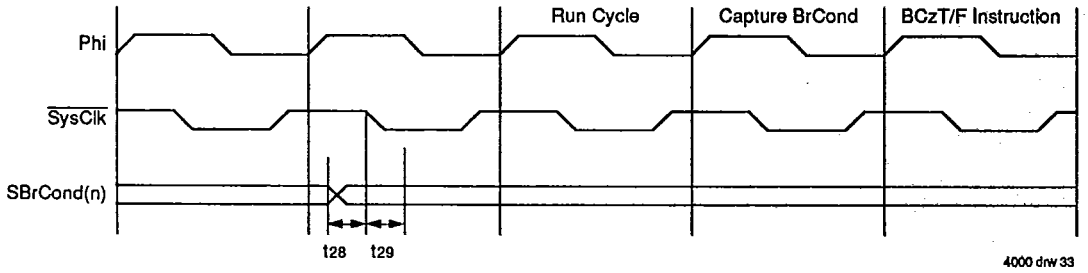


Figure 20. Synchronized Branch Condition Input Timing

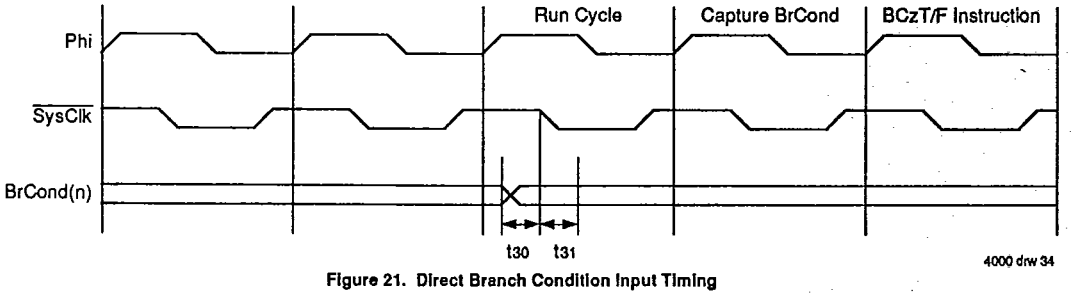
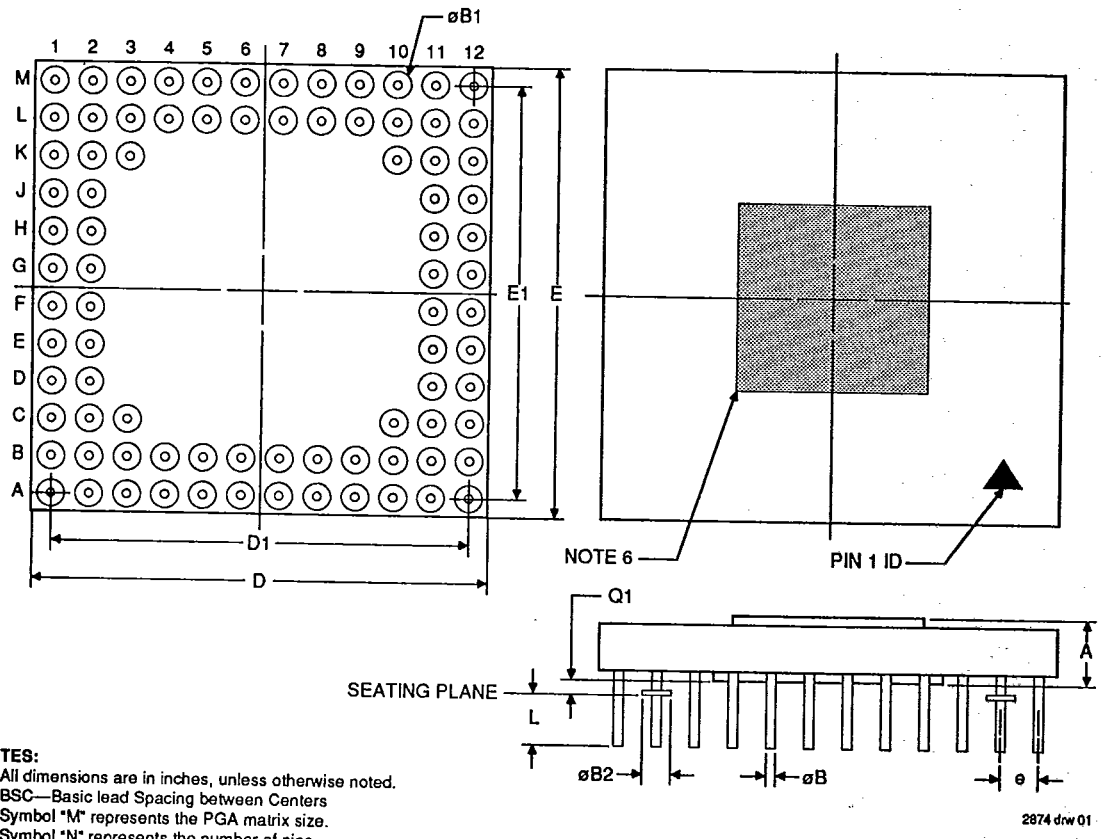


Figure 21. Direct Branch Condition Input Timing

84-PIN PGA (CAVITY DOWN)

T-49-17-32



2874 drw 01

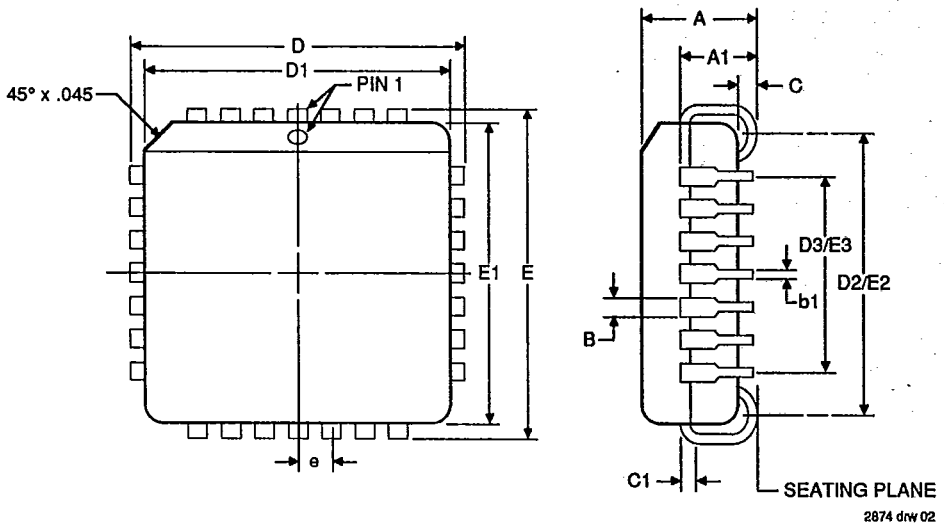
NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers
3. Symbol "M" represents the PGA matrix size.
4. Symbol "N" represents the number of pins.
5. Chamfered corners are IDT's option.
6. Shaded area indicates integral metallic heat sink.

Drawing #	G84-4	
Symbol	Min	Max
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
N	84	
Q1	.025	.060

C

T-49-17-32

84 LEAD PLCC (SQUARE)



2874 drw 02

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.

DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
Cl	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

ORDERING INFORMATION

T-49-17-32

IDT XXXXX - XX X X

Device Type	Speed	Package	Process/ Temp. Range	
			Blank	Commercial Temperature Range
			'B'	Compliant to MIL-STD-883, Class B
			'M'	Military Temperature Range Only
		'J'		84-Pin PLCC
		'PH'		84-Pin PLCC with Integral Thermal Slug
		'G'		84-Pin PGA with Integral Thermal Slug
	'20'			20.0 MHz
	'25'			25.0 MHz
	'33'			33.33 MHz
	'40'			40.0 MHz
79R3051				4kB Instruction Cache, No TLB
79R3051E				4kB Instruction Cache, With TLB
79R3052				8kB Instruction Cache, No TLB
79R3052E				8kB Instruction Cache, With TLB

VALID COMBINATIONS

IDT	79R3051 - 20, 25	All packages
	79R3051E - 20, 25	All packages
	79R3052 - 20, 25	All packages
	79R3052E - 20, 25	All packages
	79R3051 - 33, 40	PGA, PH Packages Only
	79R3051E - 33, 40	PGA, PH Packages Only
	79R3052 - 33, 40	PGA, PH Packages Only
	79R3052E - 33, 40	PGA, PH Packages Only

C