

FEATURES

- ❑ 4K x 4 Static RAM with Separate I/O, Transparent Write (L7C171), or High Impedance Write (L7C172)
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 8 ns maximum
- ❑ Low Power Operation
 - Active: 190 mW typical at 35 ns
 - Standby: 100 μ W typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ Plug Compatible with IDT 71681/71682, Cypress CY7C171/172
- ❑ Package Styles Available:
 - 24-pin Plastic DIP
 - 24-pin Sidebrazed, Hermetic DIP
 - 24-pin CerDIP
 - 28-pin Ceramic LCC

DESCRIPTION

The L7C171 and L7C172 are high-performance, low-power CMOS static RAMs. The storage cells are organized as 4096 words by 4 bits per word. Data In and Data Out are separate. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 190 mW (typical) when operating at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write

accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C171 and L7C172 consume only 15 μ W (typical) at 3 V, allowing effective battery backup operation.

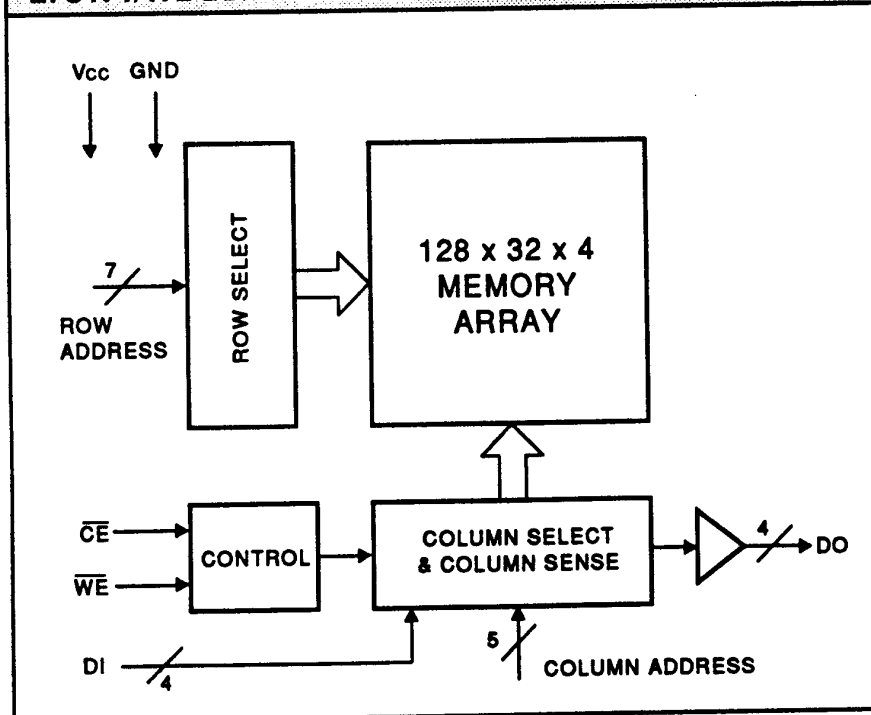
The L7C171 and L7C172 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output bus simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A11. Reading from a designated location is accomplished by presenting an address and driving $\overline{\text{CE}}$ low while $\overline{\text{WE}}$ remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{\text{WE}}$ is low (L7C172 only) or $\overline{\text{CE}}$ is high.

Writing to an addressed location is accomplished when the active-low $\overline{\text{CE}}$ and $\overline{\text{WE}}$ inputs are both low. Either signal may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C171 and L7C172 can withstand an injection current of up to 200 mA on any pin without damage.

L7C171/172 BLOCK DIAGRAM



MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V _{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V _{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V _{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V _{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V _{CC} ≤ 5.5 V

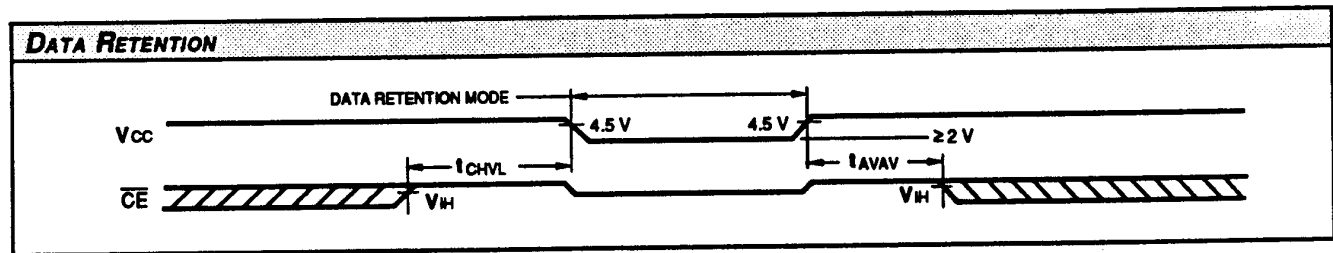
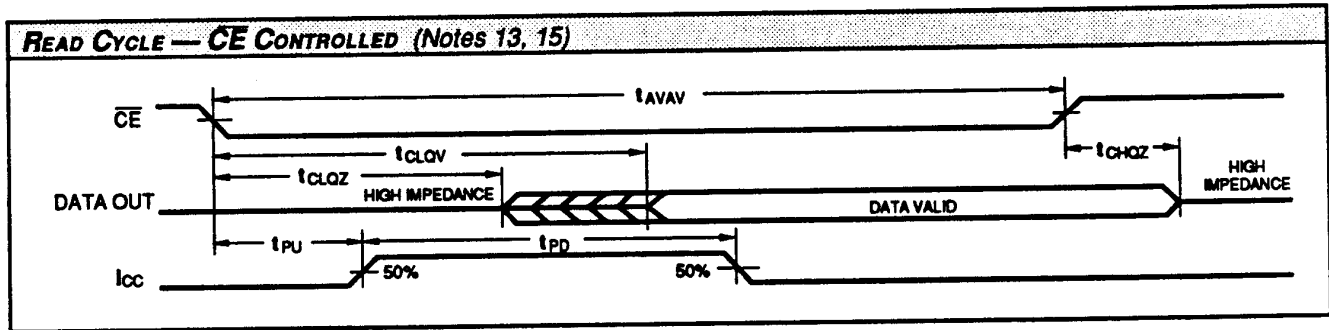
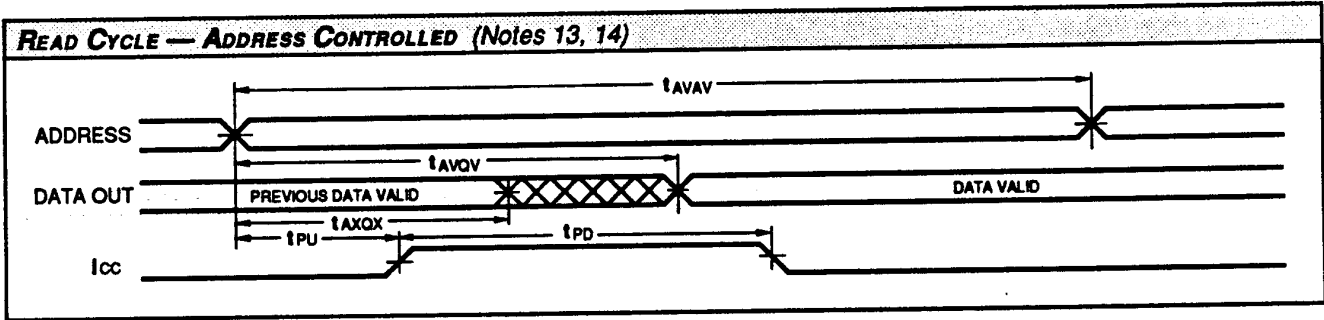
ELECTRICAL CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	I _{OH} = –4.0 mA, V _{CC} = 4.5 V	2.4			V
V _{OL}	Output Low Voltage	I _{OL} = 8.0 mA			0.4	V
V _{IH}	Input High Voltage		2.0		V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I _{Ix}	Input Current	GND ≤ V _{IN} ≤ V _{CC}	–10		+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , \overline{CE} = V _{CC}	–10		+10	μA
I _{OS}	Output Short Current	V _{OUT} = GND, V _{CC} = Max (Note 4)			–350	mA
I _{CC2}	V _{CC} Current, TTL Inactive	(Notes 5, 7)		15	30	mA
I _{CC3}	V _{CC} Current, CMOS Standby	(Note 8)		20	100	μA
I _{CC4}	V _{CC} Current, Data Retention	V _{CC} = 3.0 V (Note 9)		5	50	μA
C _{IN}	Input Capacitance	Ambient Temp = 25°C, V _{CC} = 5.0 V			5	pF
C _{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

Symbol	Parameter	Test Condition	L7C171/172-							Unit
			35	25	20	15	12	10	8	
I _{CC1}	V _{CC} Current, Active	Notes 5, 6	50	70	90	110	120	130	165	mA

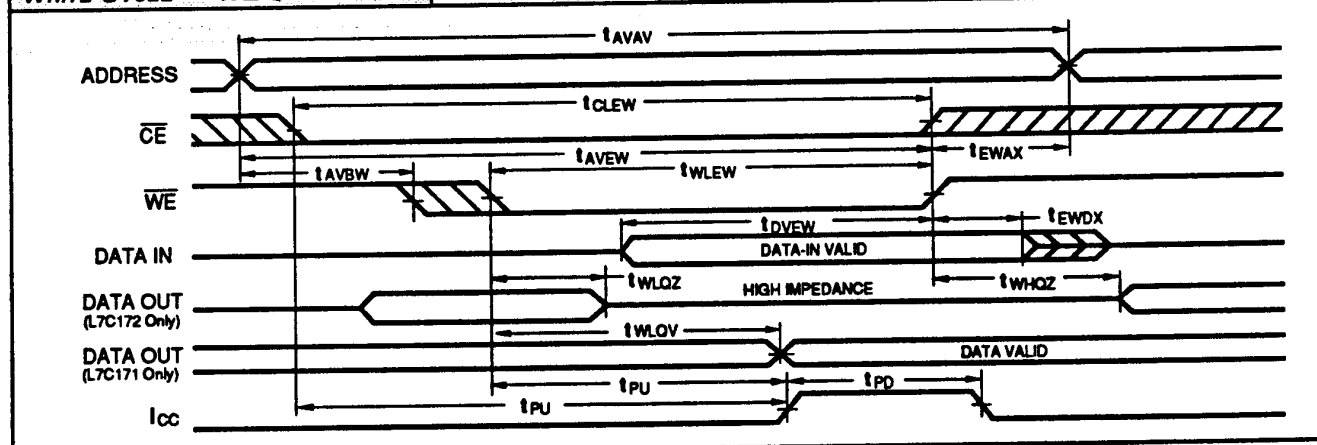
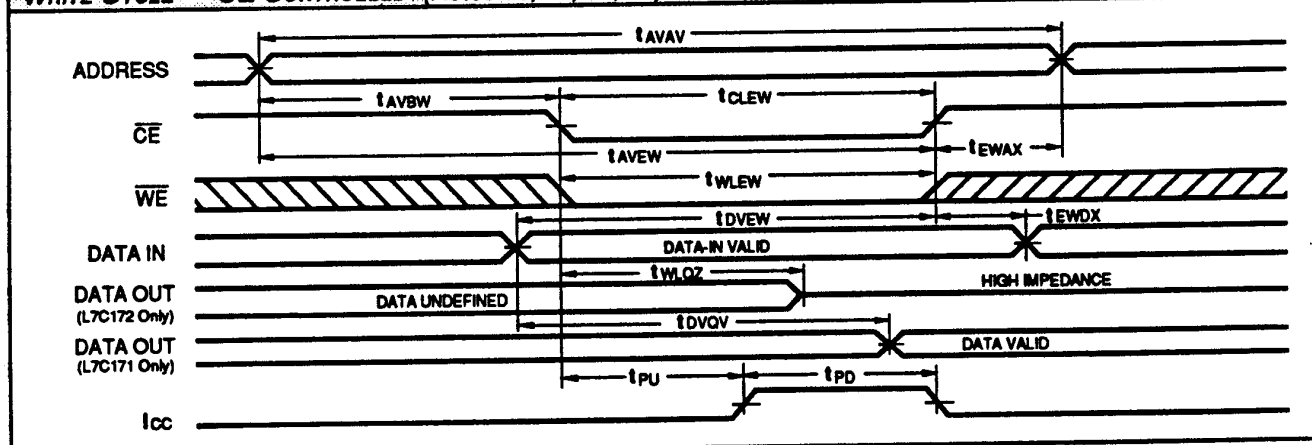
SWITCHING CHARACTERISTICS Over Operating Range (ns)

READ CYCLE (Notes 11, 12, 22, 23, 24)		L7C171/172-													
Symbol	Parameter	35		25		20		15		12		10		8	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12		10		8	
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
tAXQX	Address Change to Output Change	3		3		3		3		3		3		3	
tCLOV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
tCLOZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
tCHOZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
tpD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	



SWITCHING CHARACTERISTICS Over Operating Range (ns)**WRITE CYCLE** (Notes 11, 12, 22, 23, 24)

Symbol Parameter		L7C171/172-													
		35		25		20		15		12		10		8	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8	
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
twLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
tdVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
teWDX	End of Write Cycle to Data Change	0		0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
twLOZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3
twLOV	Write Enable Low to Output Valid		30		20		15		15		12		10		8
tdVOV	Data Valid to Output Valid		30		20		15		15		12		10		8

WRITE CYCLE — WE CONTROLLED (Notes 16, 17, 18, 19)**WRITE CYCLE — CE CONTROLLED** (Notes 16, 17, 18, 19)

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at -0.6 V. A current in excess of 100 mA is required to reach -2 V. The device can withstand indefinite operation with inputs as low as -3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of $+5.0$ V, an ambient temperature of $+25^{\circ}\text{C}$ and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{\text{CE}} \leq \text{VIL}$, $\overline{\text{WE}} \geq \text{VIH}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{\text{CE}} \geq \text{VIH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{\text{CE}} = \text{VCC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{\text{CE}}$ must be $\geq \text{VCC} - 0.2$ V. For all other inputs $\text{VIN} \geq \text{VCC} - 0.2$ V or $\text{VIN} \leq 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and

IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{\text{WE}}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{\text{CE}}$ low).

15. All address lines are valid prior to or coincident with the $\overline{\text{CE}}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{\text{CE}}$ low and $\overline{\text{WE}}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{\text{WE}}$ goes low before or concurrent with $\overline{\text{CE}}$ going low, the output remains in a high impedance state.

18. If $\overline{\text{CE}}$ goes high before or concurrent with $\overline{\text{WE}}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

- Falling edge of $\overline{\text{CE}}$.
- Falling edge of $\overline{\text{WE}}$ ($\overline{\text{CE}}$ active).
- Transition on any address line ($\overline{\text{CE}}$ active).
- Transition on any data line ($\overline{\text{CE}}$ and $\overline{\text{WE}}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ± 200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

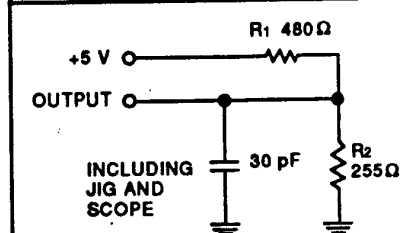


FIGURE 1b.

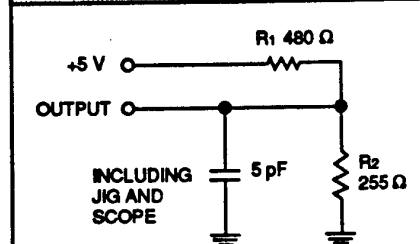
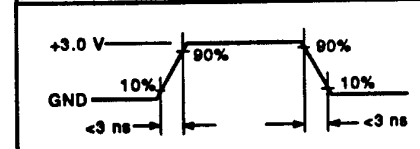


FIGURE 2.



LOGIC

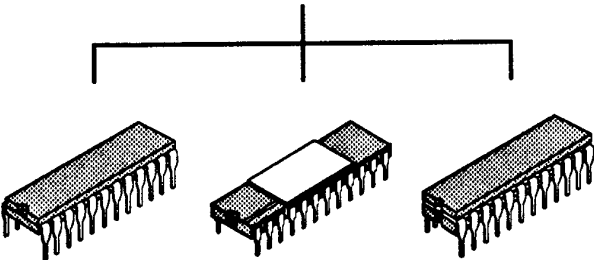
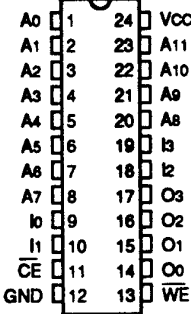
DEVICES INCORPORATED

Memory Products

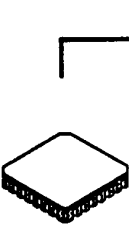
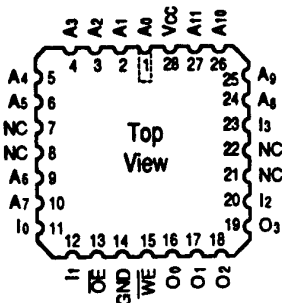
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ORDERING INFORMATION

24-pin
(0.3" wide)



28-pin
(450 x 450)



Speed	Plastic DIP (P2)	Sidebrazed Hermetic DIP (D2)	CerDIP (C1)	Ceramic Leadless Chip Carrier (K1)		
0°C to +70°C — COMMERCIAL SCREENING						
35 ns	L7C171PC or L7C172PC	L7C171DC or L7C172DC	L7C171CC or L7C172CC	L7C171KC or L7C172KC		
25 ns						
20 ns						
15 ns						
12 ns						
10 ns						
8 ns						
-55°C to +125°C — COMMERCIAL SCREENING						
35 ns		L7C171DM or L7C172DM	L7C171DM or L7C172DM	L7C171KM or L7C172KM		
25 ns						
20 ns						
15 ns						
12 ns						
10 ns						
8 ns						
-55°C to +125°C — EXTENDED SCREENING						
35 ns		L7C171DME or L7C172DME	L7C171DME or L7C172DME	L7C171KME or L7C172KME		
25 ns						
20 ns						
15 ns						
12 ns						
10 ns						
8 ns						
-55°C to +125°C — MIL-STD-883 COMPLIANT						
35 ns		L7C171DMB or L7C172DMB	L7C171DMB or L7C172DMB	L7C171KMB or L7C172KMB		
25 ns						
20 ns						
15 ns						
12 ns						
10 ns						
8 ns						