YAMAHA LSI

YSD221

DIT3

Digital audio Interface Transmitter 3

■ OUTLINE

YSD221(DIT3) is an LSI which outputs the digital sound signals as digital audio interface (DIF) signals that conform to EIAJ CP-340 and AES/EBU.It also has a function of multiplexing with DIF signals from the CD signal processing LSI.

Use of YSD221 in combination with YM7110(LVFM) enables sound signals from the multi-disc player to be fully digitized, peripheral circuits to be reduced, sound signals to be switched and bilingual processed as well.

■ FEATURES

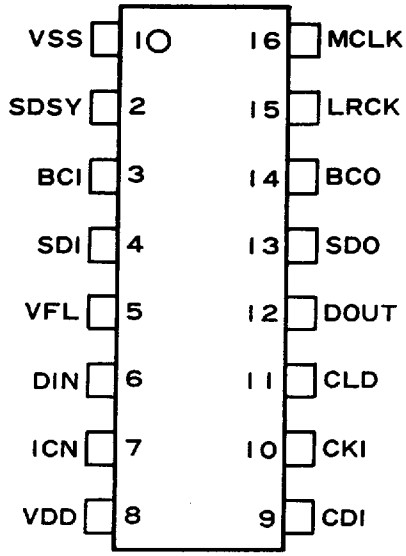
- Synchronous operation with the external clock (384fs) inputted into the MCLK terminal.
- Capable of accepting synchronized DIF signals in addition to the digital sound signals.
- Useable for bilingual discs as any input channel signals can be switched to the output channel.
- Outputs input signals as bi-phase signal.
- Also outputs signals to the digital filter, etc.
- First 32 bit of the channel status can be set through microprocessor.
- 5V single power supply, Si-gate CMOS process.
- 16 pin SOP or 16 pin DIP.

YAMAHA CORPORATION

9945524 0002723 3T6

YSS221 CATALOG
CATALOG No. : LSI-4SD221A2
1996. 5

■ PIN CONFIGURATION



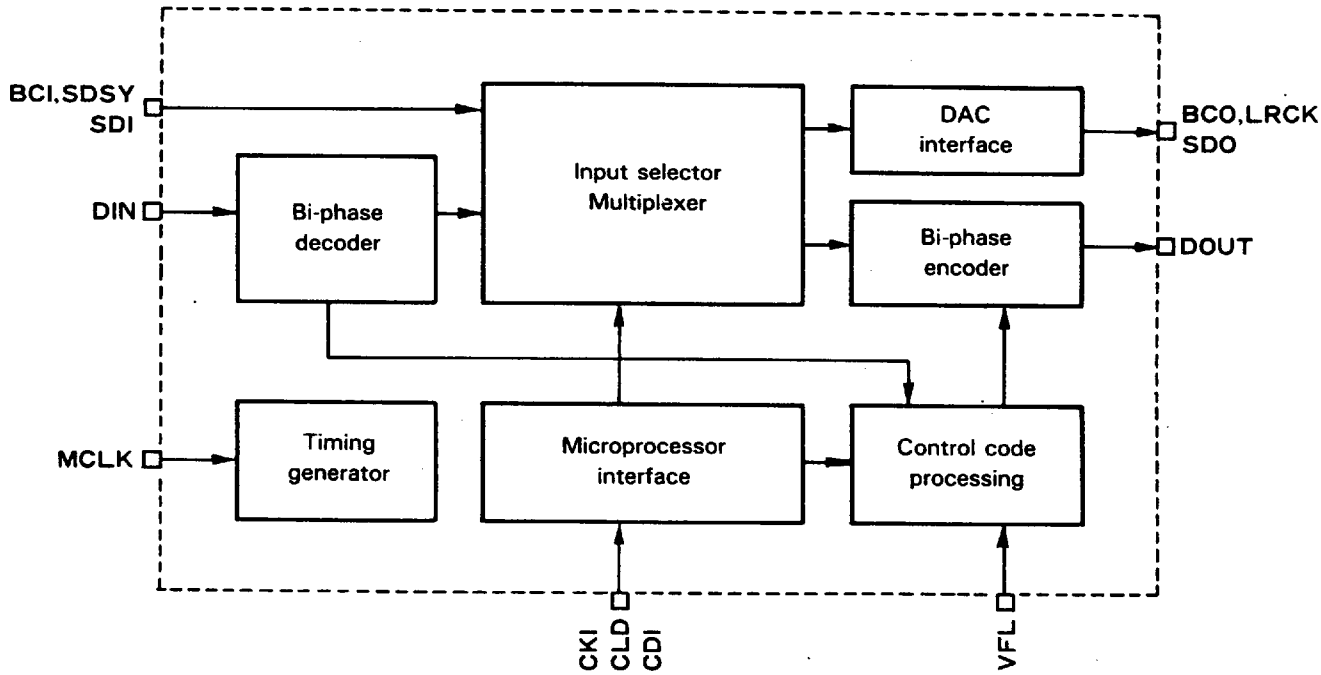
<16 SOP, 16 DIP Top View>

■ PIN DESCRIPTION

No.	Name	I/O	Function	
1	VSS		GND	
2	SDSY	I+	Digital sound signal input	Word clock
3	BCI	I+		Bit clock
4	SDI	I+		Serial data
5	VFL	I−		Validity flag data
6	DIN	I+	Synchronized digital audio interface signal input	
7	ICN	I+	Initial clear input	
8	VDD		+5V power supply	
9	CDI	I	Microprocessor interface	Serial data input
10	CKI	I		Clock input
11	CLD	I		Load input
12	DOUT	O	Digital audio interface signal output	
13	SDO	O	Digital sound signal output	Serial data
14	BCO	O		Bit clock
15	LRCK	O		L/R clock
16	MCLK	I	Master clock input (384fs)	

(Note) I+: Input terminal with pull-up resistor
I−: Input terminal with pull-down resistor

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

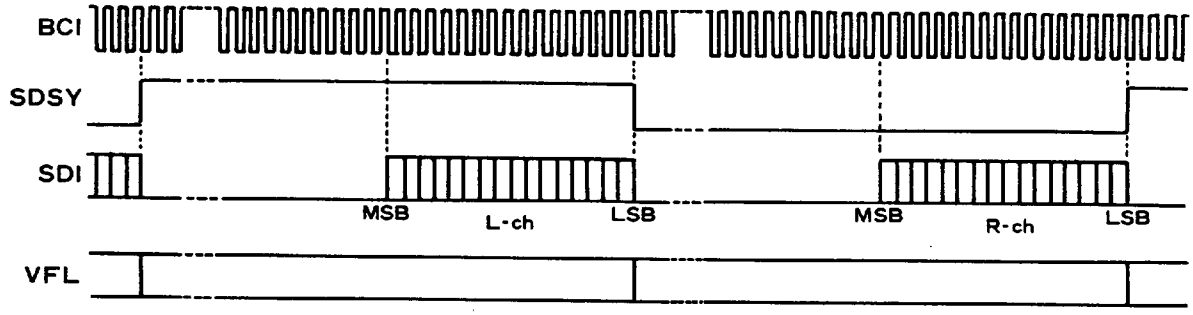
1. Master clock MCLK

Inputs 384fs master clock to MCLK pin.

2. Data input DIN, BCI, SDSY, SDI, VFL

Digital sound signals are inputted through each pin of BCI, SDSY, SDI and VFL.
The input format is set through the microprocessor.
Interface with YM7110(LVFM) is also available.

<DIGITAL SOUND INPUT FORMAT (when LVFM='0')>



- The acceptable sound data length is 16 bit.
- BCI, SDSY, SDI and VFL must be synchronized with MCLK.
- BCI must be one of 32fs, 48fs, 64fs, 96fs, 128fs and 192fs.

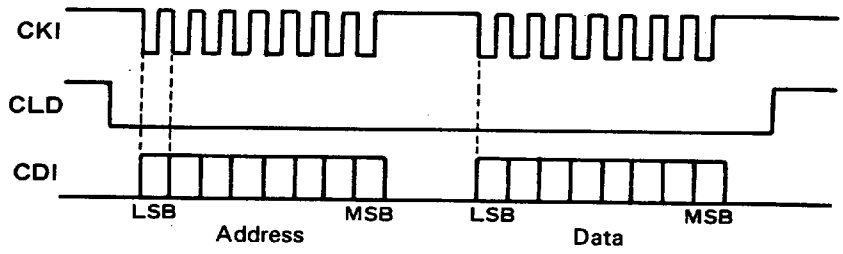
DIF signal is inputted through DIN pin by making use of the output of CD signal processing LSI, etc. 24 bit data including AUX bit and the control code can be accepted.
When inputting the DIF signal, it must be synchronized with the MCLK clock.

3. Microprocessor interface CLD, CKI, CDI

Setting multiplex of the input signal and channel status 32 bit should be done by sending the serial data in the format shown below through the microprocessor interface

3-1. Data format

Send the register address and setting data as a set.



3-2. Register map

ADDR		LSB	b1	b2	b3	b4	b5	b6	MSB
0	Output setting	LVFM	—	—	—	—	—	—	TEST
1		DIF	DAON	DION	—	CMOD	UMOD	VMOD	—
2		DA L		DA R		DI L		DI R	
3	Channel status First 32 bit setting data	0	Control					0	0
4		Category code							
5		Source No.				Channel No.			
6		Sampling frequency				Clock accuracy		0	0

LVFM: Setting digital sound input format

0: Digital sound format <default>
1: YM7110(LVFM) format

TEST: LSI test

Always set to '0'.

DIF: Setting DIF signal output

0: Output OFF (DOUT='L')
1: Output ON <default>

DAON: Setting digital sound output

0: Output OFF (SDO MUTE) <default>
1: Output ON

DION: Setting DIF signal output

0: Output OFF (Audio data mute)

1: Output ON <default>

CMOD: Setting channel status output mode

0: Microprocessor setting data output (same for L and R, first 32 bit each and all '0' after this) <default>

1: Data inputted from DIN is copied and output (L and R, 192 bit each)

UMOD: Setting user data output mode

0: All '0' output <default>

1: Data inputted from DIN is copied and output (192 bit *2)

VMOD: Setting validity flag output mode

0: '0' output all the time

1: Data inputted from VFL (when SDI is selected) or DIN (when DIF is selected) is copied and output <default>

DA L, DA R: Setting digital sound output multiplex

DA L selects digital sound output to L channel and DA R selects output data to R channel

DA L		Signal output to digital sound output L channel
LSB	b1	
0	0	Digital sound input L channel
1	0	Digital sound input R channel
0	1	DIF signal input L channel
1	1	DIF signal input R channel

default value is (LSB, b1)=(0, 0)

DA R		Signal output to digital sound output R channel
b2	b3	
0	0	Digital sound input L channel
1	0	Digital sound input R channel
0	1	DIF signal input L channel
1	1	DIF signal input R channel

Initial value is (b2, b3)=(0, 0)

DI L, DI R: Setting DIF signal output multiplex

DI L selects DIF signal output to L channel and DI R selects output data to R channel

DI L		Signal output to DIF signal output L channel
b4	b5	
0	0	Digital sound input L channel
1	0	Digital sound input R channel
0	1	DIF signal input L channel
1	1	DIF signal input R channel

default value is (b4, b5)=(0, 0)

DI R		Signal output to DIF signal output R channel
b6	MSB	
0	0	Digital sound input L channel
1	0	Digital sound input R channel
0	1	DIF signal input L channel
1	1	DIF signal input R channel

Initial value is (b6, MSB)=(1, 0)

Channel status 32 bit:

Set data as the first 32 bit of channel status.

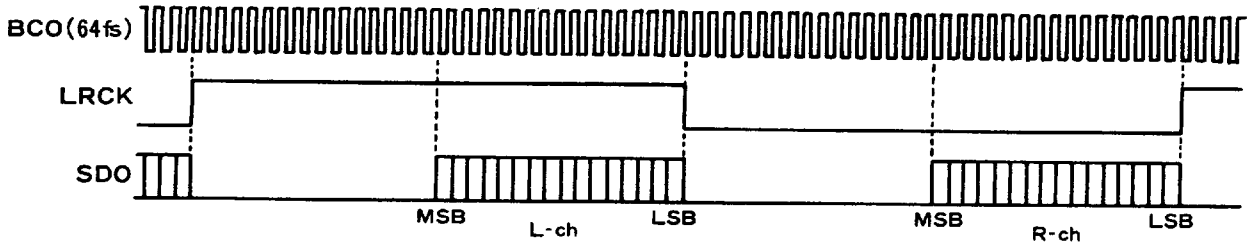
The data, as set, is output to both L and R channels from the immediately following preamble 'B' frame.

The initial value is all '0'.

4. Data output DOUT, BCO, LRCK, SDO

The audio data and control code are output through DOUT pin after bi-pahse modulation. If DIF signal is selected, 24 bit including the AUX bit is output. Also, the digital sound data is output in the following format through BCO, LRCK and SDO terminals.

<DIGITAL SOUND OUTPUT FORMAT>



- The sound data length is 16 bit regardless of the input signal

5. System reset ICN

This LSI requires initial clear operation when the power is turned ON.

After the clock is fed, set the ICN pin to 'L' for 32 or more cycles of the sampling frequency.

While the ICN pin is 'L', DOUT output becomes 'L'.

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{op}	0 ~ 70	°C
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{op}	0	25	70	°C

3. DC characteristics

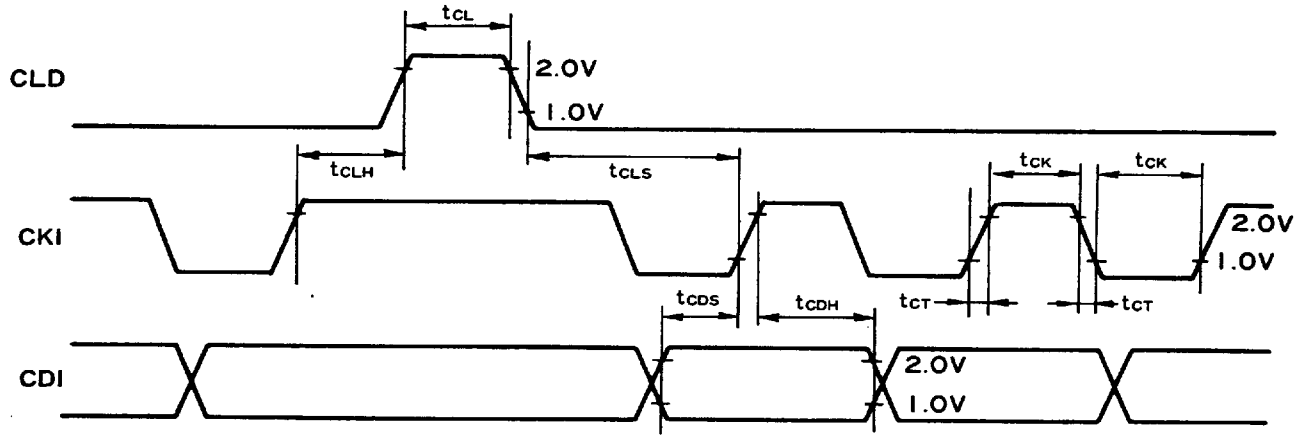
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}				10	mA
Input voltage H level (1)	V_{IH1}	*1	2.2			V
Input voltage L level (1)	V_{IL1}	*1			0.8	V
Input voltage H level (2)	V_{IH2}	*2	3.5			V
Input voltage L level (2)	V_{IL2}	*2			1.5	V
Input leakage current	I_{LK}	*3	−10		10	μA
Pull-up, pull-down resistance	RP	*4	60		600	kΩ
Output voltage H level	V_{OH}	I_{OH} = −0.4mA, *5	4.0			V
Output voltage L level	V_{OL}	I_{OL} = 1.0mA, *5			0.4	V
Input capacitance	C_I	f = 1MHz			8	pF

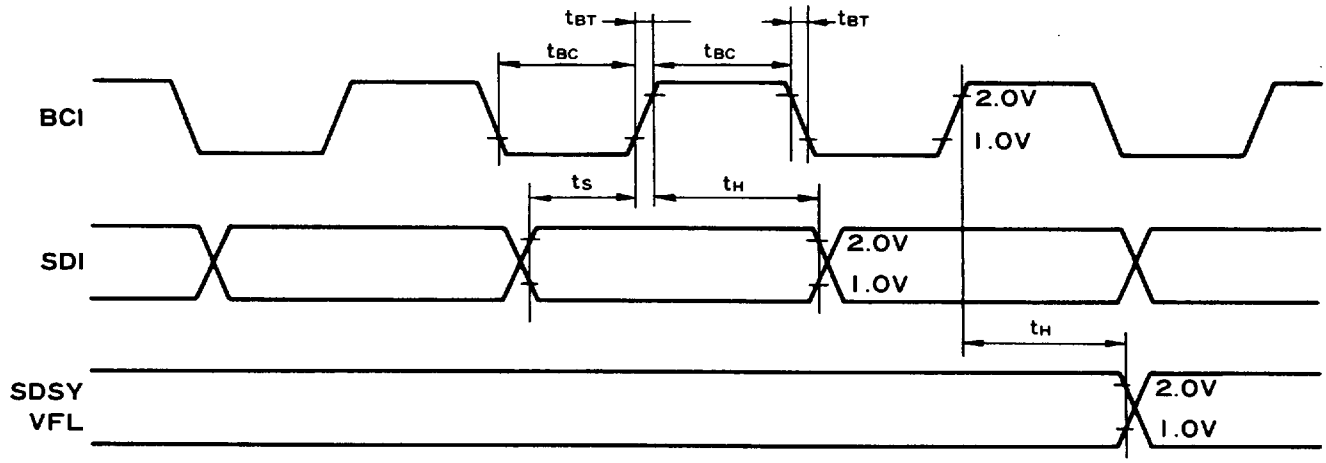
*1) Applicable to input pins except for ICN.
*2) Applicable to ICN pin.
*3) Applicable to CDI, CKI, CLD and MCLK pins.
*4) Applicable to SDSY, BCI, SDI, VFL, DIN and ICN pins.
*5) Applicable to all output pins.

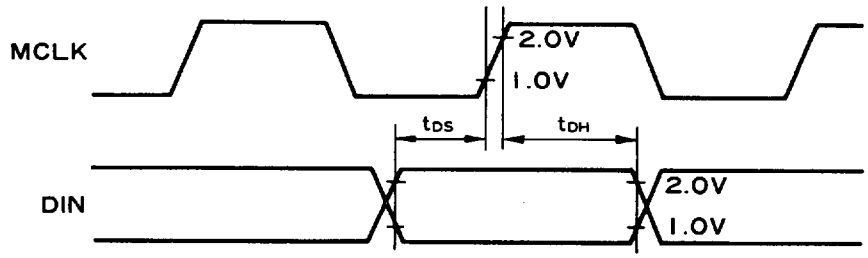
4. AC characteristics

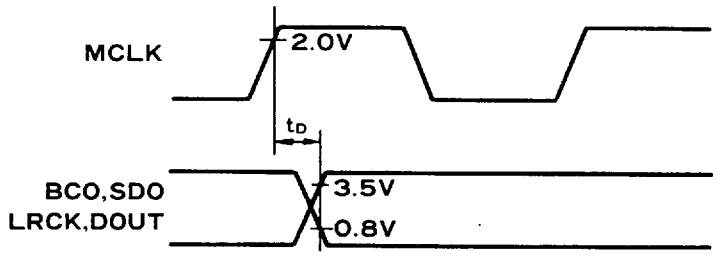
Parameter			Symbol	Min.	Typ.	Max.	Unit
MCLK	frequency		f_M	12.2		18.5	MHz
	Duty		D_M	40	50	60	%
CDI	Setup time		t_{CDS}	20			ns
	Hold time		t_{CDH}	20			ns
CKI	ON/OFF time		t_{CK}	40			ns
	Transition time		t_{CT}			50	ns
CLD	Setup time		t_{CLS}	40			ns
	Hold time		t_{CLH}	0			ns
CLD	ON time		t_{CL}	14/f_M			ns
SDI	Setup time		t_S	20			ns
	Hold time		t_H	20			ns
BCI	ON/OFF time		t_{BC}	40			ns
	Transition time		t_{BT}			50	ns
DIF	Setup time	*1	t_{DS}	20			ns
	Hold time	*1	t_{DH}	20			ns
BCO, LRCK, SDO, DOUT		*2					
	Delay time		t_D			80	ns

*1) Either t_{DS} or t_{DH} may be less than its Min. value but not both of them at the same time.
*2) Load capacitance : 100pF or less



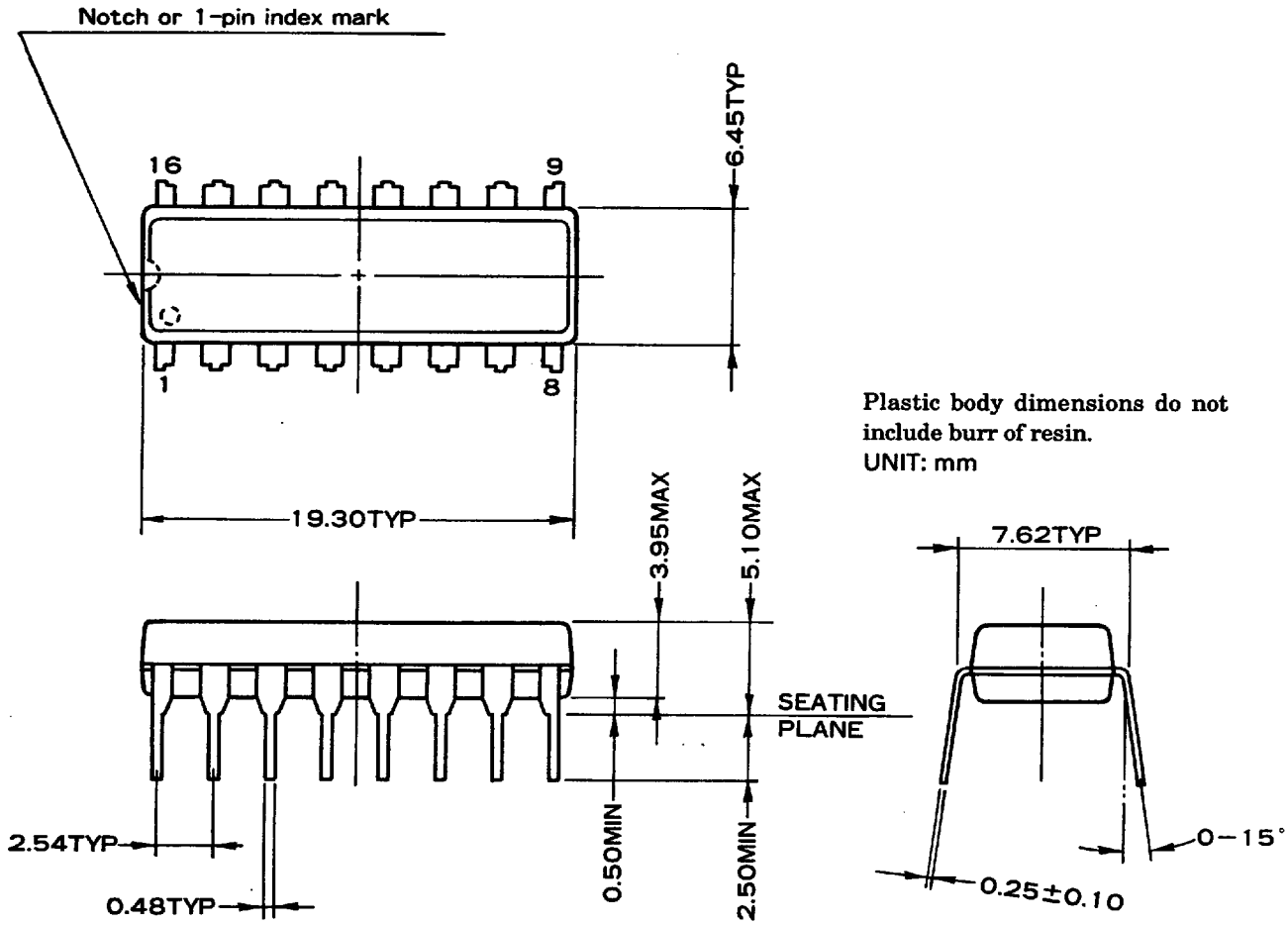




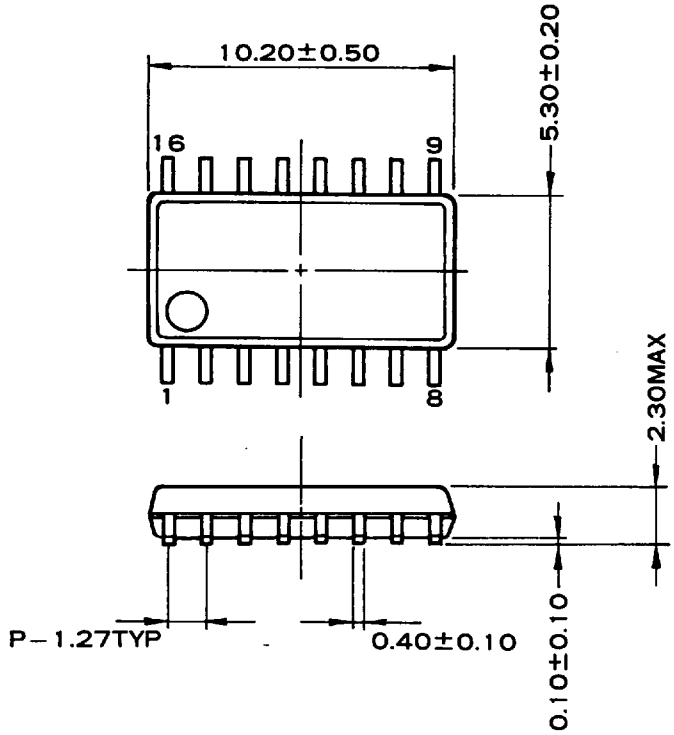


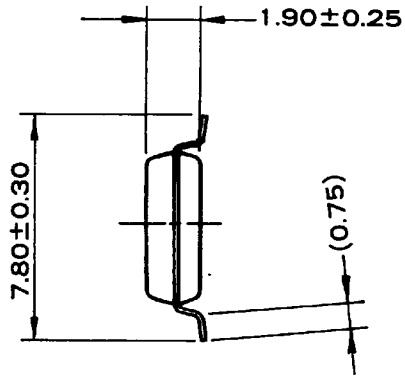
■ EXTERNAL DIMENSIONS

● YSD221-D



Plastic body dimensions do not include burr of resin.
UNIT: mm





Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.