Microchip

Military

28C256

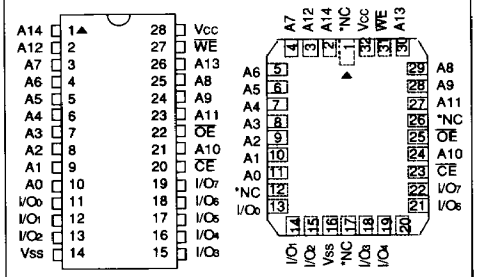
256K (32K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast read access time—90, 120, 150 ns maximum
- CMOS Technology for low power dissipation
  - —80 mA active
  - —350 µA standby
- Fast byte-write time—3 ms or 10 ms
- Fast page-write-time—3 ms or 10 ms
- Data retention >10 years
- High endurance 10^4 erase/write cycles
- Automatic write operation
  - —Internal control timer
  - —Auto-clear before write operation
  - —On-chip address and data latches
- Data polling
- Chip clear operation
- Enhanced data protection
  - —VCC detector
  - —Power-up timer
- Electronic signature for device identification
- 5-volt-only operation
- Organized 32K x 8 JEDEC standard pinout
  - —28-pin Dual In-line Package (DIP)
  - —32-pin Leadless Chip Carrier (LCC)
- Extended Temperature Range:
  - —Military (B): -55°C to +125°C

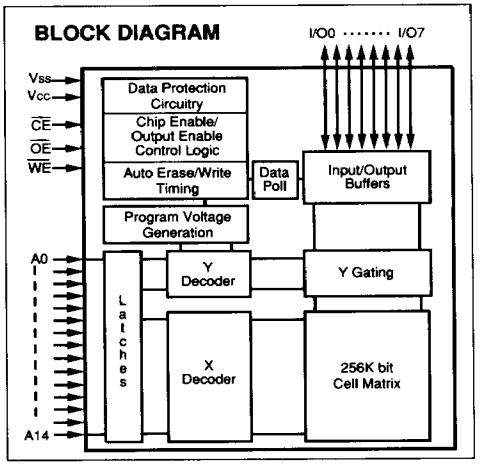
PIN CONFIGURATION

Top View



▲ Pin 1 indicator on PLCC on top of package
* NC (No Connect)

BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 28C256 high speed, low power page mode 32,768 x 8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with Microchip's advanced and reliable non-volatile CMOS technology.

The 28C256 is accessed like a static RAM for the read or write cycles without the need of external components. During a "write" the address and 1 to 64 bytes of data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear the addressed memory cells and write the latched data using an internal control timer.

The completion of a write cycle is detected by either DATA polling of output I/O7 or TOGGLE BIT of I/O6.

Data protection is achieved with Vcc sensing, an additional 5 ms (typical) delay after power on, and a software write protection scheme. Furthermore, holding $\overline{OE}$ Low, $\overline{CE}$ high or $\overline{WE}$ high inhibits writing to the device.

The 28C256 also provides two useful software controlled features; Software Chip Clear and Software Write Protection. The feature of Software Chip Clear allows users to erase the whole memory with 5 V only power supply. Software Write Protection sets a non-volatile fuse to protect the memory from inadvertent writes.

The 28C256 operates from a single 5 V supply and is packaged in standard JEDEC-approved packages. All necessary programming voltages are internally generated and timed.

The advanced CMOS technology offers fast access times of 90 ns (28C256-90) at low power dissipation of 80 mA. When the chip is deselected, the standby current is less than 350 µA.

PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5 V
Vss	Ground
NC	No Connect

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc and input voltages w.r.t. Vss .....-0.3 V to + 6.25 V
Voltage on $\overline{OE}$ w.r.t. Vss .....-0.3 V to +15 V
Voltage on A9 w.r.t. Vss .....-0.3 V to +15 V
Output voltage w.r.t. .....-0.6 V +Vcc +0.6 V
Ambient temp. with power supplies .....-55°C to 125°C
Storage temperature .....-65°C to 150°C

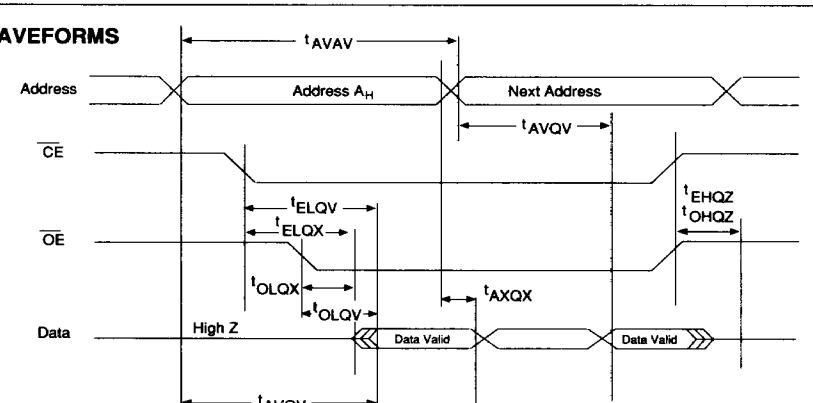
*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ/WRITE OPERATION
DC Characteristics

Vcc = +5 V ± 10%
Military (B): TAMB = -55°C to +125°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc + 0.3 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = 0.1 V to Vcc + 1
Input Capacitance		CI		10	pF	VIN = 0 V; TAMB = 25°C; f = 1 MHz; Vcc = 5.0 V
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -4 mA IOL = 6 mA
Output Leakage		ILO	-10	10	µA	VOUT = 0.1 V to Vcc
Output Capacitance		CO		10	pF	VIN = 0 V; TAMB = 25°C; f = 1 MHz, Vcc = 5.0 V
Power Supply Current, Active	TTL Input	ICC1		80	mA	f = 1TAVAV (min) Vcc = 5.5 V; $\overline{OE}$ = $\overline{CE}$ = VIL, VIH = 2.0 V to Vcc
Power Supply Current, Standby	TTL Input CMOS Input	ICCa ICC(s)3		3 350	mA µA	$\overline{CE}$ = VIH $\overline{CE}$ = Vcc ± 0.3 V

READ WAVEFORMS



READ OPERATION AC Characteristics

AC Testing Waveform: V_{IH} = 2.4 V; V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: ≤ 10 ns
Ambient Temperature: Military (B): T_{AMB} = -55°C to 125°C
Measurement Reference Levels: Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V

Parameter	Symbol	28C256 -15		28C256 -12		28C256 -90		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	150	-	120	-	90	-	ns
Address Access Time	TAVAV (1)	-	150	-	120	-	90	ns
Chip Enable Access Time	TELAV (2)	-	150	-	120	-	90	ns
Output Enable Access Time	TOLAV	-	80	-	50	-	40	ns
$\overline{CE}$ Enable to output in Low Z $\overline{OE}$ Enable to output in Low Z	TELAX TOLAX	10	-	10	-	10	-	ns
$\overline{CE}$ Disable to output in High Z $\overline{OE}$ Enable to output in High Z	TEHQZ TOHAZ	-	60	-	50	-	40	-
Output Hold from Address Changes	TAXAX	0	-	0	-	0	-	-

Notes:(1) $\overline{OE}$ can be delayed up to (TAVAV - TOLAV) after the address the valid without impact on TAVQV.
(2) $\overline{OE}$ can be delayed up to (TELAV - TOLAV) after the falling edge of $\overline{CE}$ without impact on TELAV.

DEVICE OPERATION

The Microchip Technology Inc. 28C256 has five basic modes of operation—read, standby, page or byte write, write inhibit and chip clear —as outlined in the following table.

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X(1)	X	High Z
Write (2)				
- Byte/Page	⏦(4)	V_{IH}	⏦	D_{IN}
Write Inhibit	X	V_{IL}	X	High Z/D_{OUT}
Write Inhibit	V_{IH}	X	X	High Z
Write Inhibit	X	X	V_{IH}	High Z/D_{OUT}
Chip Clear (3)	V_{IL}	V_H (5)	⏦	High Z

Notes: (1) X = any TTL level
(2) Refer to "Programming Waveforms"
(3) Refer to "Chip Clear Waveforms"
(4) ⏦ = Low going pulse
(5) V_H = 12V ± 5%

Read Mode

The 28C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

Standby Mode

The 28C256 is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Hardware Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions. The following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.8 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip. In addition, upon power-up an internal timer (5ms typical) will inhibit the recognition of any program operation. During this period, all normal read functions will be operational. After both the VCC detection and the internal timer have elapsed, normal programming operation can be performed.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 20ns duration from initiating a write cycle.

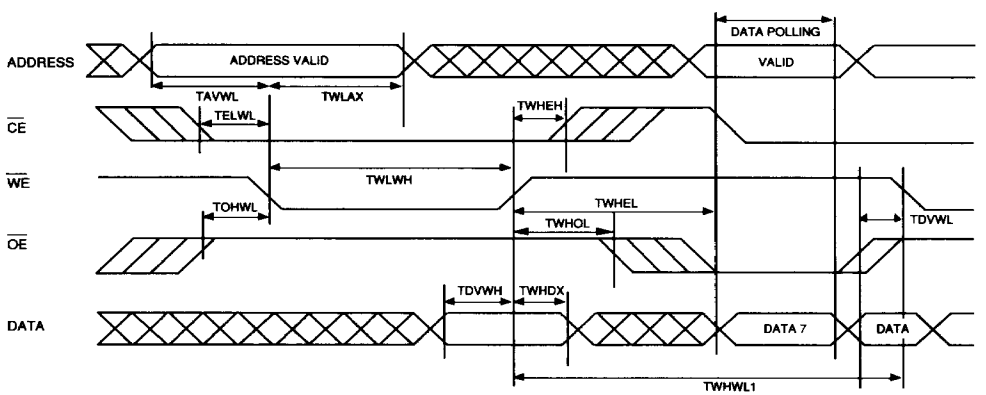
Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

WRITE OPERATION AC Characteristics

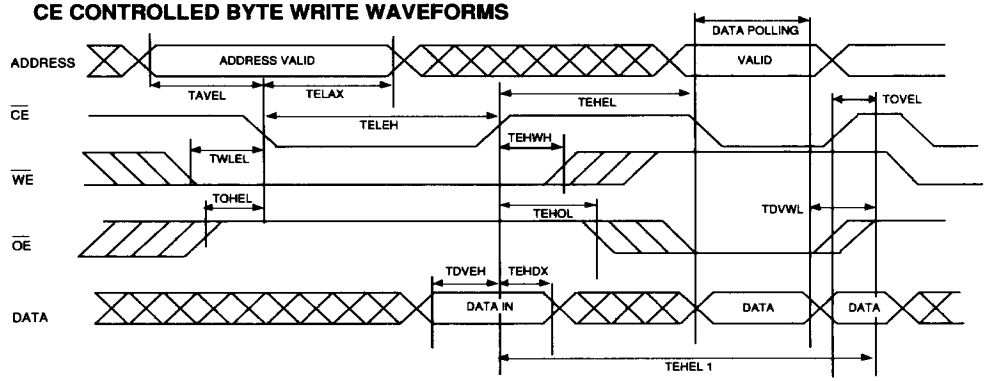
AC Testing Waveform: V_{IH} = 2.4 V; V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: ≤10 ns
Ambient Temperature: Military (B): TAMB = -55°C to 125°C
Measurement Reference Levels: Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-up Time	TAVWL TAVEL	0	-	ns	-
Data Set-up Time	TDVWH TDVEH	50	-	ns	-
Address Hold Time	TWLAX TELAX	50	-	ns	-
Data Hold Time	TWHDX TEHDX	0	-	ns	-
Write Pulse Width	TWLWH TELEH	150	-	ns	-
$\overline{OE}$ Set-up Time	TOHWL TOHEL	0	-	ns	-
$\overline{OE}$ Hold Time	TWHOL TEHOL	0	-	ns	-
Time to Data Polling	TWHEL TEHEL	-	0	ns	-
Delay to Next Write	TOVWL TOVEL	0	-	ns	-
Write Cycle Time	TWHWL1 TEHEL1	-	3, 10	ms	1, 3 ms Typical
Byte A Cycle	TWHWL2 TEHEL2	0.2	149	µs	For page mode
Write Set-up Time	TELWL TWLEL	0	-	ns	-
Write Hold Time	TWHEH TEHWH	0	-	ns	-

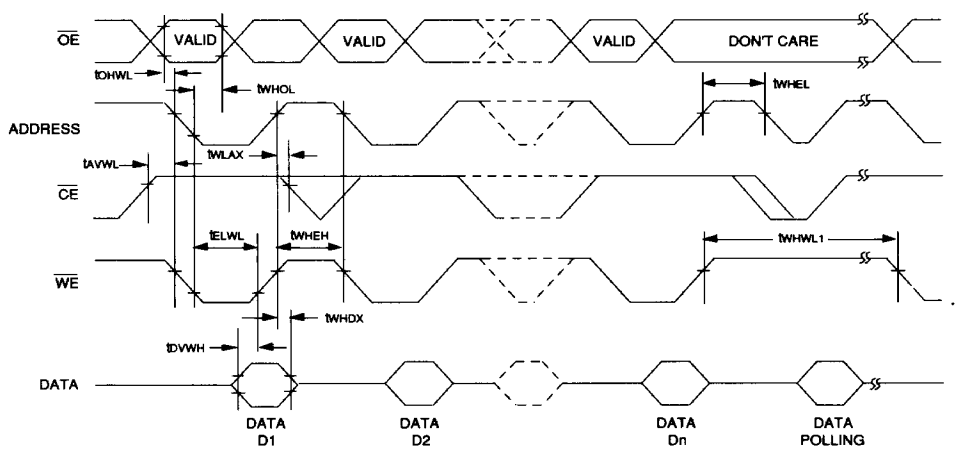
$\overline{WE}$ CONTROLLED BYTE WRITE WAVEFORMS



$\overline{CE}$ CONTROLLED BYTE WRITE WAVEFORMS



PAGE WRITE WAVEFORMS

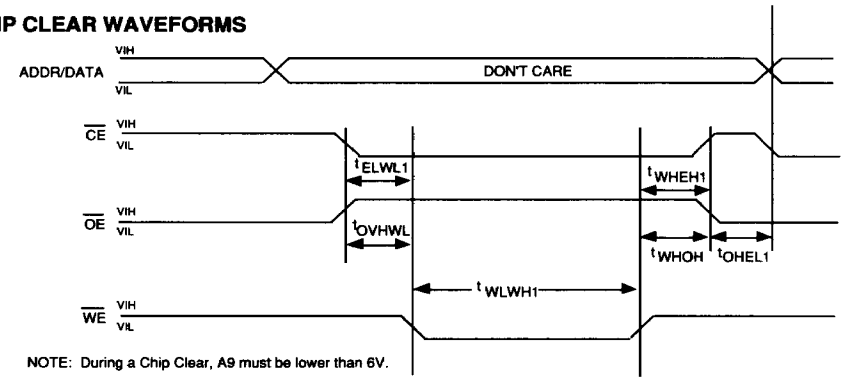


CHIP CLEAR OPERATION

AC Testing Waveform: V_{IH} = 2.4 V; V_{IL} = 0.45 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Military (B): T_{AMB} = -55°C to 125°C

Parameter	Symbol	Min	Max	Units	Remarks
$\overline{CE}$ Set-up Time	TELWL1	5	-	µs	-
$\overline{OE}$ Set-up Time	TOVHWL	5	-	µs	-
$\overline{CE}$ Hold Time	TWHEH1	5	-	µs	-
$\overline{OE}$ Hold Time	TWHOH	5	-	µs	-
$\overline{WE}$ Pulse Width for Chip Erase	TWLWH1	10	-	ms	-
Time to Next Operation	TOHEL1	5	-	µs	-
$\overline{OE}$ High Voltage	VH	12	13	V	-

CHIP CLEAR WAVEFORMS



NOTE: During a Chip Clear, A9 must be lower than 6V.

DEVICE IDENTIFICATION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	ⓥ	VIH	ⓥ	A9 = VH	Vcc	Data In

Note: YH = 12.5 V ± 0.5 V

Write Mode

The 28C256 has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

Page Write

The page write feature of the 28C256 allows the entire memory to be written in 2 seconds. Page write allows one to sixty-four bytes of data to be written into 28C256 in a single internal programming cycle. Internally, there are 64 byte registers (one page) addressed by A0 through A5. Data are loaded into corresponding registers during the load period and all data will be written into the specified one page of memory at once. The rules for page write are given below:

A. The page mode is initiated by any write operation and the following bytes can be loaded in the same way.
B. Each successive byte load cycle, started by the falling edge of write control signals (i.e. $\overline{WE}$ or $\overline{CE}$, whichever occurs last), must begin within 149μ seconds from the rising edge of the preceding write control signal. Otherwise, the load period ends and the internal programming cycle starts.
C. If page address (A6 through A14) does not stay the same through the entire load cycle, all data loaded will be written into the page address of the last data.
D. If the same byte location (addressed by A0 through A5) is loaded more than once, the latest value will be written into the memory.
E. There is no page write window limitation as long as rule B is followed.
F. In order to avoid unnecessary cycling of unused memory cells, only those bytes actually loaded into the page buffer will be written to memory.

Write Operation Status Bits

The 28C256 provides the user three write operation status bits. I/O7 is used for $\overline{DATA}$ polling and I/O6 is used as Toggle Bit, and I/05 is used for the Page-load timer.

Data Polling (I/07)

The 28C256 features $\overline{DATA}$ Polling to signal the completion of a byte write cycle. During a byte write or page write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O4 are indeterminable). After completion of the write cycle, true data is available. $\overline{DATA}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Toggle Bit (I/O6)

The Toggle Bit is another method of determining the internal programming status. During the internal programming cycle I/O6 will toggle on each attempted read (i.e. ...0-1-0-1-0...). The first read value is "0". The toggling will cease after the completion of the internal programming cycle.

Page Load Timer (I/O5)

During the write loading period and internal programming cycle, I/O5 will show the page-load timer status on read operation. "O" means it is still in the loading window. "I" tells the user that the loading period has expired and the internal programming cycle has begun.

Software Data Protection

The 28C256 offers a software controlled data protection feature. Once the software data protection is employed, the 28C256 is automatically protected during power-up and power-down without the need for external circuits. The 28C256 is further protected from inadvertent and accidental writes in the power-on state. That is, a software algorithm must be issued prior to writing any data to the device. The first issuing of the software algorithm sets the write protection circuit, which is non-volatile and will remain set for the lifetime of the device unless the reset command is issued.

Write Protection Set/Reset Algorithms

Setting the software write protection mode requires a series of three bytes of data to be written consecutively into three specific addresses. The write sequence must conform to the page write timing specification. The Write Protection setting code listed below shows the sequence of setting the write protection mode. The third byte of the algorithm effectively opens the page write window to enable one page write immediately after the software algorithm. Once the internal programming cycle is completed, the 28C256 will automatically be returned to the write protection state. The write protection circuit can be reset by performing a series of six byte writes as shown in the listed Write Protection Resetting code. Page write is allowed immediately after the sixth write of the reset algorithm.

WRITE PROTECTION SETTING CODE

Data	Address
AA	5555
55	2AAA
AO	5555

WRITE PROTECTION RESETTING CODE

Data	Address
AA	5555
55	2AAA
80	5555
AA	5555
55	2AAA
20	5555

Software Chip Clear

The 28C256 also provides a software controlled chip clear feature. The whole memory can be cleared to state "1" by issuing a series of six-byte codes to specific addresses. The software chip clear algorithm is shown in the Software Chip clear code listing. The software chip clear functions only when write protection is reset. During the 10msec chip clear cycle, both Data Polling and Toggle Bit features can be used to detect the internal programming status.

SOFTWARE CHIP CLEAR CODE

Data	Address
AA	5555
55	2AAA
80	5555
AA	5555
55	2AAA
10	5555

Device Identification

An extra row of 64 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0 to 7FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Hardware Chip Clear

The 28C256 array can be cleaned to state "1" by raising $\overline{OE}$ to 12V and setting $\overline{CE}$ to V_{IL} then bringing $\overline{WE}$ to V_{IL}.

Retention Endurance

Read retention for data written into the 28C256 is greater than 10 years, with up to 10^4 write cycles. There is no limit to the number of times data may be read.

ORDERING INFORMATION

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers.

PART NUMBERS

28C256 - 15 B X A

Lead Finish	A	Solder Dip
	B	Matte Tin
	C	Gold
Package:	X	Cerdip
	U	Ceramic Leadless Chip Carrier
Temperature Range:	B	-55° C to 125° C
Access Time:	15	150 nsec
	12	120 nsec
	90	90 nsec
Device	28C256	256K (32K x 8) CMOS Electrically Erasable EPROM

Screening per MIL-STD-883C