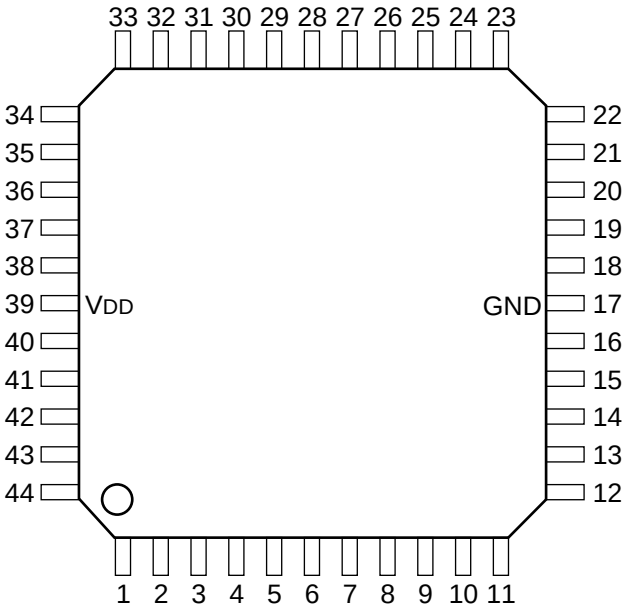
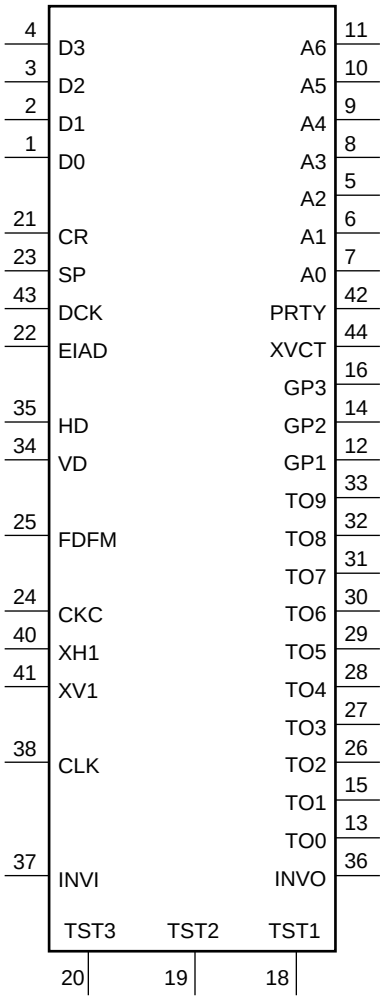
C-MOS GATE ARRAY

—TOP VIEW—





PIN No.	I/O	SYMBOL	PIN No.	I/O	SYMBOL	PIN No.	I/O	SYMBOL	PIN No.	I/O	SYMBOL
1	I	D0	12	O	GP1	23	I	SP	34	I	VD
2	I	D1	13	O	TO0	24	I	CKC	35	I	HD
3	I	D2	14	O	GP2	25	I	FDFM	36	O	INVO
4	I	D3	15	O	TO1	26	O	TO2	37	I	INVI
5	I/O	A2	16	O	GP3	27	O	TO3	38	I	CLK
6	I/O	A1	17	—	GND	28	O	TO4	39	—	V_{DD}
7	I/O	A0	18	I	TST1	29	O	TO5	40	I	XH1
8	I/O	A3	19	I	TST2	30	O	TO6	41	I	XV1
9	O	A4	20	I	TST3	31	O	TO7	42	O	PRTY
10	O	A5	21	I	CR	32	O	TO8	43	I	DCK
11	O	A6	22	I	EIAD	33	O	TO9	44	O	XVCT

INPUT

CKC	:	XH1 ACTIVE EDGE DECISION
CLK	:	SYSTEM CLOCK
CR	:	COMPENSATION DATA SELECT (H : µ-COM MODE, L : NORMAL MODE)
D0-D3	:	4-BIT PARALLEL DATA
DCK	:	DATA INPUTS STROBE PULSE
EIAD	:	H : EXT ADDRESS, L : INT ADDRESS
FDFM	:	FRAME READ/FIELD READ
	:	SWITCH (H : FIELD READ)
HD	:	HORIZONTAL DRIVE
INVI	:	INVERTER
SP	:	INPUT DATA SERIAL/PARALLEL SWITCH (H : SERIAL)
TST1 - TST3	:	TEST MODE SELECT
VD	:	VERTICAL DRIVE
XH1	:	CLOCK FOR COMPENSATION DATA
XV1	:	LINE COUNTER INPUT TERMINAL

OUTPUT

A4 - A6	:	DATA ADDRESS
GP1 - GP3	:	GATE PULSE FOR COMPENSATION DATA (R, G, B-CH)
INVO	:	INVERTER
PRTY	:	12-BIT DATA PARITY CHECK (H : EVEN)
TO0 - TO9	:	TEST TERMINAL FOR INTERNAL DATA OUTPUTS
XVCT	:	ROM POWER VOLTAGE CONTROL TERMINAL

INPUT/OUTPUT

A0 - A3	:	DATA ADDRESS OUTPUTS (DATA ADDRESS INPUTS ; µ-COM MODE)