Features

Profiles and standards
- 4:2:2 Profile at Main Level
- Main Profile at High Level
- Main profile at Main Level
- Simple Profile at Main Level

Image resolutions
- Up to 720x512x30 Fps NTSC
- Up to 720x608x25 Fps PAL

Input image pre-processing
- Horizontal noise filter
- Vertical noise filter
- Temporal filter
- Supports horizontal image scaling
- Supports 4:2:2 to 4:2:0 chroma conversion

Compression Options
- 4:2:2 or 4:2:0 output chroma format
- Supports field or frame encoding
- Variable GOP structure
- External reference rate control
- Supports dynamically variable parameters
- Supports MPEG-2 or ATSC user data insertion
- Minimum encoding latency
- Supports up to +/- 200H and +/- 128V search range
- Programmable quantization tables

Output
- Selectable ES or PES output format
- Produces up to 50 Mbps

Memory
- Single SDRAM memory interface
- Requires a minimum 8 MB of 125 MHz SDRAM
- Supports 2 bank and 4 bank memory chips

Technology
- 3.3V and 2.5V power supplies
- 1.6W nominal power dissipation
- IBM CMOS SA-12E (0.18µm) process technology
- 35 mm HPBGA package

Description

The IBM eNV SD video encoder chip offers flexibility and provides a compact solution for your SD application. The chip supports both MPEG-1 and MPEG-2 real-time encoding. It handles multiple profiles and levels including 4:2:2 Profile at Main Level and can encode picture resolutions up to 720x512 and 720x608 in NTSC and PAL, respectively.

The architecture offers a wide range of capability to encode SD images. The chip can compress images into either MPEG-2 4:2:2 profile for professional applications or Main profile for broadcast applications. It can deliver 4:2:2 or 4:2:0 chroma output format. The user can program a search range of up to +/-200H and +/-128V based on their application needs.

The chip outputs up to 50 Mbps with superior image quality, making it desirable for high quality, high bit rate solutions.

The programmable on-chip noise reduction filter provides an effective solution to achieve the best image quality at lower bit rates, making a highly desirable choice for broadcast and distribution applications requiring VBR and statistical-multiplexing.

Dynamic changing of encoding parameters such as GOP structure, bit rate control, and search range in real time provides added flexibility to optimize picture quality at the available bandwidth.

Block Diagram

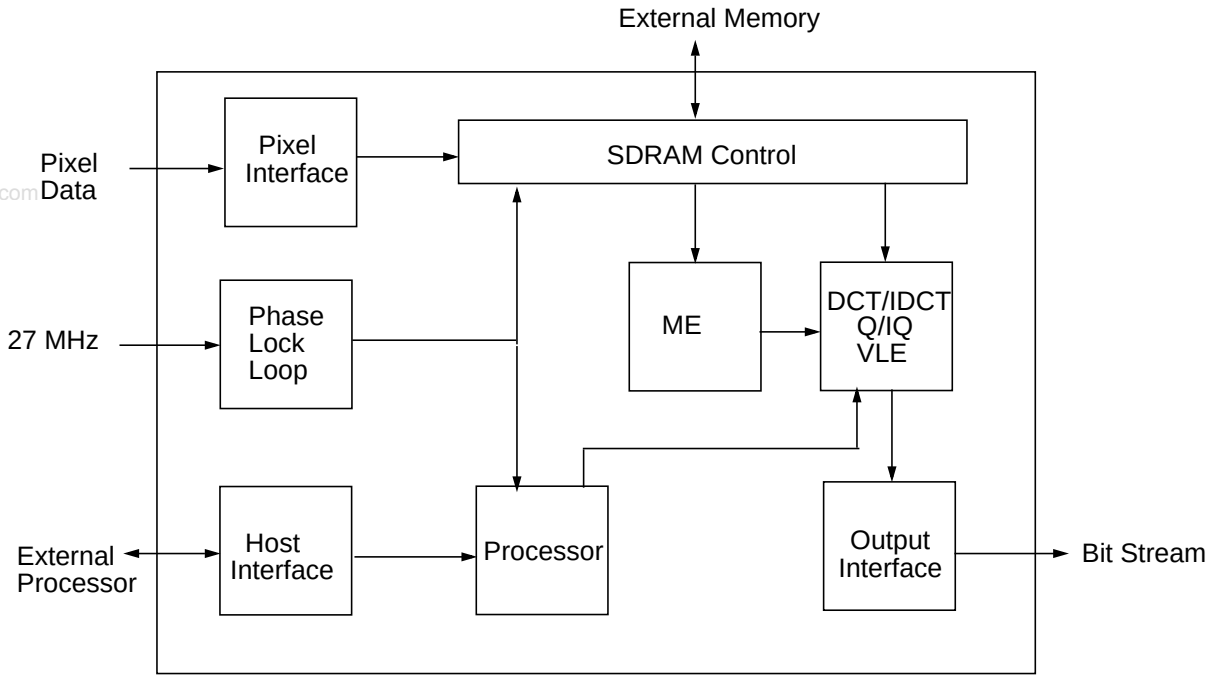

Fig. 1. eNV Block Diagram

Pixel Interface

The Pixel Interface supports user selectable CCIR 656 (8-bit) or CCIR 601(16-bit) operation. A 27 MHz pixel clock is used for CCIR 656 format. It also supports a clock rate of up to 13.5 Mhz clock for the CCIR 601 (16-bit) mode. This interface is designed to accept pixel data upon completion of the initialization process after power-on reset.

Phase Lock Loop

The Phase Lock Loop (PLL) takes as input the 27 MHz reference clock, divides it into the system clock rate, and provides synchronized clock pulses to the entire chip.

Host Interface

Connected to an external processor, the Host Interface communicates user input encoding parameters to the system through a 16-bit data bus and 8-bit address bus. Data is entered via register writes or via dedicated Picture and GOP stacks. The Host Interface also offers a means of inputting certain commands to the encoder's processor by mailbox, and the reading of select system registers for status and checking.

Processor

A dedicated RISC processor programmed to optimize encoding across a broad range of parameters. The processor acts as an engine for rate control, motion estimation, and motion compensation calculations. Microcode-based field upgrades are available to the customer and are a key feature of the eNV SD video encoder.

SDRAM Control

A single memory interface designed to support 125MHz, 32-bit SDRAM. The encoder requires a minimum of 8MB of external memory for full IPB encoding.

Motion Estimation (ME)

A hierarchical motion estimation and compensation unit capable of searching up to +/-200 horizontal pixels and +/-128 vertical pixels. The ME unit performs past reference searches in the case of P and B pictures, and future reference and bi-directional searches in the case of B pictures. Adaptive frame/field motion estimation with interpolation for 1/2 pixel refinement is performed on a per macroblock basis.

DCT/IDCT/Q/IQ/VLE

Dedicated hardware function for coding the bitstream and creating reconstructed reference data for motion estimation and compensation. The quantizer (Q) and inverse quantizer (IQ) units are capable of holding up to eight 8x8 user quantization tables (2 intra luma, 2 non-intra luma, 2 intra chroma, 2 non-intra chroma).

Output Interface

Designed for programmable output modes and speeds up to 50Mb/sec. Outputs the bitstream in either ES or PES format, with encoding statistics available at the output interface.

Environmental and Electrical Specifications

The eNV SD chip is designed to operate from 0 to 70 degrees C ambient environment.

Table 1. Operating Range/Ratings of eNV SD

Parameter	Value	Units
Vdd (supply voltage)(maximum)	2.625	Volts
Vdd (Nominal supply voltage)	2.5 ± 5%	Volts
Vdd2 (supply voltage)(maximum)	3.465	Volts
Vdd2 (Nominal supply voltage)	3.30 ± 5%	Volts
System Clock	27	MHz
Ambient temperature range (operating conditions)	0 - 70	˚C
Operating temperature range (Chip Tj)	0 - 100	˚C
Storage temperature range	-55 to 125	˚C
Air Flow (minimum)	0.5	meters/sec
Power Dissipation (nominal)	1.6	Watts
Power Dissipation (maximum)	1.8	Watts

Note: The allowable ambient temperature range specified is based on the module mounted to a 2-signal/2-power plane card with the specified airflow on both sides of card, vertical orientation.

The drivers and receivers are compatible with 3.3 Volt-tolerant technologies.

Table 2. Physical Information of SD PBGA Package

Parameter	Value	Unit
Module dimension	35x35	mm
Module height	2	mm
Ball pitch	1.27	mm
Ball diameter	0.75	mm

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Revision Log

Rev. Date	Contents of Modification
Sept. 04, 2001	Initial Release (00)
Sept. 06, 2001	Minor corrections to text, added Figure and Table numbers (01)
Sept. 13, 2001	Minor changes to text requested by IBM attorney (02)