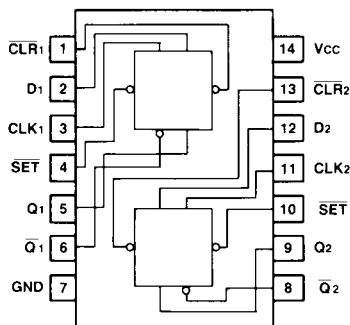


Dual D-Type Positive-Edge-Triggered Flip-Flop

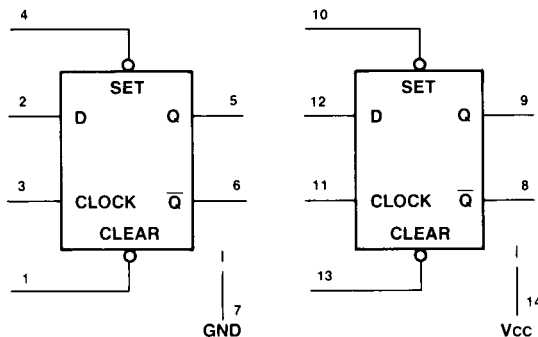
The LS74 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 14-pin plastic DIP or surface mount package.



Truth Table

Inputs				Outputs	
Set	Clear	Clock	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\bar{Q}_0$

Logic Diagram



* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

H = High level (steady state)

L = Low level (steady state)

↑ = Transition from low to high level

X = Irrelevant (any input, including transitions)

Q₀ = Level of Q before the indicated steady-state input conditions were established

$\bar{Q}_0$ = Complement of Q₀ or level of Q before the indicated steady-state input conditions were established

Electrical Characteristics

VCC = 5.0 ±0.5 V, TA = -55 to +125°C (WA-LS)

VCC = 5.0 ±0.25 V, TA = 0 to 70°C (WP90224L5)

VCC = 5.0 ±0.5 V, TA = -40 to +85°C (WA-LSD, WP91398L2)

		WA-LS		WP, WA-LSD		
Parameter	Symbol	Min	Max	Min	Max	Units
Output Voltage, VCC = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low, IOL = 4.0 mA	VOL	—	0.4	—	0.4	V
IOL = 8.0 mA	VOL	—	0.5	—	0.5	V
High, IOH = -0.4 mA	VOH	2.5	—	2.7	—	V
Input Voltage, VCC = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low	VIL	—	0.7	—	0.8*	V
High	VIH	2.0	7.5	2.0	5.5	V
Clamp, IIN = -18.0 mA	VIK	—	-1.5	—	-1.5	V
Input Current, VCC = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Low, VIL = 0.4 V						
Data	IIL	—	-0.4	—	-0.4	mA
Clock, Set	IIL	—	-0.8	—	-0.8	mA
Clear	IIL	—	-1.2	—	-1.2	mA
High, VIH = 2.7 V						
Data	IIH	—	20.0	—	20.0	μA
Clock, Set	IIH	—	40.0	—	40.0	μA
Clear	IIH	—	60.0	—	60.0	μA
@ VI max,						
VI = 7.0 V (except Set and Clear, VI = 5.5 V) (WA-LS)						
VI = 5.5 V (WP, WA-LSD)						
Data	II	—	0.1	—	0.1	mA
Clock, Set	II	—	0.2	—	0.2	mA
Clear	II	—	0.3	—	0.3	mA
Output Current, VCC = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Short-Circuit	Ios	-20.0	-100.0	-20.0	-100.0	mA
Supply Current, VCC = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)	ICC	—	8.0	—	8.0	mA

* WA-LSD, WP91398L2: VIL = 0.7 V

$V_{CC} = 5.0 \text{ V}, T_A = 25^\circ\text{C}, C_L = 15 \text{ pF}$

		WA-LS		WP, WA-LSD		
Parameter	Symbol	Min	Max	Min	Max	Units
Propagation Delay						
Clock-to-Output, Low-to-High	t _{PLH}	—	20.0	—	25.0	ns
High-to-Low	t _{PHL}	—	30.0	—	40.0	ns
Clear- or Set-to-Output, Low-to-High	t _{PLH}	—	18.0	—	25.0	ns
Clear- or Set-to-Output (Clock Low), High-to-Low	t _{PHL}	—	24.0	—	40.0	ns
Clear- or Set-to-Output (Clock High), High-to-Low	t _{PHL}	—	35.0	—	40.0	ns
Operating Conditions						
Pulse Width, Clock High	t _{wOH}	25.0	—	25.0	—	ns
Preset or Clear	t _w	25.0	—	25.0	—	ns
Setup Time, Low	t _{DSL}	20.0	—	20.0	—	ns
High	t _{DSH}	25.0	—	20.0	—	ns
Hold Time, Low	t _{DHL}	5.0	—	5.0	—	ns
High	t _{DHH}	5.0	—	5.0	—	ns
Maximum Clock Frequency	f _{max}	30.0	—	25.0	—	MHz

Power supply voltage (V_{CC})..... 7.0 V

Operating temperature (TA)..... WA-LS: -55 to +125°C

WP90224L5: 0 to 70°C

WA-LSD, WP91398L2: -40 to +85°C

Storage temperature (T_{stg})..... -65 to +150°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

Timing Diagrams

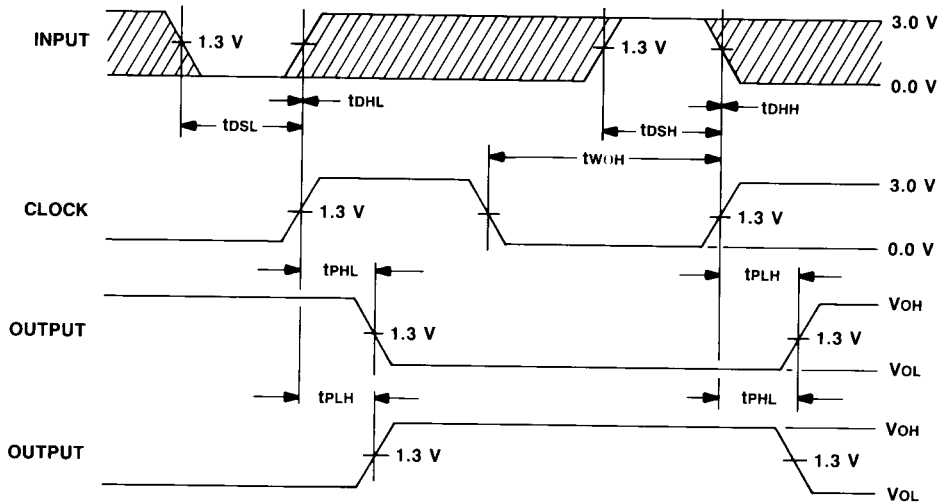


Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width (Note 1)

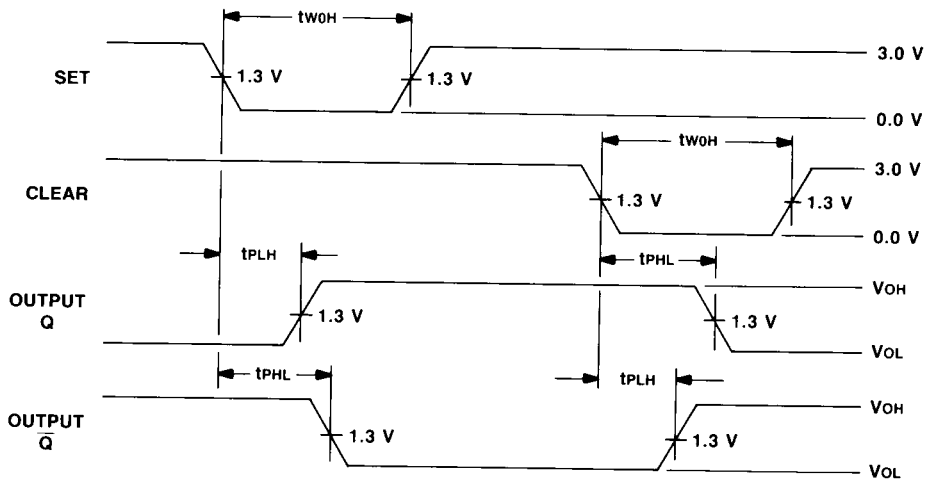


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths (Note 2)

Notes:

1. This waveform is for an output with internal conditions such that the output is low except when disabled by the output control.
2. This waveform is for an output with internal conditions such that the output is high except when disabled by output control.