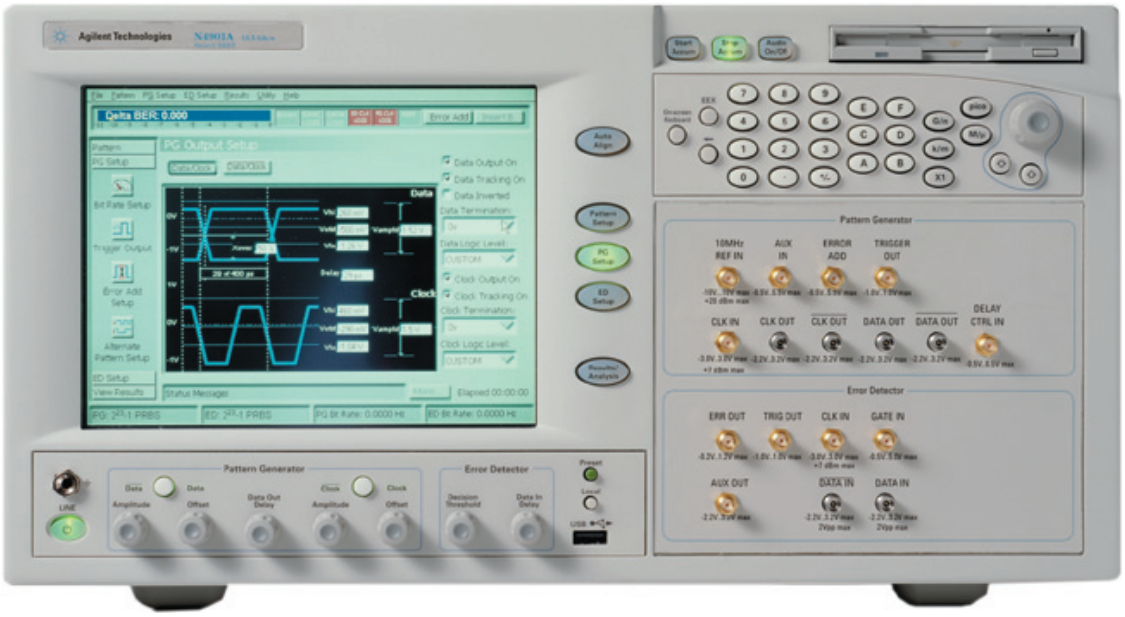
N4902B SerialBERT 7 Gbps

Technical Specification

Version 1.0



Agilent Technologies

General

The N4902B SerialBERT 7 Gbps operates within a range from 620 Mbps up to 7 Gbps. Available configurations are:

- one Pattern Generator and one Error Detector
- one Pattern Generator only
- one Error Detector only

Key values & Benefits

- Range of operation 620 Mbps to 7 Gbps
- Jitter Injection, Jitter Tolerance measurement capabilities
- True differential data generation and analysis
- CDR with ranges at approximately 3 Gbps and 6 Gbps
- Intuitive, state-of-the-art Windows XP. touchscreen user interface
- Inter-operability between N4902B and other instruments
- Compatability with existing remote commands e.g. Agilent 71612 and 86130A Series
- Signal integrity
- Fastest transition times

Pattern Generator

- Pattern generation for PRBS or memory based patterns
- Flexible levels addressing a broad range of technologies, e.g. ECL, PECL (3.3V), LVDS, CML

Error Detector

- BER Measurements
- Automatic Threshold
- Sampling Point
- Search Data Polarity
- G. 821 Measurement
- Measurement Suite
- Auto Alignment

Measurement features

- Output Timing Jitter
- Spectral Jitter
- Output Level
- Bit Error Rate
- Fast Eye Mask
- Eye Contour

Display

8” color LCD touchscreen

Data Entry

Touch-screen display, numeric keypad with up/down arrows, dial-knob control or USB keyboard and mouse.

Hard Disk

For local storage of user patterns and data. Internal or external disk available.

Removable Storage

- Floppy Disk Drive 1.44 MB
- USB Stick

Online Help

For comprehensive software support

Interfaces

GPIB (IEEE 488), LAN, parallel printer port, VGA output, 4 x USB 2.0, 1 x USB 1.1 ports

User Interface

The time needed to set up the first measurement is minimised based on intuitive and easy-to-learn interfaces.

The “N4902B SerialBERT 7 Gbps” User Interface is easily fitted to a variety of applications. In addition, the optimized measurement suite guarantees an immediate return on investment.

The User Interface provides the following functions:

- Patter Generator Setup
- Error Setup Analyser / Detector
- Pattern Editor
- Measurement Results

By utilizing network capabilities, N4902B SerialBERT is remote controllable via LAN. GPIB is available for MS Windows, Unix or Linux operating systems. Test executives can control the system by using National Instruments’ LabVIEW, Agilent TestExec, and Microsoft® Excel or Visual Basic.

Examples for Results Screens

The Generator Pattern Editor allows simple access to timing & level parameters, as seen below.

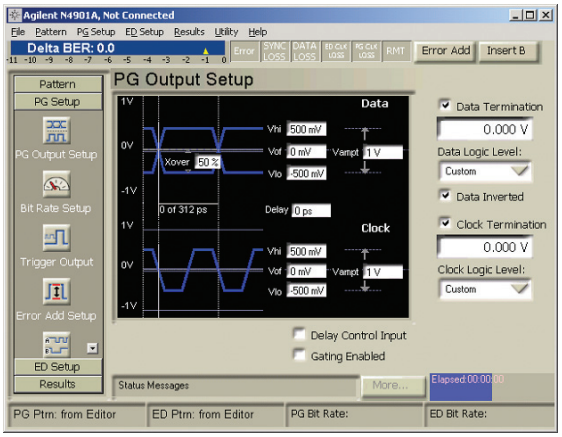


Figure 1: Generator Setup

The Sampling Point Setup allows simple access to Sampling Point precision referring to timing point threshold.

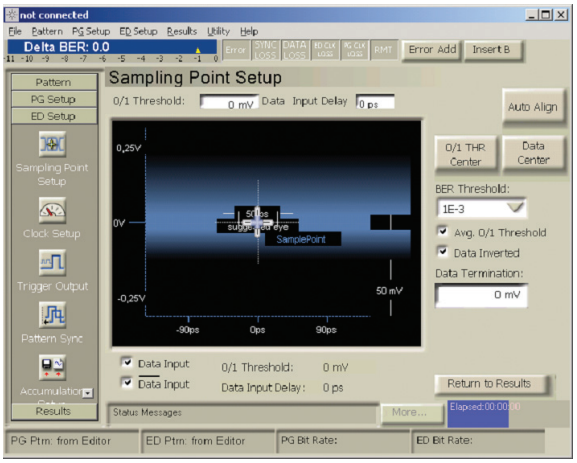


Figure 2: Error Detector Setup

The Pattern Editor allows the operator to deal with user-specific data.

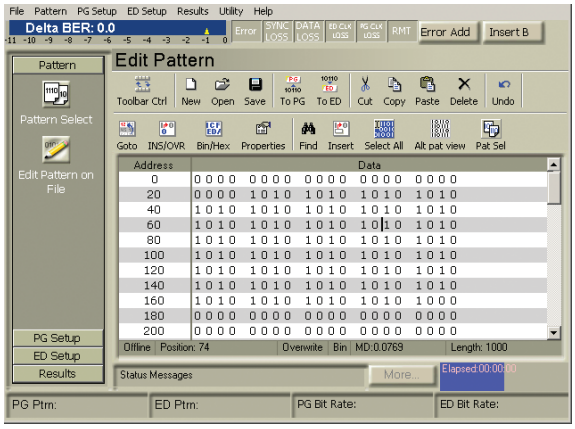


Figure 3: Pattern Editor Setup

The diagram below shows bit error results based on CCITT Ref. G.821.

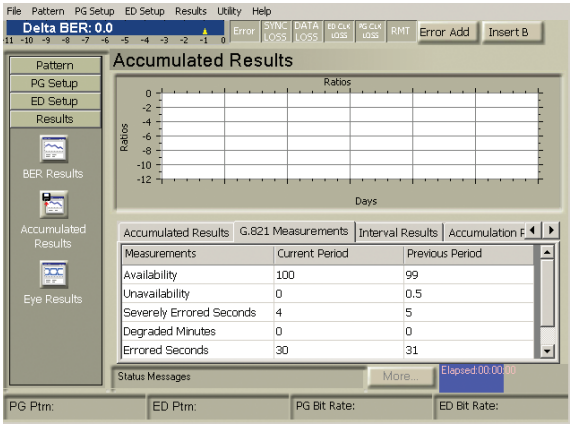


Figure 4: G.821 Results

Measurement Suite

The Measurement Suite of the SerialBERT 7 Gbps offers comprehensive analysis features, detailed insight for design verification and efficient pass/fail testing in manufacturing.

Spectral Jitter Decomposition (see Fig. 5)

It includes a measurement for the spectral decomposition of jitter components. The decomposition technique allows inband- and outband-characterization of circuits and devices including PLLs and CDRs. While debugging designs, the new measurement allows the exploration of the various components of deterministic jitter.

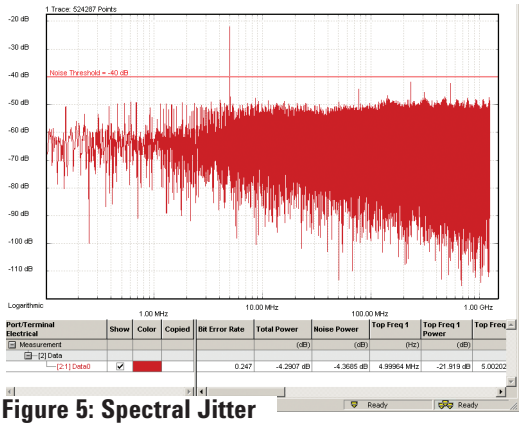


Figure 5: Spectral Jitter

BERT Scan incl. Rj / Dj separation (see Fig. 6)

This measurement shows the BER of the DUT's output versus sample point delay, which is displayed as a curve with BER vs. sample delay and threshold. Available results are setup/hold time, phase margin, Jitter incl. extrapolation of total jitter (rms, peak-to-peak) and RJ/DJ Separation. The output timing measurement is available as a bathtub plot and as a histogram. This provides measurement of RJ, DJ and Total Jitter. The measurement method is equivalent to the IEE802.3ae method. In order to guarantee the validity of the measurement, a "quality of fit" value is also provided.

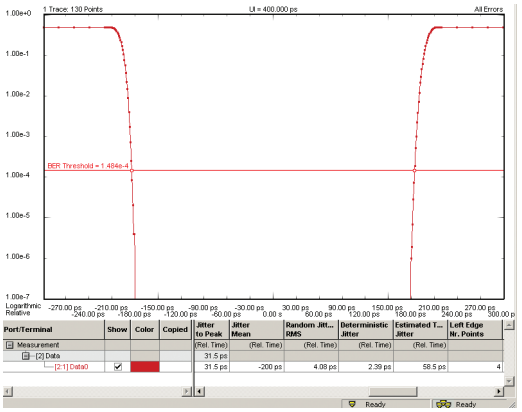


Figure 6: BERT Scan incl. Rj/Dj Separation

Output Level and Q Factor (see Fig. 7)

Figure 7 shows the sample BERT delay corresponding to the threshold. Available results are Q Factor, table.

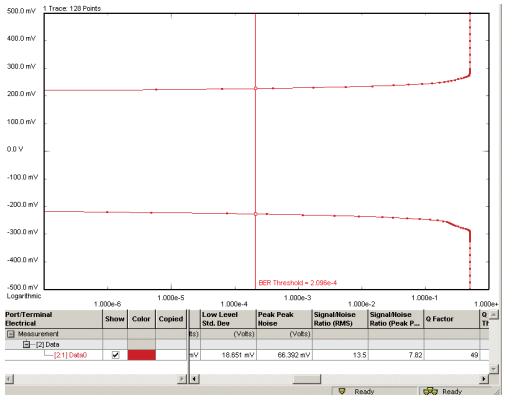


Figure 7: Output Level & Q Factor

Eye Contour (see Fig. 8)

For device characterization the eye opening measurement generates a three-dimensional bit error rate (BER) diagram as a function of the sample delay and the sample threshold. Besides the eye opening, the eye contour measurement provides results for the optimum sample point. The eye opening measurement allows selecting different views such as eye contour, pseudo color and equal BER plots.

Fast Eye Mask

For fast pass/fail testing in manufacturing, this measurement checks up to 32 points, equivalent to mask testing.

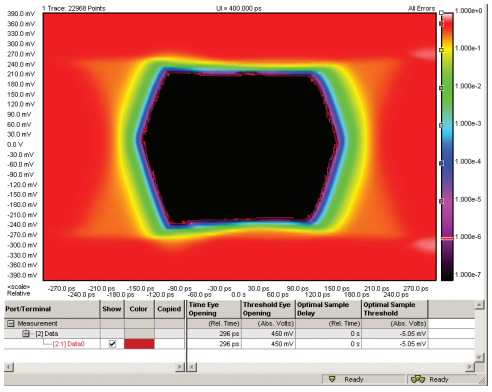


Figure 8: Eye Contour

Pattern Generator

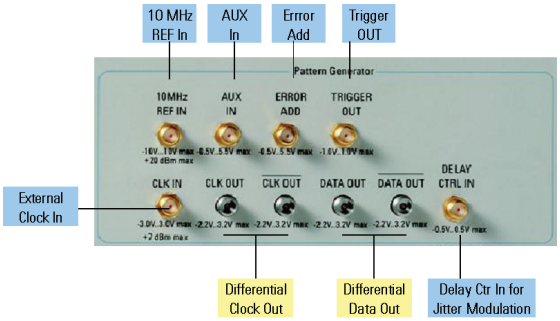


Figure 9: Front View of Pattern Generator

Waveform examples for Differential Data Output

Pulse Performance Measurement allows different amplitude voltages with variable amplitudes from 50mV...1.8V, output voltage. The window makes -2V...2.8V possible and a variable delay. An example is shown below in Figure 10.

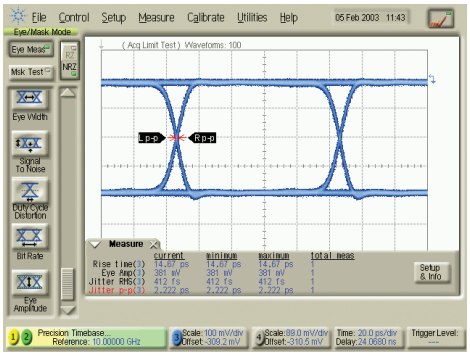


Figure 10: 50% Signals at 2V

Features:

· Polarity - normal or inverted data
· Data high level adjust
· Data amplitude adjust
· Clock/Data relative delay adjustment
· Vertical data-eye cross-over adjust
· Output gating
· Error add
· Delay control input

Data Output

Table 1: Parameters for SerialBERT 7 Gbps General

Range of operation:	620 Mbps to 7 Gbps
Interface	Differential or single-ended **(1)**, DC coupled, 50Ω
Format	NRZ, normal or inverted
Amplitude/Resolution	0.10 V to 1.8 V in 5 mV steps
Output voltage window	-2.0 V to +3.0 V
Predefined Levels	ECL, PECL (3.3V), LVDS, CML
Transition times (10% to 90%)	< 25 ps pp **(2)**
Jitter	9 ps pp typical
Clock/data delay	±0.75 ns
Resolution	100 fs
Terminations	50Ω, -2 V to 3 V or 50Ω AC coupled (the external termination voltage must be below the output high level)
Crossing point of adjustment	20%.....80% typical
Single Error Inject	Adds single errors on demand
Fixed Error Inject	Fixed error ratios of 1 error in 10^n bits, n = 3, 4, 5, 6, 7, 8, 9
Delay Control Input	± 100ps, DC to 1 GHz @ data rate <10.5 Gpbs
Connector	2.4 mm female

(1) In single-ended mode the unused output has to be terminated by a 50Ω resistor to ground
(2) at ECL levels

Clock Output

Table 2: Parameters for N4902B SerialBERT 7 Gbps Generator

Clock Output	1, differential or single-ended, 2.4mm(f) **(1)**
Frequency	620 MHz - 7 GHz
Impedance	50 Ohm typ.
Amplitude/Resolution	0.1Vpp to 1.8 Vpp in 5mV steps
Output voltage window	-2.00 to +2.80 V
Short circuit current	72 mA max.
External termination voltage	-2V to +3V **(2)**
Addressable technologies	LVDS, CML
	PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS
Transition times (10%-90%)	<25 ps
Jitter	1 ps RMS typ.
SSB phase noise (10GHz@ 10kHz offset, 1Hz bandwidth)	< - 75 dBc with internal clock source

(1) In single-ended mode, the unused output must be terminated with 50 Ohm to GND.
(2) External termination voltage must be less than 3V below V_{OH}. External termination voltage must be less than 3V above V_{OL}. Termination into AC is possible.

10 MHz Reference Input

A 10 MHz reference signal can be applied from which the internal clock is derived.

Table 3: Specifications

Interface	AC coupled, 50Ω nominal
Amplitude	200 mV to 2 V
Connector	SMA female

Clock Scheme

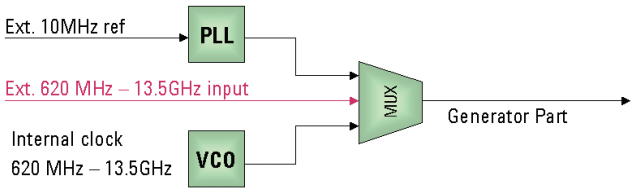


Figure 11: Block Diagram for the Clock Section

Three clock paths are possible:

- 10 MHz Ref. Input used to synchronise SerialBERT 7 Gbps with other equipment at 10 MHz
- Ext. Clock Input operates from 620 MHz to 7 GHz. This allows the input of a FM modulated clock for Jitter Transfer or Jitter Tolerance measurements
- Internal clock reference operates from 620 MHz to 7 GHz

Clock Input

Table 4: Clock Input

Frequency range	620 MHz to 7 GHz
Interface	AC coupled, 50Ω nominal
Amplitude	150 mV to 2 V
Connector	SMA female

Table 5: Delay Control Input

Interface	DC coupled, 50Ω nominal
Input voltage window	-250 mV to +250 mV
Delay Range	-100 ps to + 100 ps
Modulation Bandwidth	DC to 1 GHz
Connector	SMA female

Modulation

Face Modulation operates between 620 and 7 Gbps. It is a linear Δd/Δt function that allows diverse signal distortions to be added.

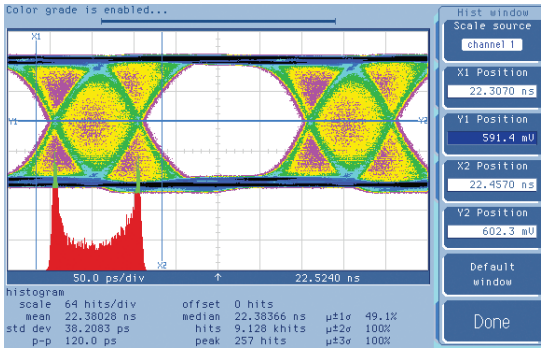


Figure 12: Sinusoidal Jitter

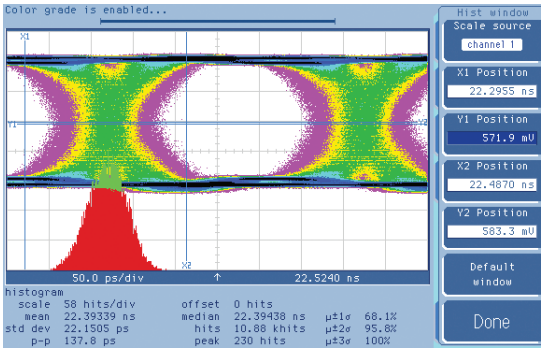


Figure 13: Random Jitter

Trigger Output

This provides an electrical trigger synchronous with the pattern for use with an oscilloscope or other test equipment. There is a fixed delay of 32 ns typical between trigger and data output for the selected bit. It operates in two modes: pattern trigger and divided clock trigger.

Pattern Trigger Mode

For PRBS patterns the pulse is synchronized with a user specified trigger pattern. The repetition rate is 1 pulse for every 4th pattern repetition. For alternate patterns the trigger pulse occurs at bit 0 of the selected pattern. For all other patterns, the trigger pulse is synchronized to a user-definable bit in the pattern.

Divided Clock Mode

In divided clock mode the trigger is a square wave at the clock rate divided by 2, 4, 8, 10, 16, 20, 40, 64, 128.

Table 6: Specifications

Pulse width	Square wave
Levels	High: +0.5 V; Low -0.5 V typ.
Transition times	35 ps typical
Interface	DC coupled, 50Ω nominal
Connector	SMA female

Auxiliary Input

This port can be used to control user programmable, alternate test patterns or inhibit data output (force the output data to a fixed low level). When Alternate Pattern Mode is selected the instrument will output one of two patterns (A or B). The auxiliary input controls which pattern is output in one of two modes. In both modes, switching between patterns is at the end of a pattern and is 'hitless' (error free).

Mode 1: One-shot
A rising edge on the auxiliary input inserts a single version of pattern B into repetitions of pattern A.

Mode 2: Alternate
The logic state of the signal at the auxiliary input determines which pattern is output. An active (TTL high) signal will output Pattern 3.

The auxiliary input may also be used to inhibit the data output signal. If Alternate Pattern mode is not selected, an active (TTL high) signal at the auxiliary input port forces (gates) the data to a logic zero at the next 32-bit boundary in the pattern.

Auxiliary Input
Switch between two different data sequences using an external trigger pulse

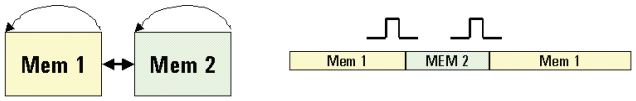


Figure 14: External Trigger Pulse

Table 7: Specifications

Interface	**DC coupled, 50Ω nominal**
Levels	**TTL levels**
Minimum Pulse Width	**100 ns**
Connector	**SMA female**

Patterns

PRBS (HW Generated)
- 2^{31} - 1 Polynomial: $x^{31} + x^{28} + 1 = 0$ (inverted)
- 2^{23} - 1 Polynomial: $x^{23} + x^{18} + 1 = 0$ (inverted) (ITU-T O.151)
- 2^{15} - 1 Polynomial: $x^{15} + x^{14} + 1 = 0$ (inverted) (ITU-T O.151)
- 2^{11} - 1 Polynomial: $x^{11} + x^{9} + 1 = 0$ (inverted) (ITU-T O.152)
- 2^{10} - 1 Polynomial: $x^{10} + x^{7} + 1 = 0$ (inverted)
- 2^{7} - 1 Polynomial: $x^{7} + x^{6} + 1 = 0$ (inverted) (ITU-T V.29)

Zero Substitution
Zeros can be substituted for data to extend the longest run of zeros in the patterns below. The longest run can be extended to the pattern length -1. The bit following the substituted zeros is set to 1.

Variable Mark Density
The ratio of ones to total bits in the patterns below can be set to 1/8, 1/4, 1/2, 3/4, or 7/8.

Available test patterns for zero and variables:
- 8388608 bits based on 2^{23}-1 PRBS
- 32768 bits based on 2^{15}-1 PRBS
- 8192 bits based on 2^{13}-1 PRBS
- 2048 bits based on 2^{11}-1 PRBS
- 1024 bits based on 2^{10}-1 PRBS
- 128 bits based on 2^{7}-1 PRBS

User-programmable Test Patterns
User defined patterns are available with variable length from 1 bit to 33,554,432 bits (2^{25}).

Alternate Test Pattern
Switch between two equal length user programmable patterns, each up to 16,777,216 bits. Switching is possible by using a front panel key, GP-IB or the auxiliary input port. Changeover is synchronous with the end of the pattern. The length of the alternating patterns should be a multiple of 512 bits. Two methods of controlling pattern changeover are available: one-shot and alternate.

External Error Inject Input
The external “Error Inject Input” adds a single error to the data output for each rising edge at the input.

Table 8: Specifications

Interface	DC coupled, 50Ω nominal
Levels	TTL compatible
Minimum pulse width	100 ns
Connector	SMA female

Delay Control Input
The delay control modulates the delay of the data ouputs.

Table 9: Delay Control Input

Interface	DC coupled, 50Ω nominal
Input Voltage Window	-250 mV to +250 mV
Delay Range	-100 ps to +100 ps @ 7 Gbps
Modulation Bandwidth	DC to 1 GHz
Connector	SMA female

Error Detector

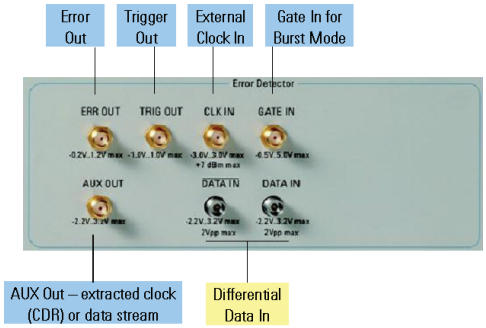


Figure 15: Front view Error Detector

Data Input

Features:

- Differential data inputs
- Data polarity - normal or inverted data.
- Clock/Data delay adjust.
- Clock/Data auto-alignment.
- 0/1 decision threshold auto-alignment.
- Clock data recovery (CDR) for selected frequency ranges or ext. clock

Table 10: Parameters for N4902B Error Detector

Range of operation	620 Mbps to 7 Gbps	
Impedance	Single-ended: 50Ω, -2.0V to +3.0V terminated(1) Differential: 100Ω	
Termination Voltage	-2 V to +3 V or off (true differential mode)	**(1)**
Format	NRZ	
Max Input Amplitude	2.0 V	
Sensitivity	<50 mV pp	**(2)**
Decision threshold range	-2 V to +3 V in 0.1 mV steps	
Max Levels	-2.2V to +3.2V	
Phase Margin	1UI - 12ps typical	**(3)**
Clock/Data phase alignment	±0.75 ns in 100 fs steps	
Clock data recovery (CDR)	4.23 Gbps to 6.40 Gbps 2.11 Gbps to 3.20 Gbps	
CDR Output Jitter	0.01 UI_{rms} typical	
Connector	2.4 mm female	

(1) A user has to define a 2V operating voltage window, which is in the range between -2.0 V to +3.0 V. Data signals, termination voltage and decision threshold have to be within this voltage window.

(2) @ 10 Gbps, BER 10^{-12}, PRBS 2^{31} -1.

(3) Based on internal clock

Clock Input

Table 11: Specifications

Frequency range	620 MHz to 7 GHz
Interface	AC coupled, 50Ω nominal
Amplitude	100 mV to 1.2 V
Connector	SMA female

Possibilites for CDR movement or External Clock Input.

Trigger Out

Error Detector Pattern Trigger Output

This provides an electronic trigger synchronous with the selected error detector reference pattern. It operates in two modes, pattern trigger and divided clock trigger.

Pattern Trigger Mode

This provides an electrical trigger synchronous with the selected error detector reference pattern. In pattern mode the pulse is synchronized to repetitions of the output pattern. For PRBS patterns the repetition rate is 1 pulse for every 4th pattern repetition

Divided Clock Mode

In divided clock mode the trigger is a square wave at the clock rate divided by 4, 8, 16, 32, 40, 64, 128.

Table 12: Specifications

Interface	DC coupled, 50 Ω nominal
Levels	High: + 0.5 V; Low: - 0.5 V
Minimum pulse width	pattern length x clock period/2 at 10Gb/s with 1000 bits = 50 ns
Connector	SMA female

Errors Output

This provides an electrical signal to indicate received errors. The output is the logical 'OR' of errors in a 128-bit segment of the data.

Table 13: Specifications

Interface Format	RZ, active high
Interface	DC coupled, 50Ω nominal
Levels	High: 1V nominal; Low: 0 V nominal
Pulse Width	128 clock periods
Connector	SMA female

Gating Input

The Gating Input is used to enable the error counters including during burst gating mode. In both these cases the error counters will always be enabled for a multiple of 512 pattern bits

Table 14: Gating Input

Interface levels	TTL levels
Pulse width	256 clock periods
Connector	SMA female

Connecting an external termination to the gating input will pull it low and disable the instrument error counters. Gating resumes when the Gating Input returns high.

AUX Output

This output can be used to provide either clock or data signals:

CLOCK: clock signals from the input or recovered clock signals in CDR mode.

DATA: data after being compared with the threshold.

Automatic Clock-to .Data Alignment

An important feature of the SerialBERT error detector is the ability to automatically align the clock and data inputs such that the error detector samples are in the middle of the eye (in the time axis).

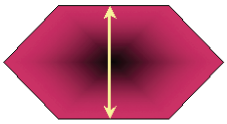
Table 15: Specifications of AUX Out

Interface	AC coupled, 50Ω nominal
Amplitude	600 mV nominal
Connector	SMA female

Audible Error Indicator

Selectable to indicate errors, instantaneous error ratios, and errors above user-defined thresholds. On/Off volume control, and audible pitch changes with higher pitch corresponding to higher BER

Automatic Threshold Center Search



Automatic Clock-Data Sampling Point Search

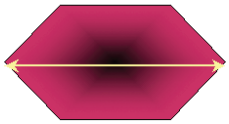


Figure 16: Automatic Optimum Sampling Point Location

Automatic 0/1 Threshold Centre

The 0/1 threshold center operation is used to set the 0/1 threshold midway between two points, top and bottom of the eye where the bit error ration is equal to a selectable threshold. There are three methods of determining the 0/1 Threshold of input signals at the error detector data input: Manual, Automatic Track and Automatic Center.

Manual

0/1 threshold can be set manually.

Automatic Track

This continuously tracks the mean DC level of the input signal and adjusts the threshold accordingly. The 0/1 threshold calculated is displayed. Adjustment is made within approximately 100ms. limited to a 2V window selected by the user.

Automatic Centre

The error detector sets the 0/1 threshold midway between two points, the top and bottom of the eye, where the bit error ratio is equal to a selectable threshold. The eye height is calculated and displayed. It is limited to a 2V window selected by the user.

Cable Droop Compensation

The N4902B SerialBERT 7 Gbps provides an excellent waveform at the end of a 24“ cable (N4910A). The cable droop is compensated and there is an excellent transition time <25 ps.

Mechanical Parameters

Table 16: General Mainframe Characteristics

Operating Temperature	5 °C to 40 °C
Storage Temperature	-40 °C to +70 °C
Humidity	5 - 40 °C, 95% rel.Humidity
Power Requirements	100 - 240 Vac, ± 10%, 47 - 63 Hz, 350 Vac
Physical dimensions	Width: 424.5 mm Height: 221.5 mm Depth: 580.0 mm
Weight (Net)	24.5 kg
Weight (shipping) (Max)	36.0 kg

Upgrade 7 Gbps - 13.5 Gbps

Agilent offers a factory-based upgrade possibility for the N4902B SerialBERT from 7 Gbps to 13.5 Gbps. For this service, please contact Agilent Technologies. The upgrade requires the following order instructions:

Table 17: Upgrades 7 Gbps - 13.5 Gbps

Order No.	Feature
N4900AS-101	Upgrade version N4902A-100 to 13.5Gb/s
N4900AS-102	Upgrade version N4902A-200 to 13.5Gb/s
N4900AS-103	Upgrade version N4902A-300 to 13.5Gb/s

Order Instructions

N4902B SerialBERT 7 Gbps, USB Mouse

IO-Configuration:

N4902B-100 Pattern Generator & Error Detector
N4902B-200 Pattern Generator only
N4902B-300 Error Detector only

Calibration/Test Data:

N4902B-UK6 Commercial Calibration with Test Data

Accessories:

N4910A Cable Kit: 2.4mm matched cable pair
N4911A-002 Adapter 3.5mm female to 2.4 mm male
N4912A 2.4mm, 50 Ohm termination, male

Warranty

R1280A Standard Warranty: 3 years Return-to-Agilent Extended Warranty: 5 years Return-to-Agilent

Calibration

R1282A Calibration plans are available to order for 3 or 5 years; calibration interval 12 month

Related Literature	Pub. No.
• N4901B SerialBERT 13.5 Gbps Data Sheet	5989-0398EN
• Agilent Physical Layer Test Product Overview	5988-5914EN
• N4902B SerialBERT 13.5 Gbps Product Note	5988-9676EN
• N4900 SerialBERT Jitter Fundamentals Application Note	5989-0089EN
• Jitter Tolerance Testing 81250 ParBERT Application Note	5989-0223EN
• ParBERT 81250 Product Overview	5968-9188E

Specification Assumptions
The specifications in this brochure describe the instrument's warranted performance. Non-warranted values are stated as typical. All specifications are valid in a range from 5°C to 40°C ambient temperature after a 30 minute warm-up phase. If not otherwise stated, all inputs and outputs need to be terminated with 50 Ohms to ground. All specifications, if not otherwise stated, are valid using the recommended N4910A cable set (24 mm, 24" matched pair).

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Taiwan:
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(fax) 0800 286 331

Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6836 0252
Email: tm_asia@agilent.com

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