PCA8565

Real time clock/calender

Rev. 01 — 31 March 2003 **Product data**

1. General description

The PCA8565 is a CMOS real time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All address and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

2. Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Century flag
- Clock operating voltage: 1.8 to 5.5 V
- Extended operating temperature range: –40 to +125 °C
- Low backup current; typical 0.5 µA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-wire I^2C-bus interface (at V_{DD} = 1.8 to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz and 1 Hz)
- Alarm and timer functions
- Integrated oscillator capacitor
- Internal power-on reset
- I^2C-bus slave address: read A3H and write A2H
- Open-drain interrupt pin.

3. Applications

- Automotive
- Industrial
- Other applications that require a wide operating temperature range.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	I^2C-bus active; f_{SCL} = 400 kHz; T_{amb} = –40 to +125 °C	1.8	-	5.5	V
I_{DD}	supply current	f_{SCL} = 400 kHz	-	-	820	µA
T_{amb}	ambient temperature		–40	-	+125	°C

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5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PCA8565TS	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

6. Block diagram

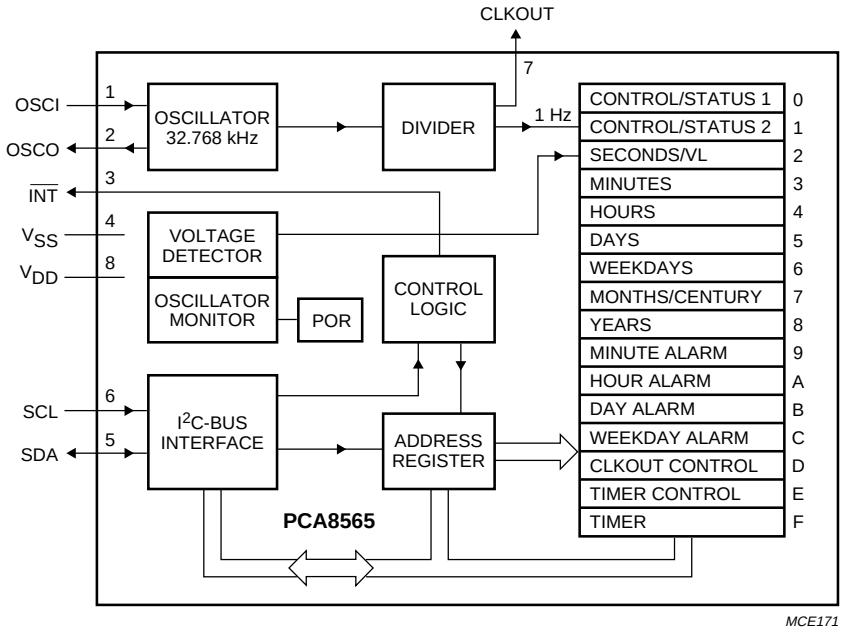

Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

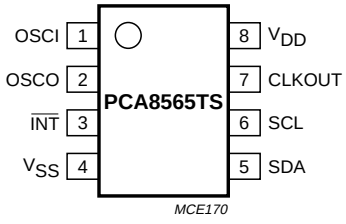

Fig 2. Pin configuration.

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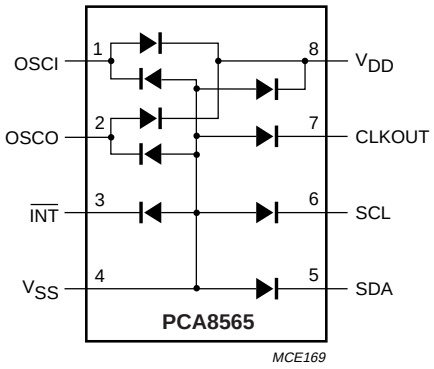

Fig 3. Device diode protection diagram.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
$\overline{INT}$	3	interrupt output (open-drain; active LOW)
V_{SS}	4	ground
SDA	5	serial data I/O
SCL	6	serial clock input
CLKOUT	7	clock output, open-drain
V_{DD}	8	positive supply voltage

8. Functional description

The PCA8565 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real Time Clock/calender (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00H and 01H) are used as control and/or status registers. The memory addresses 02H through 08H are used as counters for the clock function (seconds up to years counters). Address locations 09H through 0CH contain alarm registers which define the conditions for an alarm. Address 0DH controls the CLKOUT output frequency. 0EH and 0FH are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

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8.1 Alarm function modes

By clearing the MSB of one or more of the alarm registers (bit AE = alarm enable), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the Alarm Flag (AF). The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF can only be cleared by software.

8.2 Timer

The 8-bit countdown timer at address 0FH is controlled by the timer control register at address 0EH. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $^1/_{60}$ Hz), and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the Timer Flag (TF). The TF may only be cleared by software. The asserted TF can be used to generate an Interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. Bit TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

8.3 CLKOUT output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the CLKOUT control register at address 0DH. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

8.4 Reset

The PCA8565 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE which are set to logic 1.

8.5 Voltage-low detector

The PCA8565 has an on-chip voltage-low detector. When V_{DD} drops below V_{low}, bit VL in the seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software.

Bit VL is intended to detect the situation when V_{DD} is decreasing slowly, for example under battery operation. Should V_{DD} reach V_{low} before power is re-asserted then bit VL will be set. This will indicate that the time may be corrupted.

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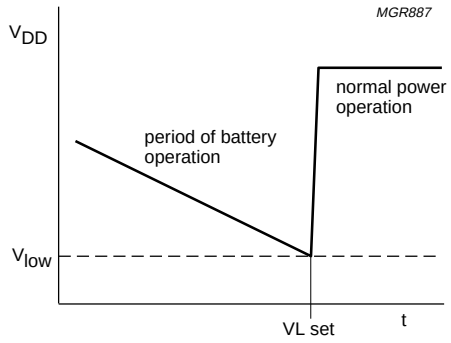

Fig 4. Voltage-low detection.

8.6 Register organization

Table 4: Binary formatted registers overview

Bit positions labelled as x are not implemented, those labelled with 0 should always be written with logic 0.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	control/status 1	TEST1	0	STOP	0	TESTC	0	0	0
01H	control/status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
0DH	CLKOUT control	FE	x	x	x	x	x	FD1	FD0
0EH	timer control	TE	x	x	x	x	x	TD1	TD0
0FH	timer	<timer countdown value>							

Table 5: BCD formatted registers overview

Bit positions labelled as x are not implemented.

Address	Register name	BCD format tens nibble				BCD format units nibble			
		Bit 7 2^3	Bit 6 2^2	Bit 5 2^1	Bit 4 2^0	Bit 3 2^3	Bit 2 2^2	Bit 1 2^1	Bit 0 2^0
02H	seconds	VL	<seconds 00 to 59 coded in BCD>						
03H	minutes	x	<minutes 00 to 59 coded in BCD>						
04H	hours	x	x	<hours 00 to 23 coded in BCD>					
05H	days	x	x	<days 01 to 31 coded in BCD>					
06H	weekdays	x	x	x	x	x	<weekdays 0 to 6>		
07H	months/century	C	x	x	<months 01 to 12 coded in BCD>				
08H	years	<years 00 to 99 coded in BCD>							
09H	minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
0AH	hour alarm	AE	x	<hour alarm 00 to 23 coded in BCD>					
0BH	day alarm	AE	x	<day alarm 01 to 31 coded in BCD>					
0CH	weekday alarm	AE	x	x	x	x	<weekday alarm 0 to 6>		

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8.6.1 Control/status 1 register

Table 6: Control/status 1 (address 00H) bits description

Bit	Symbol	Value	Description
7	TEST1	0	Normal mode
		1	EXT_CLK test mode
6	0		default value is logic 0
5	STOP	0	RTC source clock runs
		1	all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
4	0		default value is logic 0
3	TESTC	0	Power-on reset override facility is disabled; set to logic 0 for normal operation
		1	Power-on reset override may be enabled
2 to 0	0		default value is logic 0

8.6.2 Control/status 2 register

Bits TF and AF: When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.

Bits TIE and AIE: These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

Table 7: Control/status 2 (address 01H) bits description

Bit	Symbol	Value	Description
7 to 5	0		default value is logic 0
4	TI/TP	0	$\overline{INT}$ is active when TF is active (subject to the status of TIE)
		1	$\overline{INT}$ pulses active according to Table 8 (subject to the status of TIE); note that if AF and AIE are active then $\overline{INT}$ will be permanently active
3	AF	0 (read)	alarm flag inactive
		1 (read)	alarm flag active
		0 (write)	alarm flag is cleared
		1 (write)	alarm flag remains unchanged
2	TF	0 (read)	timer flag inactive
		1 (read)	timer flag active
		0 (write)	timer flag is cleared
		1 (write)	timer flag remains unchanged
1	AIE	0	alarm interrupt disabled
		1	alarm interrupt enabled
0	TIE	0	timer interrupt disabled
		1	timer interrupt enabled

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Table 8: $\overline{INT}$ operation (bit TI/TP = 1)

Source clock (Hz)	$\overline{INT}$ period (s)[2]	
	n = 1[1]	n > 1
4 096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] TF and INT become active simultaneously.

[2] n = loaded countdown value. Timer stopped when n = 0.

8.6.3 Time and date registers

Table 9: Seconds/VL (address 02H) bits description

Bit	Symbol	Value	Description
7	VL	0	clock integrity is guaranteed
		1	integrity of the clock information is no longer guaranteed
6 to 0	seconds	00 to 59	this register holds the current seconds coded in BCD format; example: seconds register contains x101 1001 = 59 seconds

Table 10: Minutes (address 03H) bits description

Bit	Symbol	Value	Description
6 to 0	minutes	00 to 59	this register holds the current minutes coded in BCD format

Table 11: Hours (address 04H) bits description

Bit	Symbol	Value	Description
5 to 0	hours	00 to 23	this register holds the current hours coded in BCD format

Table 12: Days (address 05H) bits description

Bit	Symbol	Value	Description
5 to 0	days[1]	01 to 31	this register holds the current day coded in BCD format

[1] The PCA8565 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

Table 13: Weekdays (address 06H) bits description

Bit	Symbol	Value	Description
2 to 0	weekdays[1]	0 to 6	this register holds the current weekday coded in BCD format, see Table 14

[1] These bits may be re-assigned by the user.

Table 14: Weekday assignments

Day	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1

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Table 14: Weekday assignments *...continued*

Day	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

Table 15: Months/century (address 07H) bits description

Bit	Symbol	Value	Description
7	century[1]		this bit is toggled when the years register overflows from 99 to 00
		0	indicates the century is 20xx
		1	indicates the century is 19xx
4 to 0	month	01 to 12	this register holds the current month coded in BCD format, see Table 16

[1] These bits may be re-assigned by the user.

Table 16: Month assignments

Month	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	C	x	x	0	0	0	0	1
February	C	x	x	0	0	0	1	0
March	C	x	x	0	0	0	1	1
April	C	x	x	0	0	1	0	0
May	C	x	x	0	0	1	0	1
June	C	x	x	0	0	1	1	0
July	C	x	x	0	0	1	1	1
August	C	x	x	0	1	0	0	0
September	C	x	x	0	1	0	0	1
October	C	x	x	1	0	0	0	0
November	C	x	x	1	0	0	0	1
December	C	x	x	1	0	0	1	0

Table 17: Years (address 08H) bits description

Bit	Symbol	Value	Description
7 to 0	years	00 to 99	this register holds the current year coded in BCD format

8.6.4 Alarm registers

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding bit Alarm Enable (AE) is logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their bit AE at logic 1 will be ignored.

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Table 18: Minute alarm (address 09H) bits description

Bit	Symbol	Value	Description
7	AE	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	alarm minutes	00 to 59	this register holds the minute alarm information coded in BCD format

Table 19: Hour alarm (address 0AH) bits description

Bit	Symbol	Value	Description
7	AE	0	hour alarm is enabled
		1	hour alarm is disabled
5 to 0	alarm hours	00 to 23	this register holds the hour alarm information coded in BCD format

Table 20: Day alarm (address 0BH) bits description

Bit	Symbol	Value	Description
7	AE	0	day alarm is enabled
		1	day alarm is disabled
5 to 0	alarm days	01 to 31	this register holds the day alarm information coded in BCD format

Table 21: Weekday alarm (address 0CH) bits description

Bit	Symbol	Value	Description
7	AE	0	weekday alarm is enabled
		1	weekday alarm is disabled
2 to 0	alarm weekdays	0 to 6	this register holds the weekday alarm information coded in BCD format

8.6.5 CLOCKOUT control register

Table 22: CLKOUT control (address 0DH) bits description

Bit	Symbol	Value	Description
7	FE	0	the CLKOUT output is inhibited and CLKOUT output is set to high-impedance
		1	the CLKOUT output is activated
1 to 0	FD1 and FD0		these bits control the frequency output at pin CLKOUT, see Table 23

Table 23: FD1 and FD0: CLKOUT frequency selection

FD1	FD0	CLKOUT frequency
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

8.6.6 Countdown timer

The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register bit TE. The source clock for the timer is also selected by the timer control register. Other timer properties such as interrupt generation are controlled via control/status 2 register.

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For accurate read back of the countdown value, the I^2C-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock.

Table 24: Timer control (address 0EH) bits description

Bit	Symbol	Value	Description
7	TE	0	timer is disabled
		1	timer is enabled
1 to 0	TD1 and TD0		timer source clock frequency select; these bits determine the source clock for the countdown timer, see Table 25; when not in use, TD1 and TD0 should be set to $1/16$ Hz for power saving

Table 25: TD1 and TD0: Timer frequency selection

TD1	TD0	TIMER Source clock frequency
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	$1/60$ Hz

Table 26: Timer (address 0FH) bits description

Bit	Symbol	Value	Description
7 to 0	timer	00 to FF	countdown value = n; $CountdownPeriod = \frac{n}{SourceClockFrequency}$

8.7 EXT_CLK test mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in control/status1 register. Then pin CLKOUT becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using bit STOP. When bit STOP is set, the pre-scaler is reset to 0 (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

Operation example:

1. Set EXT_CLK test mode (control/status 1, bit TEST1 = 1)
2. Set STOP (control/status 1, bit STOP = 1)

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3. Clear STOP (control/status 1, bit STOP = 0)
4. Set time registers to desired value
5. Apply 32 clock pulses to CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to CLKOUT
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.8 Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I^2C-bus pins, SDA and SCL, be toggled in a specific order as shown in Figure 5. All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I^2C-bus access. The override mode may be cleared by writing a logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.

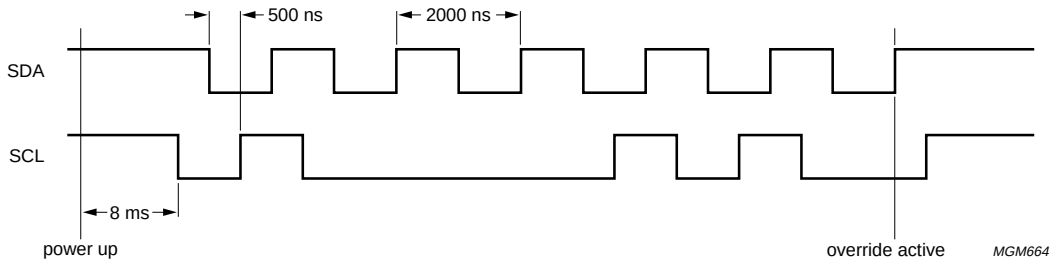

Fig 5. POR override sequence.

9. Characteristics of the I^2C-bus

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 6).

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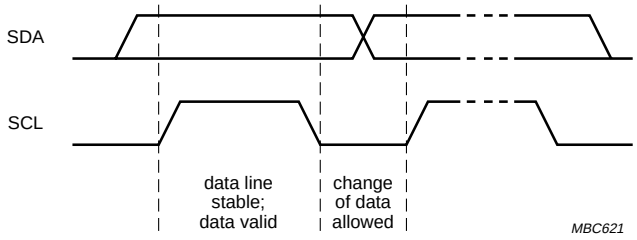

Fig 6. Bit transfer.

9.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P), see Figure 7.

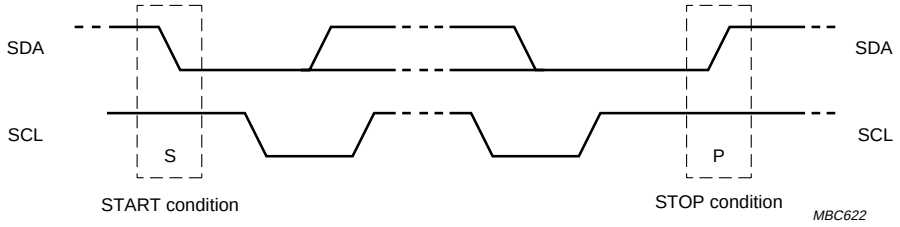

Fig 7. Definition of start and stop conditions.

9.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

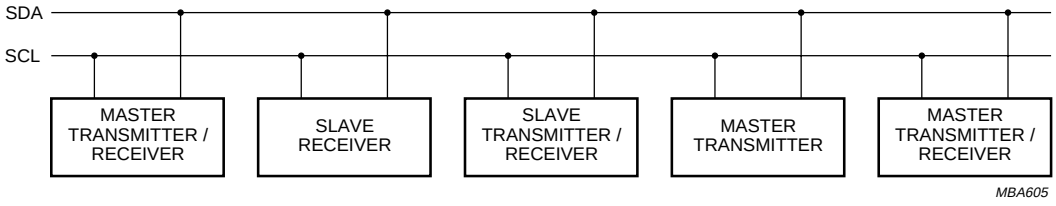

Fig 8. System configuration.

9.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related

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clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

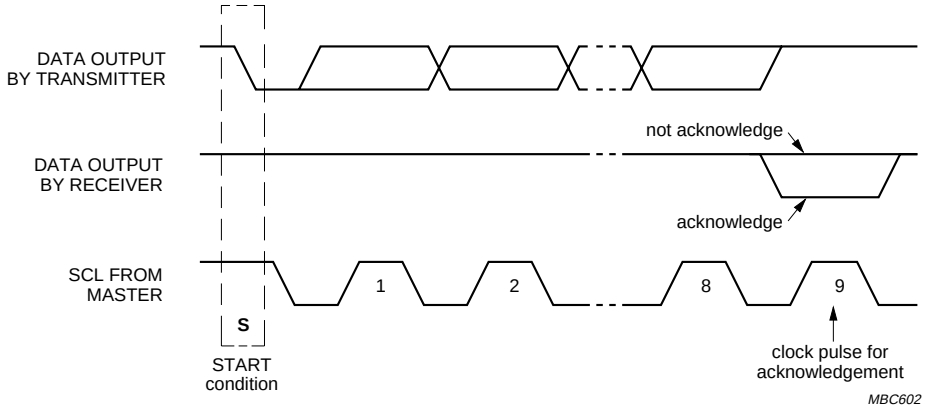

Fig 9. Acknowledgement on the I²C-bus.

9.5 I²C-bus protocol

9.5.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCA8565 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCA8565 slave address is shown in Figure 10.

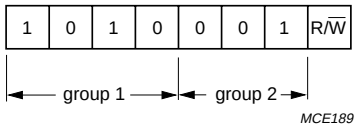

Fig 10. Slave address.

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9.5.2 Clock/calendar read/write cycles

The I²C-bus configuration for the different PCA8565 read and write cycles is shown in Figure 11, Figure 12 and Figure 13. The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

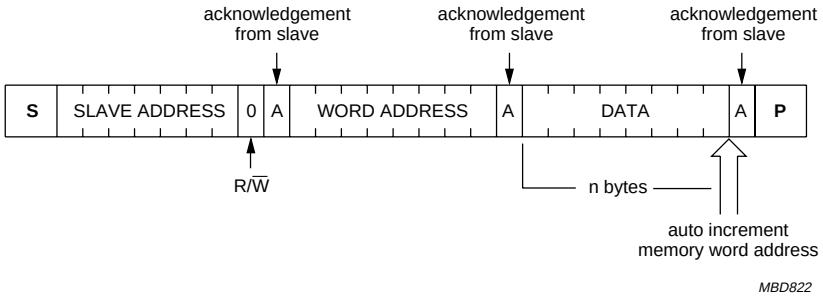

Fig 11. Master transmits to slave receiver (write mode).

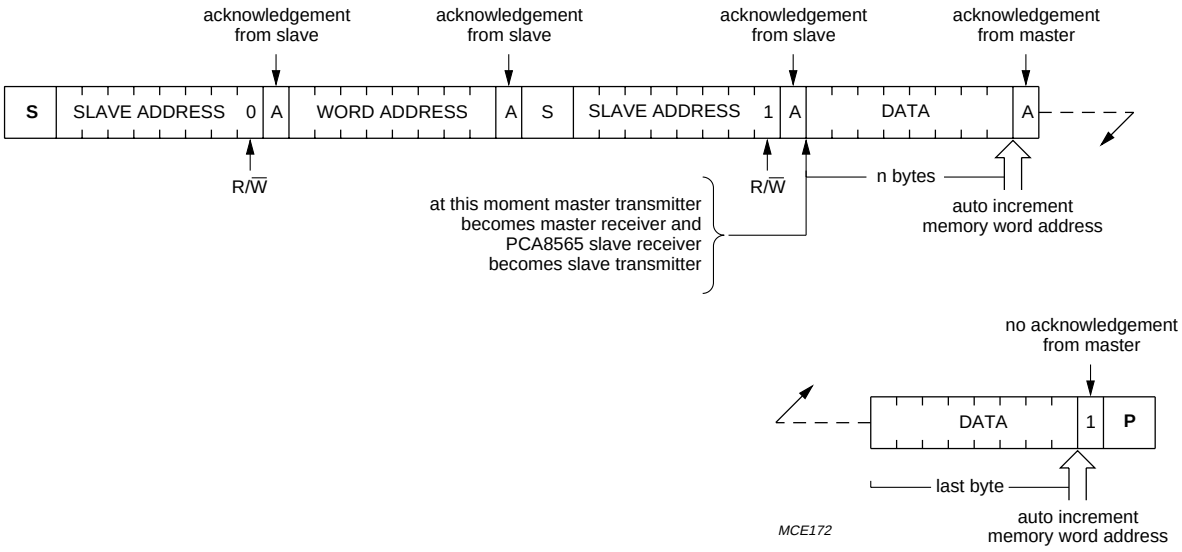

Fig 12. Master reads after setting word address (write word address; read data).

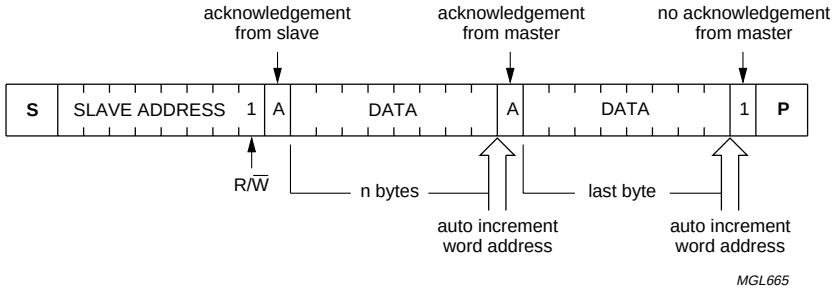

Fig 13. Master reads slave immediately after first byte (read mode).

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10. Limiting values

Table 27: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DD}	supply voltage	–0.5	+6.5	V
I_{DD}	supply current	–50	+50	mA
I_{SS}	supply current	–50	+50	mA
V_I	input voltage			
	for pins SCL and SDA	–0.5	+5.5	V
	for any other input	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	-	300	mW
T_{amb}	ambient temperature	–40	+125	°C
T_{stg}	storage temperature	–65	+150	°C

11. Static characteristics

Table 28: Static characteristics

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.8	-	5.5	V
$V_{DD(clock)}$	supply voltage for clock data integrity		V_{low}	-	5.5	V
I_{DD1}	supply current 1	interface active				
		f_{SCL} = 400 kHz	-	-	820	µA
		f_{SCL} = 100 kHz	-	-	220	µA
I_{DD2}	supply current 2	interface inactive (f_{SCL} = 0 Hz); CLKOUT disabled; T_{amb} = 25 °C [1]				
		V_{DD} = 5.0 V	-	750	1500	nA
		V_{DD} = 4.0 V	-	700	1400	nA
		V_{DD} = 3.0 V	-	650	1300	nA
		V_{DD} = 2.0 V	-	600	1200	nA
		V_{DD} = 5.0 V; T_{amb} = 125 °C [2]	-	750	5000	nA

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Table 28: Static characteristics *…continued*

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD3}	supply current 3	interface inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = 25 °C	[3]				
		V_{DD} = 5.0 V		-	1000	2000	nA
		V_{DD} = 4.0 V		-	900	1800	nA
		V_{DD} = 3.0 V		-	800	1600	nA
		V_{DD} = 2.0 V		-	700	1400	nA
		V_{DD} = 5.0 V;T_{amb} = 125 °C	[2]	-	1000	6000	nA
Inputs							
V_{IL}	LOW-level input voltage			V_{SS} − 0.3	-	0.3V_{DD}	V
$V_{IH(SCL)}$	SCL HIGH-level input voltage			0.7V_{DD}	-	5.5	V
$V_{IH(SDA)}$	SDA HIGH-level input voltage			0.7V_{DD}	-	5.5	V
$V_{IH(OSCI)}$	OSCI HIGH-level input voltage			0.7V_{DD}	-	V_{DD} + 0.3	V
$I_{LI(SCL)}$	SCL input leakage current	V_I = V_{DD} or V_{SS}		−1	0	+1	µA
$I_{LI(SDA)}$	SDA input leakage current	V_I = V_{DD} or V_{SS}		−1	0	+1	µA
C_i	input capacitance		[4]	-	-	7	pF
Outputs							
$I_{OL(SDA)}$	SDA LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V		−3	-	-	mA
$I_{OL(\overline{INT})}$	$\overline{INT}$ LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V		−1	-	-	mA
$I_{OL(CLKOUT)}$	CLKOUT LOW-level output current	V_O = V_{DD} or V_{SS}		−1	-	-	mA
I_{LO}	output leakage current			−1	0	+1	µA
Voltage detector							
V_{low}	low voltage detection			-	0.9	1.7	V
Temperature							
T_{amb}	ambient temperature			−40		+125	°C

[1] Timer source clock = $\frac{1}{60}$ Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

[2] Worst case is at high temperature and high supply voltage.

[3] Timer source clock = $\frac{1}{60}$ Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

[4] Tested on sample basis.

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12. Dynamic characteristics

Table 29: Dynamic characteristics

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 125 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
C_{INT}	integrated load capacitance		15	25	35	pF
$\Delta f_{osc}/f_{osc}$	oscillator stability	ΔV_{DD} = 200 mV; T_{amb} = 25 °C	-	2×10^{-7}	-	-
Quartz crystal parameters (f = 32.768 kHz)						
R_S	series resistance		-	-	40	kΩ
C_L	parallel load capacitance		-	10	-	pF
C_T	trimmer capacitance		5	-	25	pF
CLKOUT output						
δ_{CLKOUT}	CLKOUT duty cycle	[1]	-	50	-	%
Timing characteristics: I²C-bus[2][3]						
f_{SCL}	SCL clock frequency	[4]	-	-	400	kHz
$t_{HD;STA}$	START condition hold time		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
t_{LOW}	SCL LOW time		1.3	-	-	µs
t_{HIGH}	SCL HIGH time		0.6	-	-	µs
t_r	SCL and SDA rise time		-	-	0.3	µs
t_f	SCL and SDA fall time		-	-	0.3	µs
C_b	capacitive bus line load		-	-	400	pF
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{SW}	tolerable spike width on bus		-	-	50	ns

[1] Unspecified for f_{CLKOUT} = 32.768 kHz.

[2] All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[3] A detailed description of the I²C-bus specification, with applications, is given in brochure *The I²C-bus and how to use it.* This brochure may be ordered using the code 9398 393 40011.

[4] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

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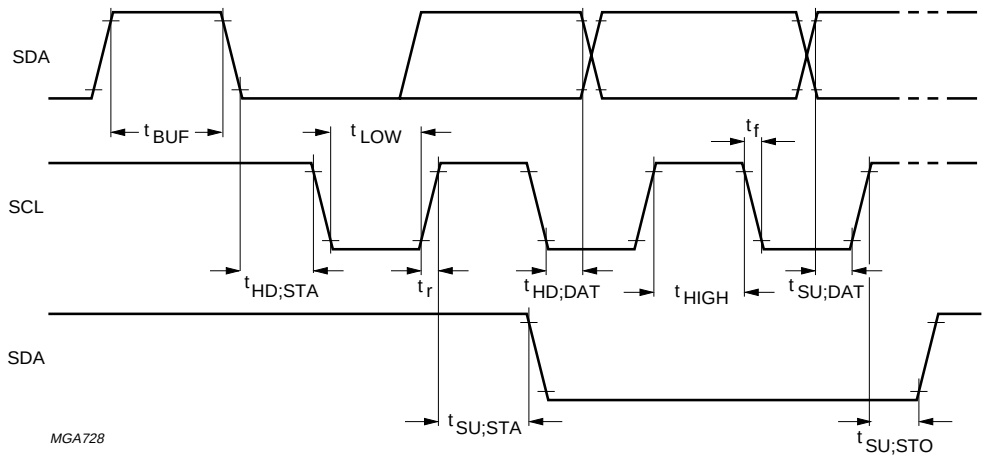
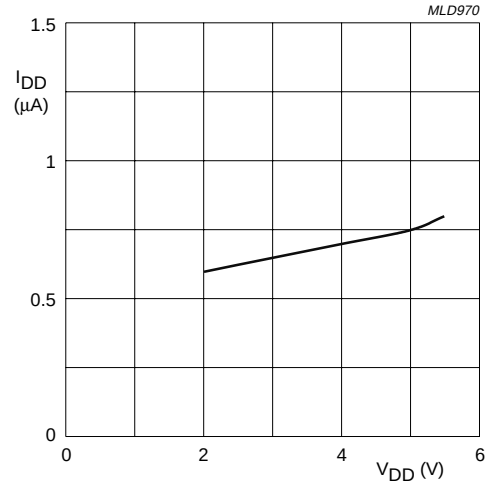
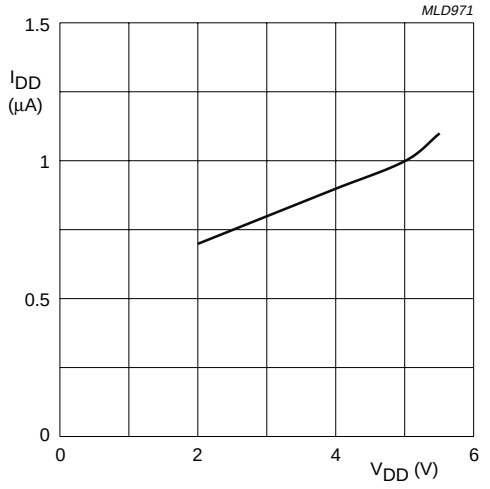


Fig 14. I²C-bus timing waveforms.



T_{amb} = 25 °C; Timer = 1 minute.

Fig 15. I_{DD} as a function of V_{DD}; CLKOUT disabled.



T_{amb} = 25 °C; Timer = 1 minute.

Fig 16. I_{DD} as a function of V_{DD}; CLKOUT = 32 kHz.

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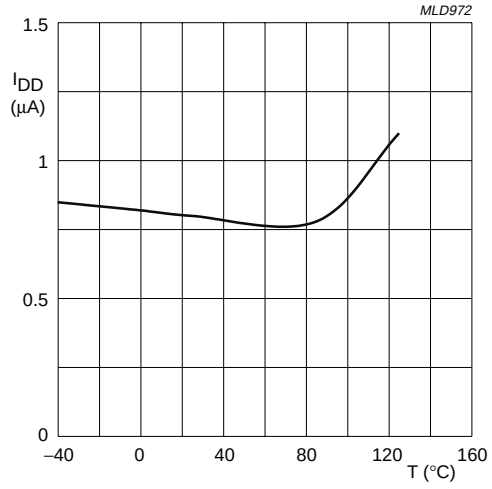
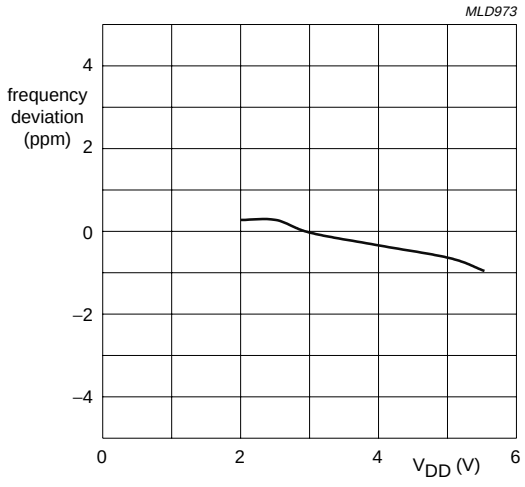


V_{DD} = 3 V; Timer = 1 minute.

Fig 17. I_{DD} as a function of T; CLKOUT = 32 kHz.



T_{amb} = 25 °C; normalized to V_{DD} = 3 V.

Fig 18. Frequency deviation as a function of V_{DD}.

13. Application information

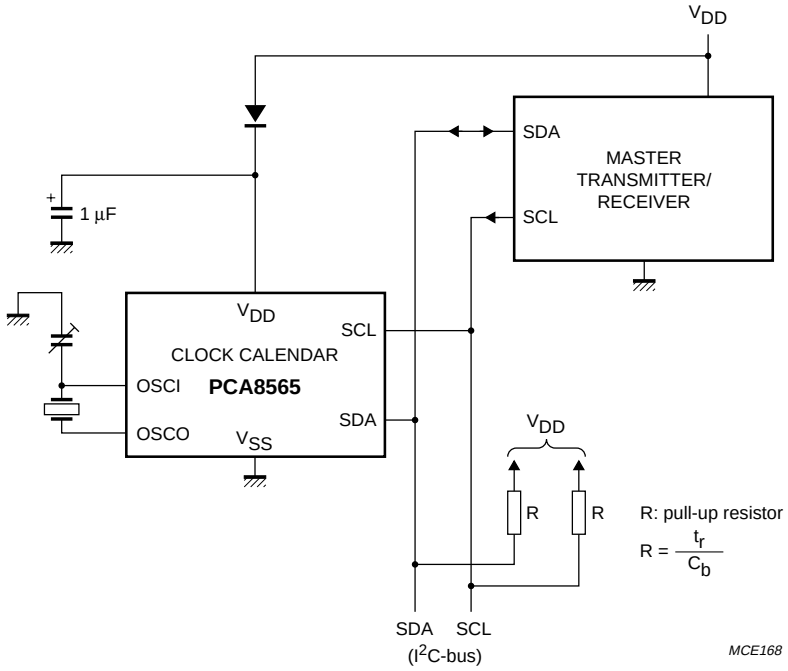


Fig 19. Application diagram.

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13.1 Quartz frequency adjustment

13.1.1 Method 1: fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout, a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at pin CLKOUT. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be easily achieved.

13.1.2 Method 2: OSCI trimmer

Using the 32.768 kHz signal available after power-on at pin CLKOUT, fast setting of a trimmer is possible.

13.1.3 Method 3: OSCO output

Direct measurement of OSCO out (accounting for test probe capacitance).

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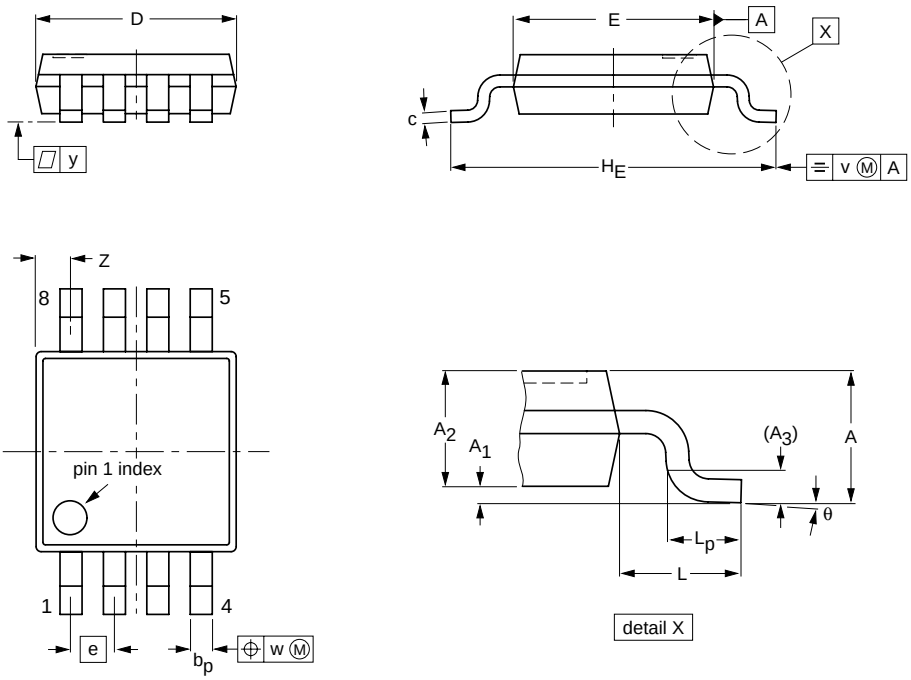
14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

Fig 20. Package outline.

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15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5mm and packages with a thickness <2.5 mm and a volume ≥350 mm^3 so called thick/large packages
- below 235 °C for packages with a thickness <2.5 mm and a volume <350 mm^3 so called small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

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- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Package related soldering information

Table 30: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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16. Revision history

Table 31: Revision history

Rev	Date	CPCN	Description
01	20030331	-	Product data (9397 750 10695)

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17. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

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