DATA SHEET

PCF5079
Dual-band power amplifier controller for GSM, PCN and DCS

Product specification
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Dual-band power amplifier controller for GSM, PCN and DCS

PCF5079

1 FEATURES

- Compatible with baseband interface family PCF5073x
- Two power sensor inputs
- Temperature compensation of sensor signal
- Active filter for Digital-to-Analog Converter (DAC) input
- Power Amplifier (PA) protection against mismatching
- Bias current source for detector diodes
- Generation of pre-bias level for PA at start of burst (home position)
- Compatible with a wide range of silicon PAs
- Compatible with multislot class 12
- Dual output with internal switch
- Two different transfer functions
- Possibility to adapt dynamic transfer functions
- Very small outline package (3×3 mm).

2 APPLICATIONS

- Global System for Mobile communication (GSM)
- Personal Communications Network (PCN) systems.

3 GENERAL DESCRIPTION

This CMOS device integrates an amplifier for the detected RF voltage from the sensor, an integrator and an active filter to build a PA control loop for cellular systems with a small number of passive components.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	2.5	3.6	5.0	V
$I_{DD(tot)}$	total supply current	–	–	10	mA
T_{amb}	ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5079T/C/1	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1
PCF5079HK/C/1	HVSON10	plastic, heatsink very thin small outline package; no leads; 10 terminals; body $3 \times 3 \times 0.90$ mm	SOT650-1

5 BLOCK DIAGRAM

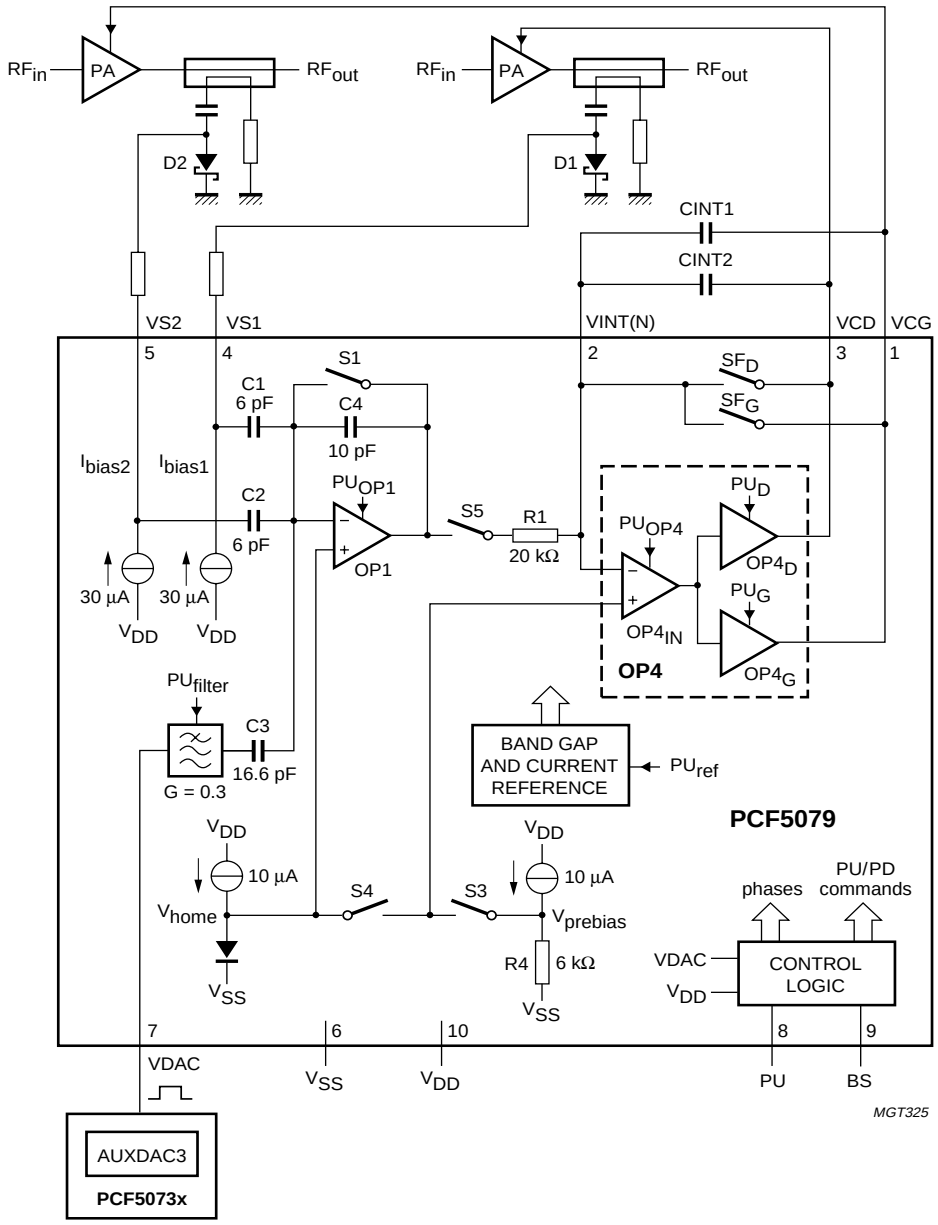


Fig.1 Block diagram.

6 PINNING

6.1 Pin description

SYMBOL	PIN	TYPE(1)	DESCRIPTION
VCG	1	O and A	PA control voltage output (GSM)
VINT(N)	2	I and A	negative integrator input
VCD	3	O and A	PA control voltage (DCS)
VS1	4	I/O and A	sensor signal input 1
VS2	5	I/O and A	sensor signal input 2
V_{SS}	6	G	reference ground
VDAC	7	I and A	DAC input voltage
PU	8	I and D	power-up input
BS	9	I and D	band selection input
V_{DD}	10	P	positive supply voltage

Note

1. O = output, I = input, I/O = input/output, A = analog, D = digital, P = power supply and G = ground

6.2 Pin configurations

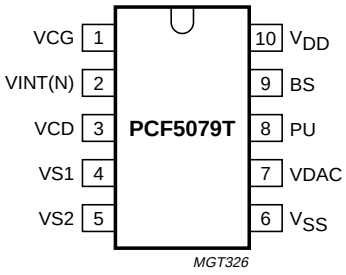


Fig.2 Pin configuration (top view) for PCF5079T, pins are numbered counter-clockwise.

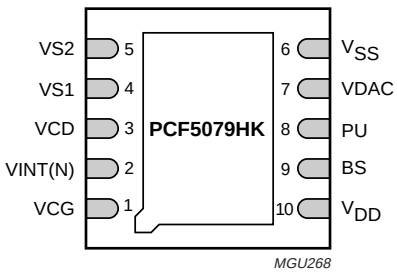


Fig.3 Pin configuration (bottom view) for PCF5079HK, pins are numbered clockwise.

7 FUNCTIONAL DESCRIPTION

7.1 General

The PCF5079 contains an integrated amplifier for the detected RF voltage from the sensor, an integrator and an active filter to build up a PA control loop for cellular systems with a small number of passive components suitable for dual-band applications. The active band can be selected by means of the dedicated input BS.

The sensor amplifier can amplify signals from an RF power detector in a range of less than –20 to +15 dBm. This can comply to the PA output power range of GSM900/1800/1900 systems when, for example, a directional coupler with 20 dB attenuation is used for GSM900 and a directional coupler with 18 dB attenuation is used for GSM1800.

The external Schottky diodes for power detection (sensor) are biased by an integrated current source of 30 μA. Variations of the forward voltage with temperature have no influence on the measured signal because they are cancelled by the switched capacitor amplifier OP1.

An external DAC with at least 10-bit resolution (for example, AUXDAC3 of baseband interface family PCF5073x) is necessary to control the loop.

An integrated active filter smooths the voltage steps of the DAC during ramp-up and ramp-down.

The operation principle is the same, independently of the selected standard. The DAC signal and the sensor signal are added by amplifier OP1. The voltage difference of both signals is integrated by operational amplifier OP4 dedicated to the selected standard, which delivers the PA control voltage on an external capacitance, CINT1 or or CINT2, between pins VINT(N) and VCD or VCG, respectively. The shape of the rising and falling power burst edges can be determined by means of the DAC voltage.

7.2 Power-up mode

The device includes a power-up input (pin PU) to switch the IC on during time slots that are used in TDMA systems, and to switch the IC off during the unused slots to reduce current consumption.

7.3 OP4 (integrator)

The operational amplifier OP4 (integrator) consists of a shared input stage, $OP4_{IN}$ and a dedicated output driver for each standard, $OP4_G$ and $OP4_D$. Depending on the status of input BS, one driver is active and the other is kept in power-down mode during active time slots.

7.4 Start-up and initial conditions

The PCF5079 is designed to operate in bursts, as required in TDMA systems. Referring to Fig.4, for each time slot to be transmitted the PCF5079 must be enabled by setting signal PU to logic 1. Once pin PU is active, BS is taken into account to allow correct initialisation of switches S1, SF_D, SF_G, S3, S4 and S5, and of the configuration signals PU_G and PU_D.

The feedback switch across the unused driver is kept open and the output voltage from the unused driver is tied to V_{SS} to maintain the off state of the unused PA.

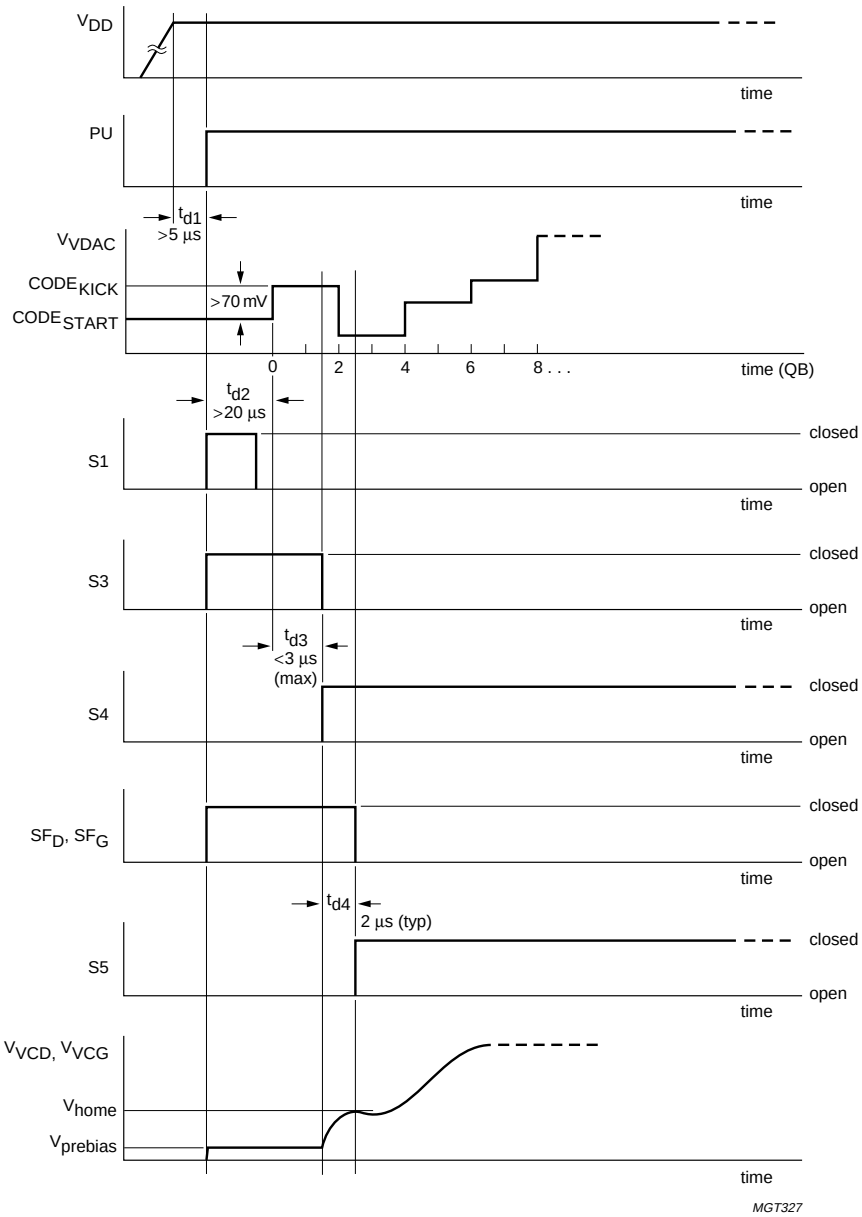
When pin PU is set to logic 1, at least 5 μs after V_{DD} has reached its final value, switches S1, the appropriate switch SF_D or SF_G and S3 are closed, and switches S4 and S5 are opened. Because switch S1 is closed, the forward voltage of Schottky diodes D1 and D2 is sampled on capacitors C1 and C2 respectively.

Moreover, the control voltage on pin VCD or VCG is initially forced to be at the pre-bias voltage because the appropriate switch SF_D or SF_G and S3 are closed, and S4 is opened.

After a fixed time, defined on-chip, switch S1 is opened and the circuit is ready.

Once switch S1 is open, a ramp signal applied at pin VDAC (at least 20 μs after the transition of pin PU from logic 0 to logic 1) with an amplitude of at least 70 mV, from $CODE_{START}$ to $CODE_{KICK}$, determines the opening of switch S3 and closing of switch S4 on the home voltage, with a delay of 3 μs maximum with respect to the ramp. After switch S3 opens (in a fixed amount of time), the control voltage on pin VCD or pin VCG rises to the home position to bias the PA to the beginning of the active range of its control curve. During this time (typically 2 μs), the appropriate switch SF_D or SF_G remains closed. When the appropriate switch SF_D or SF_G is opened, switch S5 is closed, allowing the transfer of any signal coming from amplifier OP1. After this preset, the control voltage is free to increase according to the control loop if the RF input is enabled (see Fig.12).

For higher DAC ramp steps, the delay of switch S3 opening (S4 closing) is reduced while the delay between switch SF_D (SF_G) opening with respect to S3 opening (S4 closing) remains unchanged.



The maximum value of $CODE_{START}$ is limited by the isolation requirement of the PA used in the application. The pulse determined by $CODE_{KICK}$ minus $CODE_{START}$ applied for two quarter-bits ensures a start-up of the control voltage with very low jitter and high repetitivity. The codes following $CODE_{KICK}$ have to be chosen to get the best ramp shape and spectrum performance.

Fig.4 Start-up and initialization timing diagram.

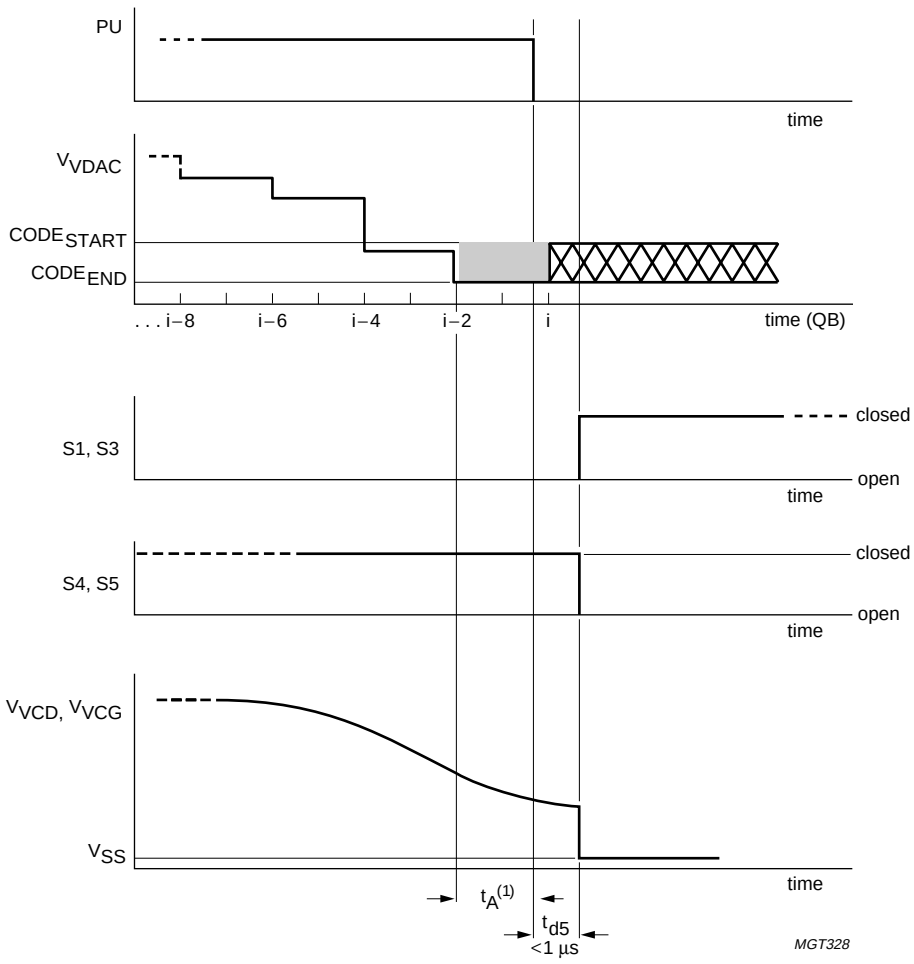
7.5 Home position voltage

Internally, a forward voltage of an on-chip silicon diode is provided as a default home position. This voltage matches the requirements at the control input of most PAs and exhibits the same temperature coefficient.

7.6 End of burst

The ramp-down should drive the PA from conduction to shut off in a controlled way (see Fig.5). To get this result, correct DAC programming is required, so that the last code of the DAC ramp-down ($CODE_{END}$) is lower than the initial code of the ramp-up ($CODE_{START}$). In this way, the energy corresponding to the difference between start and end codes, applied for a certain number of Quarter-Bits (QB), is used to balance the energy stored in the summing node during the time interval between the start of control voltage on pin VCD or VCG ramping-up and the feedback of a detected ramp to the sensor input. Also a very slow ramp-down is avoided when the PA switches off and the loop gain becomes zero.

The amount of energy required at the end of the ramp-down depends on the overall loop gain and on the time needed to reach PA conduction from the home position. At the end of a burst, when pin PU is set to logic 0, control voltage on pin VCD or VCG is forced to V_{SS}.



(1) The exact duration of t_A depends on both PCF5079 and the application loop characteristics. The contribution of PCF5079 is due mainly to the group delay of the low-pass filter on the VDAC input (see Fig.11).

Fig.5 End of burst timing diagram.

7.7 Considerations for ramp-down

Referring to Fig.5, the i-th code can be programmed to have either the $CODE_{END}$ or $CODE_{START}$ value or any code between, depending on the application preferences. These codes do not produce any power at the output of the PA, as $CODE_{START}$ has been chosen to keep the PA isolation. The proper conclusion of the ramp-down is ensured by choosing $CODE_{END} < CODE_{START}$ so that the discharge of the integration capacitance is controlled until the control voltage on pin VCD or VCG goes below the PA conduction threshold and by applying at this time the PU transition from logic 1 to logic 0.

At the beginning of a burst, the VDAC signal steps applied at OP1 are not compensated by any signal at the sensor input up to when pin VCD or VCG voltage is greater than the PA conduction threshold voltage. In any case, the initial DAC voltage steps are stored in the capacitance of amplifier OP1. $CODE_{END}$ has to be chosen so that the energy inside the shaded zone cancels the energy accumulated in the summing node (OP1) at the start of a burst and not balanced by a feedback signal at the sensor input.

The exact value of the energy required depends on the specific PA, on the characteristics of the overall loop and on the values chosen for the settable parameters inside the loop.

A rough idea can be derived with a simplified analysis of a ramp-up, ramp-down cycle using the following simplifications:

- The starting conditions for OP1 and OP4 are biasing at V_{home} with zero charge on capacitances
- The initial rising of pin VCD or VCG voltage from V_{home} is caused only by the integration of the constant $CODE_{KICK}$
- VDAC is treated as applied directly at the summing node, initially neglecting the transmission delay through the internal low-pass filter.

Generally, the integrator OP4 input can be expressed as

$$V_{in(integrator)} = g_s \times \Delta V_s - g_d \times \Delta V_{VDAC} \quad (1)$$

where g_s and g_d are respectively the gains of sensor input and DAC input in the summing amplifier OP1.

Equation (1) holds for closed loop operation. In the time interval between the rising of pin VCD or VCG voltage due to $CODE_{KICK}$ (t = 0) and when $V_{conduction}$ for the PA is reached ($t = t_1$), ΔV_s is 0 and operation is open loop. In this time interval, a charge accumulates in the summing node, which remains uncompensated.

Time t_1 can be calculated with the preceding simplification. Now, to define the quantity

$$\Delta V_{KICK} = CODE_{KICK} - CODE_{START} \quad (2)$$

the current/voltage equations around the integrator OP4 can be solved by forcing the current through R1 to be equal to the current through the integration capacitance and calculating the ΔV generated on C_{INT}, then

$$\Delta V_{CINT} = \frac{1}{C_{CINT}} \times \int_0^t i(\tau) d\tau \quad (3)$$

where

$$i(\tau) = \frac{g_d \times \Delta V_{KICK}}{R1} \quad (4)$$

Substituting equation (4) into equation (3)

$$\Delta V_{CINT} = \frac{1}{C_{CINT} \times R1} \times \int_0^t g_d \times \Delta V_{KICK} d\tau \quad (5)$$

Under the hypothesis the voltage is constant:

$$\Delta V_{CINT} = \frac{1}{C_{CINT} \times R1} \times g_d \times \Delta V_{KICK} \times t \quad (6)$$

Equation (6) can be used to calculate time t_1 at which the conduction of the PA is reached, considering that

$$t = t_1 \Rightarrow V_{home} + \Delta V_{CINT} = V_{conduction} \quad (7)$$

$$t_1 = R1 \times C_{CINT} \times \frac{V_{conduction} - V_{home}}{g_d \times \Delta V_{KICK}} \quad (8)$$

Time t_1 depends on the time constant of the integrator, by the PA and by ΔV_{KICK}. The condition to be fulfilled is that the energy contained in the shaded zone (Fig.5) is at least equal to the energy accumulated at the beginning:

$$\int_0^{t_1} V_{out_{OP1}}^2 (t)\, dt = k \times QB \times (CODE_{END} - CODE_{START})^2 \quad (9)$$

where k is the number of quarter-bits during which $CODE_{END}$ is applied.

7.8 Configurations

Table 1 Operating conditions

POWER-UP INPUT (PU)	OPERATING MODE
0	disabled; reset
1	enabled

Table 2 Band selection configuration

BAND SELECT INPUT (BS)(1)	BAND	DRIVER	SWITCHES	CONTROL VOLTAGE
0	GSM	OP4G → active; OP4D → power-down	SF_G → working; SF_D → open	V_{VCG} → working; V_{VCD} → V_{SS}
1	DCS	OP4D → active; OP4G → power-down	SF_D → working; SF_G → open	V_{VCD} → working; V_{VCG} → V_{SS}

Note

1. BS input has to be set before the PU transition logic 0 to logic 1.

7.9 Summary of current and voltage definitions

Refer to Figs 1, 4 and 12.

SYMBOL	DESCRIPTION
V_{VS1}	sensor signal of incident RF power or power sensor 1 signal
V_{VS2}	sensor signal of reflected RF wave or power sensor 2 signal
V_{VDAC}	DAC voltage
V_{VCG}	control voltage of PA
V_{VCD}	control voltage of PA
V_{home}	home position voltage
$V_{prebias}$	prebias reference voltage; used at the start-up
I_{bias1}	bias current for detector diode D1
I_{bias2}	bias current for detector diode D2
RF_{in}	input signal to the power amplifier
RF_{out}	output signal from the power amplifier

7.10 Timing

Refer to Figs 4 and 5.

SYMBOL	DEFINITION	MIN.	MAX.	UNIT
t_{d1}	delay time; V_{DD} application to PU input transition logic 0 to 1	5.0	–	µs
t_{d2}	delay time; PU input transition logic 0 to 1 to V_{VDAC} ramp-up	20	–	µs
t_{d3}	V_{VDAC} ramp-up detection time	–	3.0	µs
t_{d4}	delay time; ramp-up detected to V_{VCD}, $V_{VCG} = V_{home}$	–	2.6	µs
t_{d5}	delay time; PU input transition logic 1 to 0 to end of burst	–	1.0	µs

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	+6.0	V
V_I	DC input voltage on all pins except VS1 and VS2		–0.5	V_{DD} + 0.5	V
V_{VS1}, V_{VS2}	DC input voltage on pins VS1 and VS2		–3.0	V_{DD} + 0.5	V
I_I	DC current into any signal pin		–10	+10	mA
P_{tot}	total power dissipation				
	TSSOP10 package		–	315(1)	mW
	HVSON10 package		–	844(2)	mW
V_{es}	electrostatic handling voltage	human body model; note 3	2000	–	V
		machine model; note 4			
		pins 4 and 5	150	–	V
		all other pins	200	–	V
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

Notes

1. Where $P_{tot} = \frac{T_j - T_{amb}}{R_{th(j-a)}}$ and the thermal resistance between junction and ambient $R_{th(j-a)}$ = 206.3 K/W.
2. Where $R_{th(j-a)}$ = 77 K/W on JEDEC 2S2P board (100 × 100 mm).
3. Human body model: C = 100 pF; R = 1.5 kΩ.
4. Machine model: C = 200 pF; L = 0.75 μH; R = 0 Ω.

9 ELECTROSTATIC DISCHARGE (ESD)

The PCF5079 is compliant to the General Quality Specification for integrated circuits *"SNW-FQ-611D"* under the stress condition EDSH (human body) and the stress condition ESDM (machine model).

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	3.6	5.0	V
$I_{DD(op)}$	total operating current	no load on pins VCD or VCG	–	–	10	mA
$I_{DD(idle)}$	total idle current	no load on pins VCD or VCG; note 1	–	–	10	μA
Logic inputs (pins PU and BS)						
V_{IL}	LOW-level input voltage		0	–	0.3	V
V_{IH}	HIGH-level input voltage	V_{DD} = 2.5 to 3.7 V	0.9	–	V_{DD}	V
		V_{DD} = 3.7 to 5.0 V	0.95	–	V_{DD}	V
I_{LL}	LOW-level input leakage current	V_{IL} = 0 V	–5	–	+5	μA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LH}	HIGH-level input leakage current	V_{IH} = 5.0 V	–5	–	+5	µA
C_I	input capacitance		–	10	–	pF
Sensor inputs and bias current source (pins VS1 and VS2)						
V_{VS2}	input voltage		–3	–	V_{DD}	V
V_{VS1}	input voltage		–3	–	V_{DD}	V
I_{bias1}, I_{bias2}	bias current source for detector diodes D1 and D2	V_I = 0 V; T_{amb} = 25 °C; see Fig.6				
		V_{DD} = 2.5 V	17	28	39	µA
		V_{DD} = 5.0 V	21	33	45	µA
TC_{Ibias1}, TC_{Ibias2}	temperature coefficient of I_{bias1} and I_{bias2}		–	0.07	–	mA/K
Internal home position voltage						
V_{home}	internal home position voltage	T_{amb} = 25 °C	0.550	0.600	0.650	V
TC_{Vhome}	temperature coefficient for V_{home}		–	–2.1	–	mV/K

Note

1. A resistive load on pins VCD or VCG to ground (V_{SS}) does not result in additional current consumption.

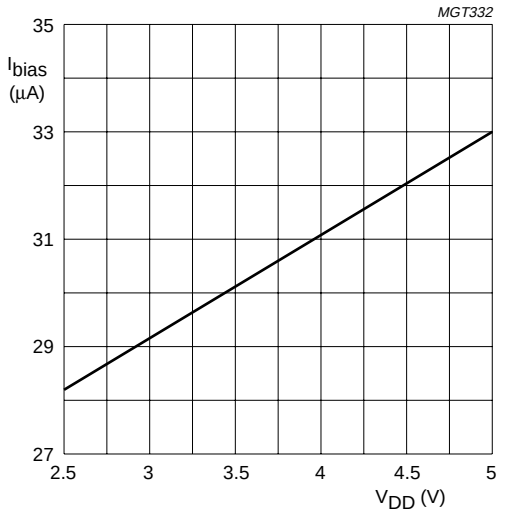


Fig.6 Typical value of I_{bias} as a function of V_{DD} at T_{amb} = 25 °C.

11 OPERATING CHARACTERISTICS

V_{DD} = 2.5 to 5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Integrator (OP4G and OP4D)						
V_{DD}	supply voltage		2.5	3.6	5.0	V
B_G	gain bandwidth	C_L = 120 pF; note 1	–	4	–	MHz
PSRR	power supply ripple rejection	f = 217 Hz; V_{DD} = 3 V; note 1	50	55	–	dB
SR_{pos}	positive slew rate	V_{DD} = 3 V; note 2	2.0	3.2	–	V/µs
SR_{neg}	negative slew rate	V_{DD} = 3 V; note 2	2.0	3.2	–	V/µs
$V_{O(min)}$	minimum output voltage	T_{amb} = 25 °C; see Fig.7	–	–	0.2	V
$V_{O(max)}$	maximum output voltage	R_L = 350 Ω; see Fig.8	$0.85V_{DD}$	–	–	V
Capacitors C1, C2 and C4						
M	matching ratio accuracy between C1, C2 and C4		–	1	–	%
Low-pass filter for DAC signal (3rd-order Bessel filter)						
f_{3dB}	corner frequency		70	100	130	kHz
$t_{d(group)}$	group delay time	see Fig.11	1.8	3.0	4.2	µs

Notes

1. Guaranteed by design.
2. Slew rates are measured between 10% and 90% of output voltage interval with a load of 40 pF to ground.

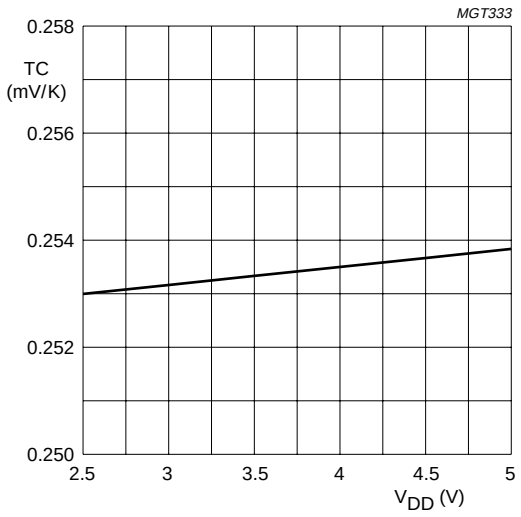


Fig.7 Temperature coefficient of $V_{O(min)}$ as a function of V_{DD}.

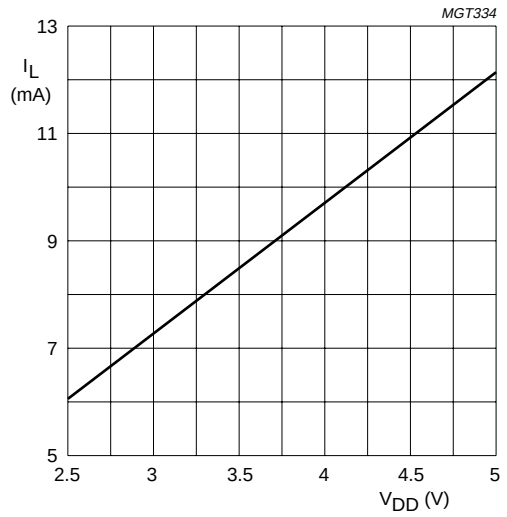
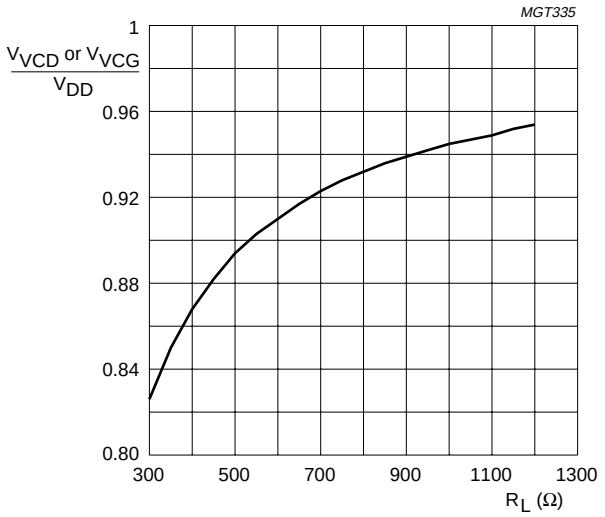
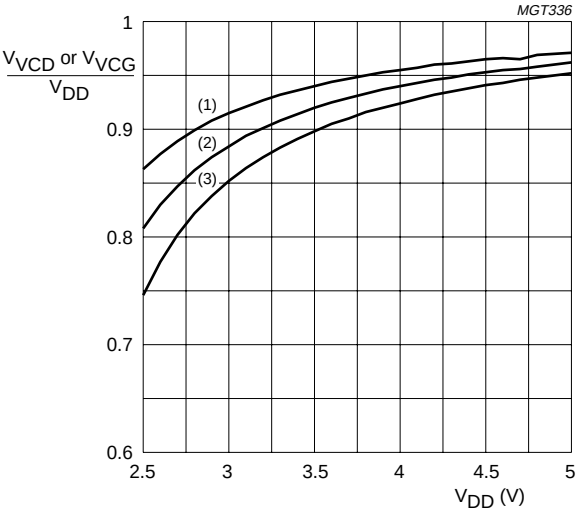


Fig.8 Minimum load current as a function of V_{DD}.



V_{DD} = 2.5 V.

Fig.9 Minimum $\frac{V_{VCD} \text{ or } V_{VCG}}{V_{DD}}$ as a function of R_L.



(1) I_L = 6 mA.
(2) I_L = 8 mA.
(3) I_L = 10 mA.

Fig.10 Minimum $\frac{V_{VCD} \text{ or } V_{VCG}}{V_{DD}}$ as a function of V_{DD}.

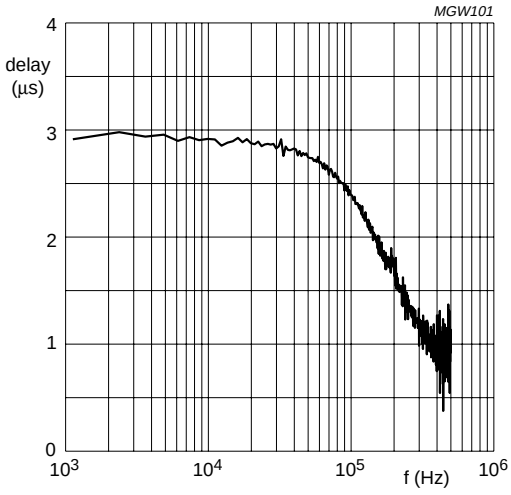
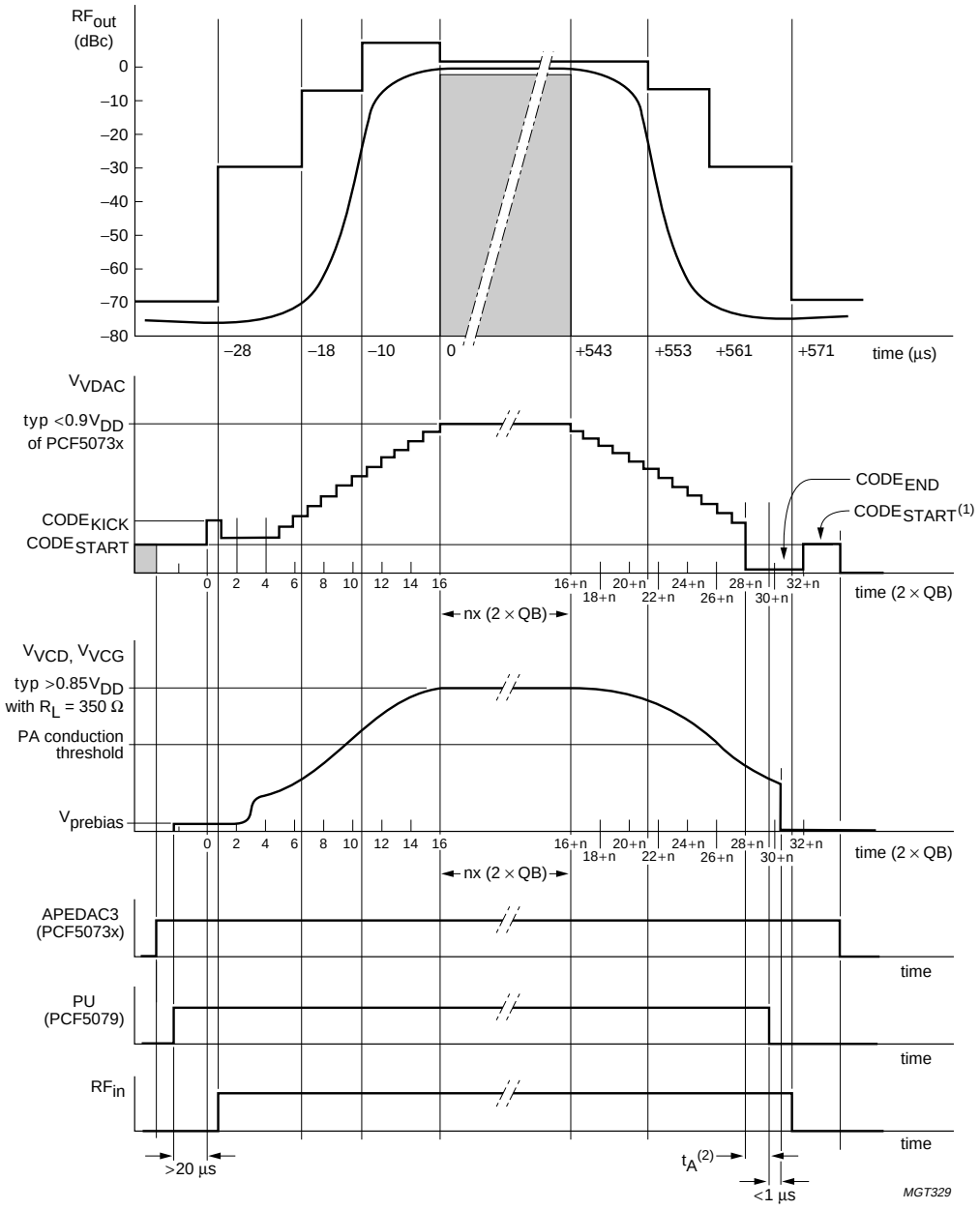


Fig.11 Low-pass filter group delay at pins VCD and VCG (typical values).

12 APPLICATION INFORMATION



(1) The software design must guarantee that $CODE_{START}$ is applied before the PU transition from logic 0 to logic 1.

(2) The exact duration of t_A depends on both PCF5079 and the application loop characteristics. The duration should be long enough to ensure that V_{VCD}, V_{VCG} is below the PA conduction threshold. The contribution of PCF5079 is mainly due to the group delay of the low-pass filter on the VDAC input (see Fig.11).

Fig.12 Timing diagram for one time slot with PCF5073x family.

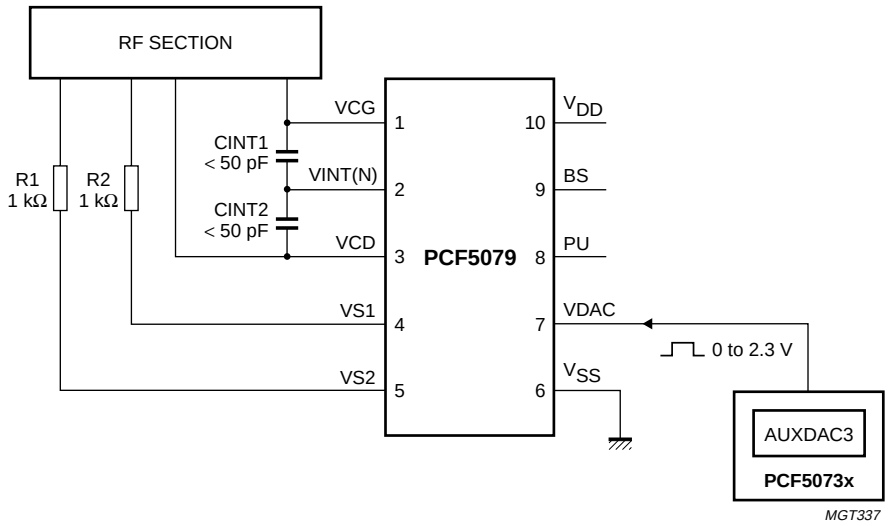


Fig.13 Diagram showing external components required.

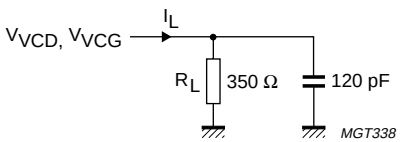


Fig.14 Worst case load on control voltage pins VCG and VCD.

12.1 Ramp control

$CODE_{KICK}$ and V_{home} define the starting conditions for ramping-up. Ramping-up and ramping-down are defined by V_{VDAC}. $CODE_{END}$ and $CODE_{START}$ define the correct shut-off of the power module.

The non-linear behaviour of the control curves of the power modules has a large influence on the loop. Starting conditions in the flat area of the control curve are critical and need some attention. Initially the voltage on pins VCD (VCG) will be at the home position. Successively, the integrator is moved into the active part of the control curve.

This is achieved by integrating $CODE_{KICK}$. When VCD (VCG) voltage has reached the active region of the control curve, the loop is closed and the circuit can follow the ramping function generated at pin VDAC. The top value of VDAC voltage determines the power of the transmit burst. Ramping-down is started according to the decrease of VDAC voltage. The loop follows the leading function for ramping-down until the RF sensor leaves its active region. The reason for $CODE_{START}$ and $CODE_{END}$ is to shorten the tail of the slope.

12.2 PA protection against mismatch

High VSWR at the PA output may occur in systems where the PA is connected to the antenna via couplers and switches with low insertion loss, depending on the antenna matching. The incident and reflected power have to be monitored and care has to be taken to prevent the summed RF power does not exceed the defined maximum value at the PA output.

As two sensor inputs are available in the PCF5079, two different detector signals can be combined: one for direct path and one for reflected path. These two voltages, fed to the sensor inputs, are summed inside the PCF5079 resulting in a decrease in the PA output power if there is an increase of the VSWR at the antenna port (see Fig.15).

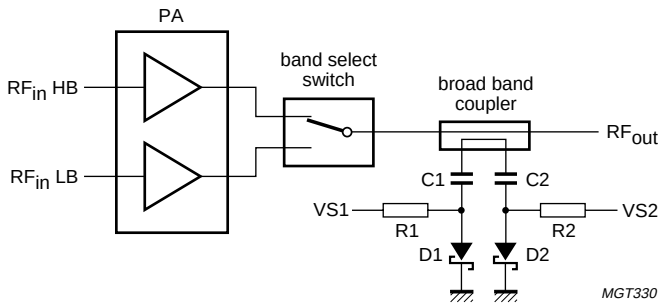


Fig.15 Example of PA mismatch protection circuit.

Table 3 Table of components (see Fig.15)

SYMBOL	COMPONENT	DESCRIPTION
D1, D2	detector diode	Philips 1PS79SB62
R1, R2	resistor	R = 1 kΩ (decoupling versions)
C1, C2	capacitor	C = 39 pF
–	band select switch	Motorola; Alpha Industries; M/A; COM GaAs MMIC; or discrete pin diode, e.g. Philips BAP51-03
–	broad band coupler	Murata LCD20 series; TDK HHM 20, 22 series

12.3 Detected voltage measurement

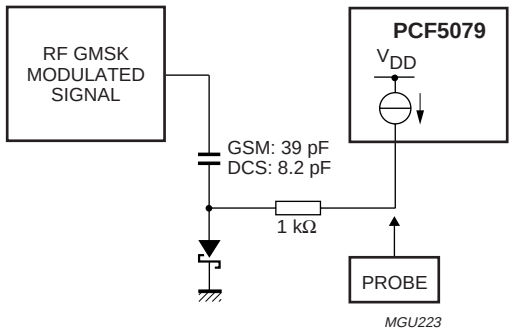
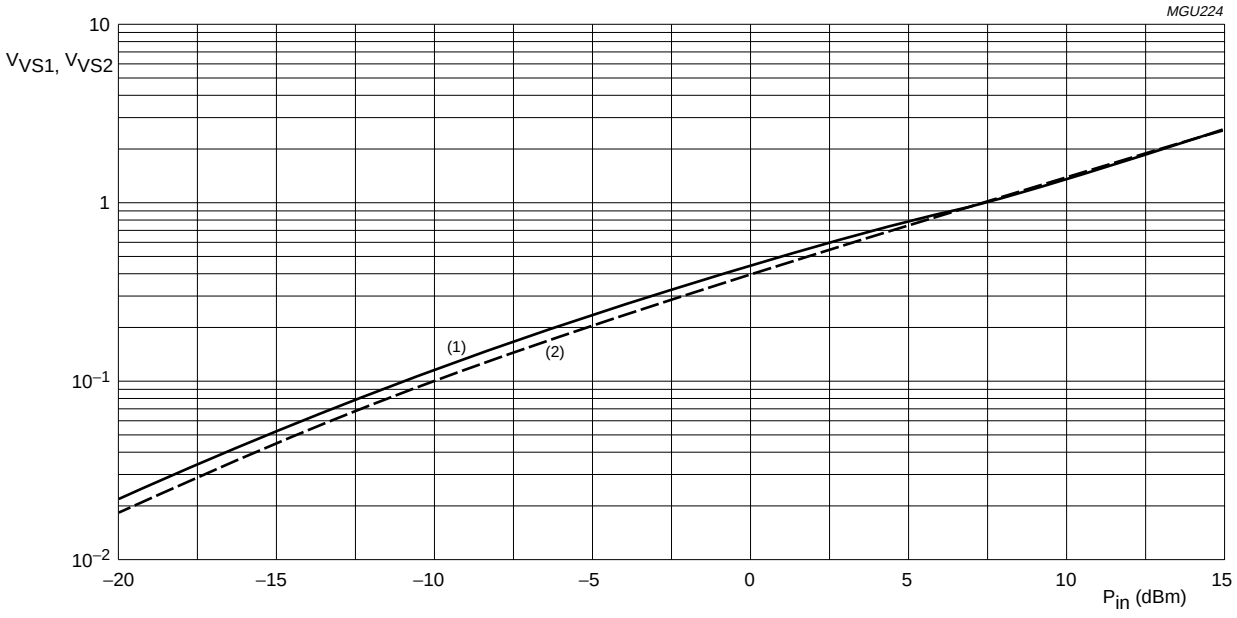


Fig.16 Set-up for measuring detected voltage for 900 MHz and 1800 MHz working.



(1) DCS.
(2) GSM.

Fig.17 Detected voltage as a function of incident power for 1PS79SB62 detector diodes.

12.4 Application examples

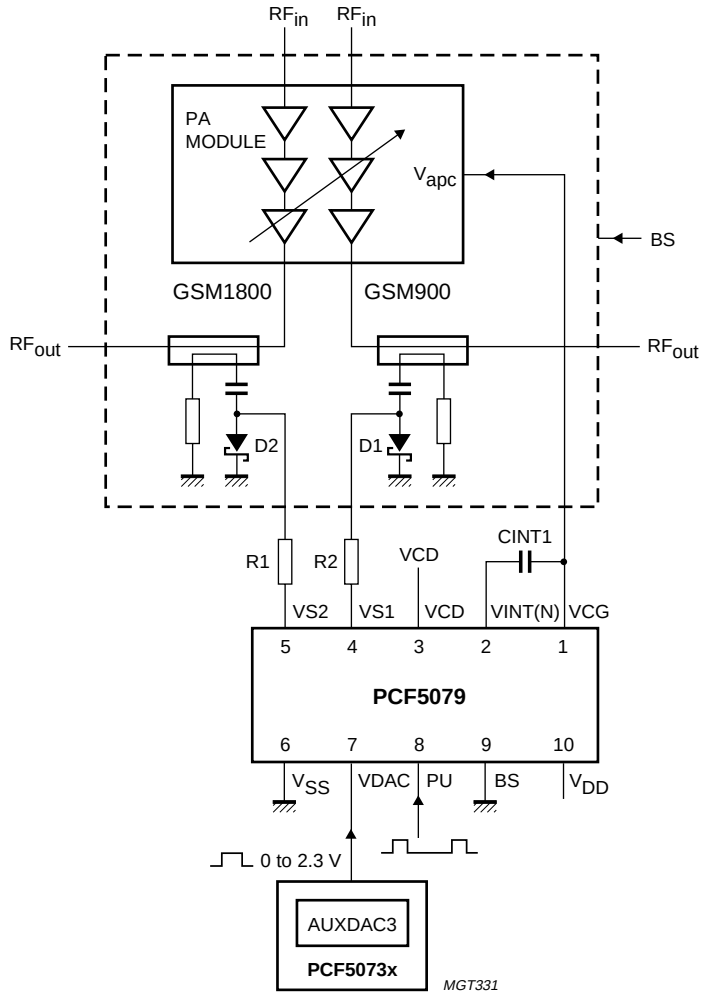


Fig.18 Application example of a dual-band PA module with single control input.

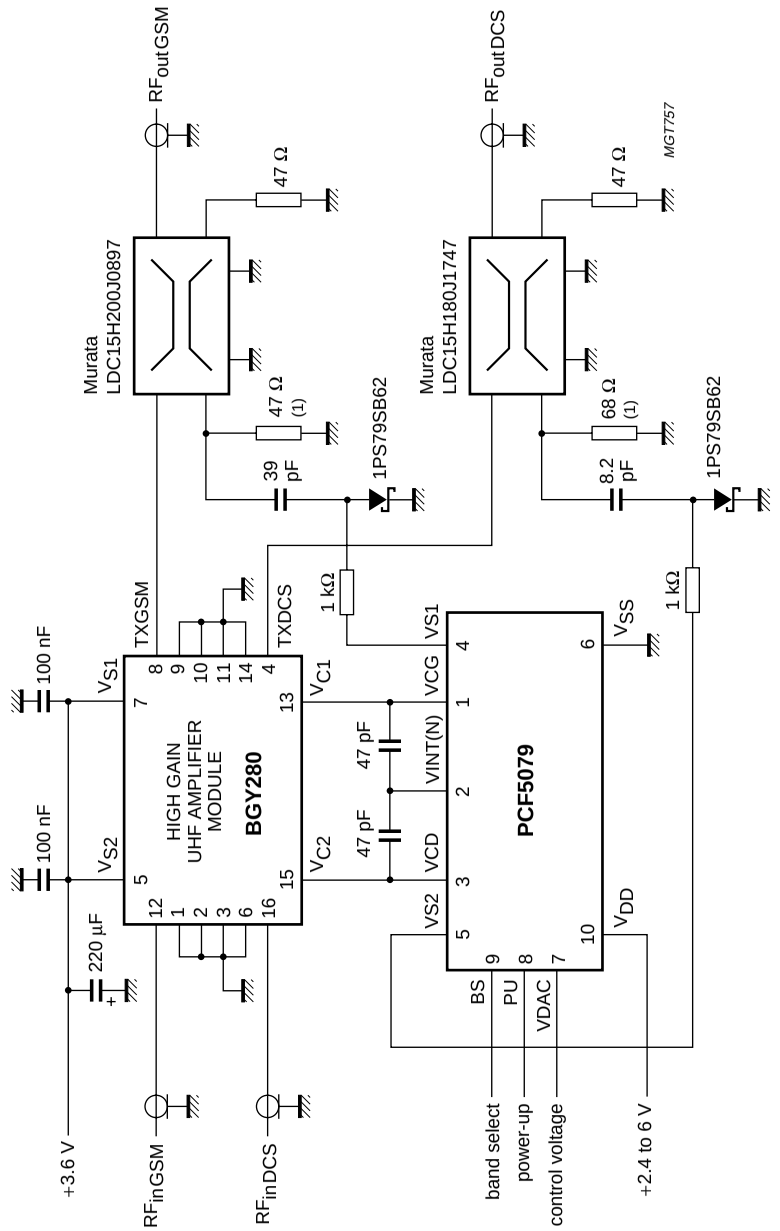
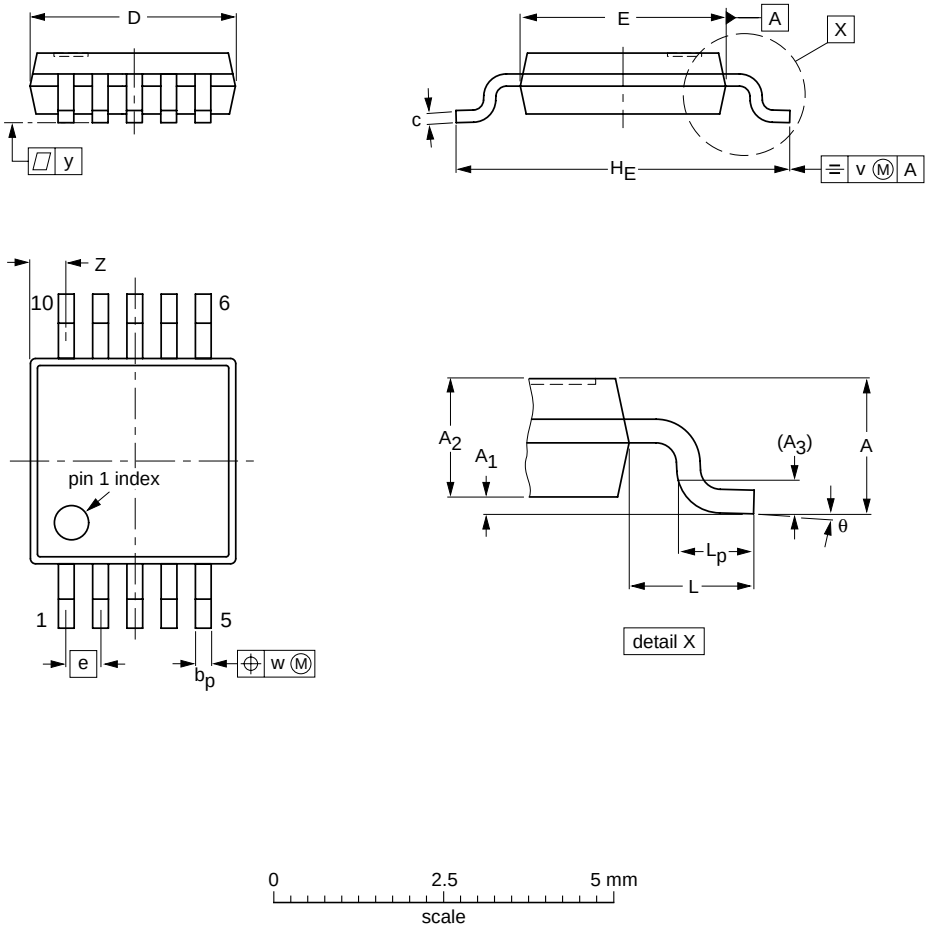


Fig.19 Application diagram.

(1) Precise value depends on the PCB design.

13 PACKAGE OUTLINES

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm **SOT552-1**



DIMENSIONS (mm are the original dimensions)

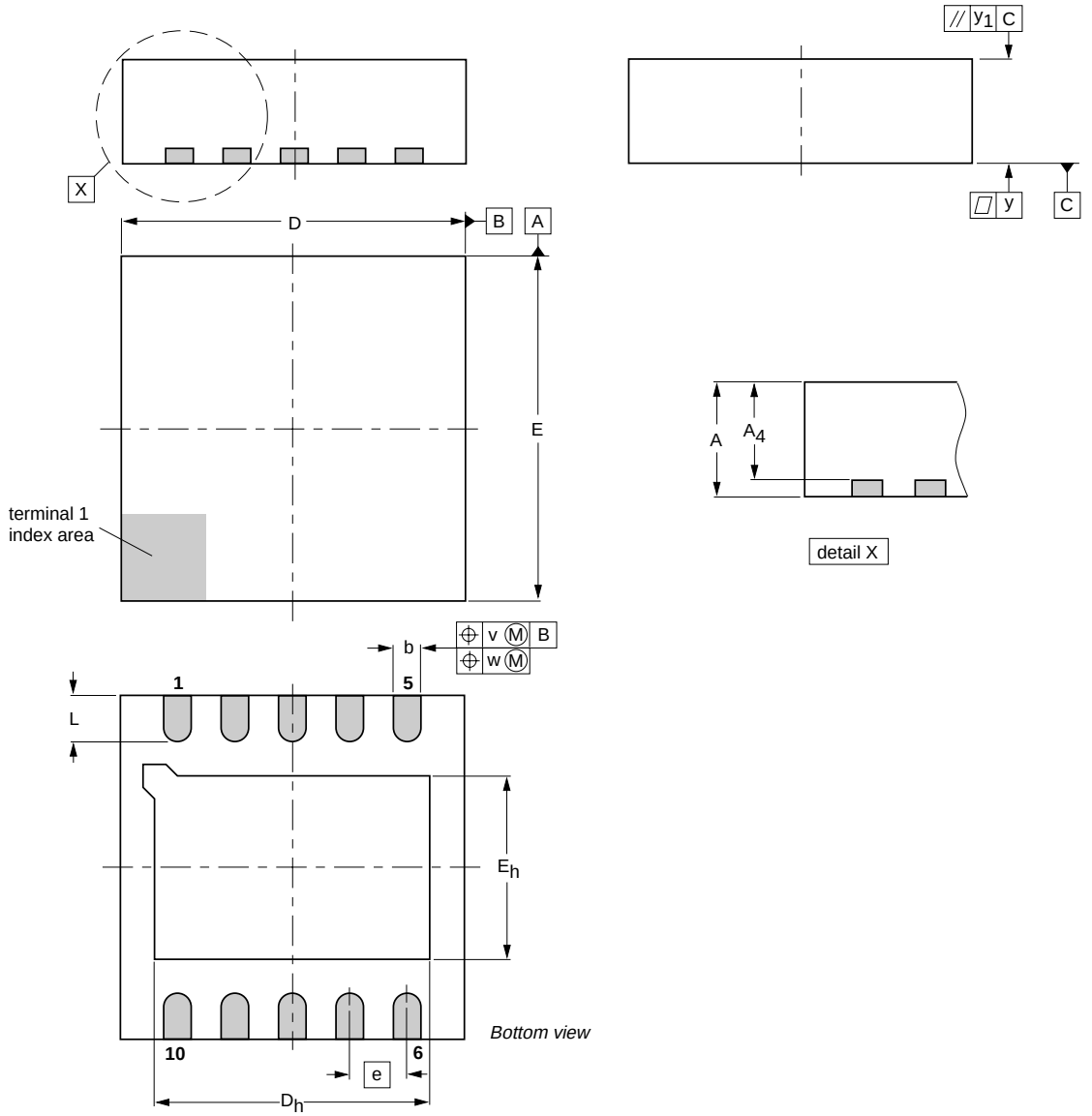
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.10 2.90	3.10 2.90	0.50	5.00 4.80	0.95	0.70 0.40	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

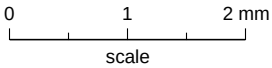
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT552-1						99-07-29

HVSON10: plastic, heatsink very thin small outline package; no leads; 10 terminals; body 3 x 3 x 0.90 mm **SOT650-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_4	b	D	D_h	E	E_h	e	L	v	w	y	y_1
mm	0.90	0.85 0.60	0.30 0.18	3.20 2.80	2.55 2.25	3.20 2.80	1.75 1.45	0.5	0.50 0.30	0.2	0.1	0.05	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT650-1		MO-229				01-01-22

14 SOLDERING (TSSOP10)

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 SOLDERING (HVSON10)

15.1 Soldering information

Information contained within this chapter is of a preliminary nature and may change without notice.

15.2 PCB design guidelines

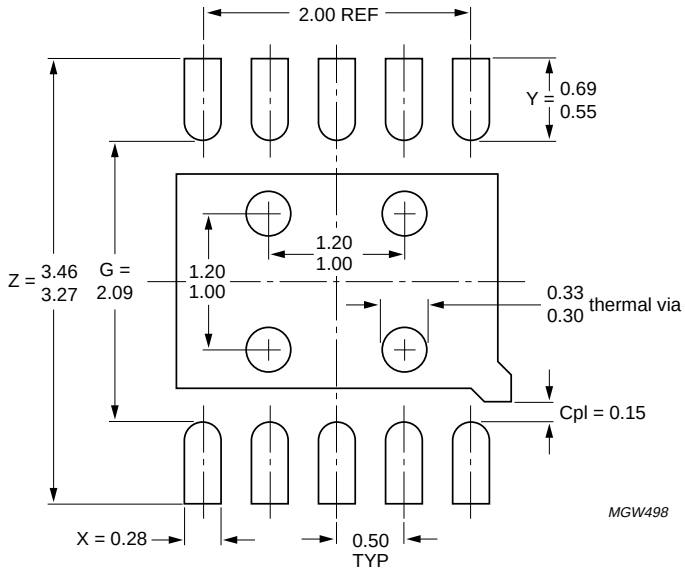
These guidelines are to help the user in developing the proper PCB design. For the surface mount process refer to *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

15.2.1 PERIMETER PAD DESIGN

Referring to Fig.20, dimensions Z and G are respectively the outside to outside and the inside to inside pad dimensions.

The dimensions X and Y indicate respectively the width and the length of the pad. Note that the calculated X dimension is the maximum value in order to avoid solder bridging between adjacent pads.The calculated Y dimension is the minimum value and therefore pad design should start with this value and the pad length at the outside be extended if more solder joint fillets are required.

The dimension 'Cpl' defines the minimum distance between the inner tip of the pad and the outer edge of the thermal pad. It is suggested that this dimension be fixed at 0.15 mm to avoid solder bridging issues between the thermal pad and the perimeter pads.



Dimensions in mm.

The solder mask opening dimension should be larger than the pad dimension by 125 to 150 μm.

Fig.20 HVSON10 PCB pattern.

15.2.2 THERMAL PAD AND VIA DESIGN

The size of the thermal pad should at least match the size of the exposed die-attach paddle. However, in some cases, the die-attach paddle size may need to be modified to avoid solder bridging between the thermal pad and the perimeter pads. In order to effectively transfer heat from the top metal layer to the inner or bottom layers of the PCB, thermal vias should be incorporated into the thermal pad design. The number of thermal vias will depend on the application and on the power dissipation and electrical requirements. It is recommended to incorporate an array of thermal vias at a pitch of 1.0 to 1.2 mm with the via diameter between 0.3 and 0.33 mm.

15.2.3 Stencil design for perimeter pads

For optimum paste release the area and aspect ratios of the stencil should be greater than 0.66 and 1.5 respectively.

$$\text{Area ratio} = \frac{\text{area of aperture opening}}{\text{aperture wall area}} = \frac{L \times W}{2T(L + W)}$$

$$\text{Aspect ratio} = \frac{\text{aperture width}}{\text{stencil thickness}} = \frac{W}{T}$$

where:

L = aperture length

W = aperture width

T = stencil thickness.

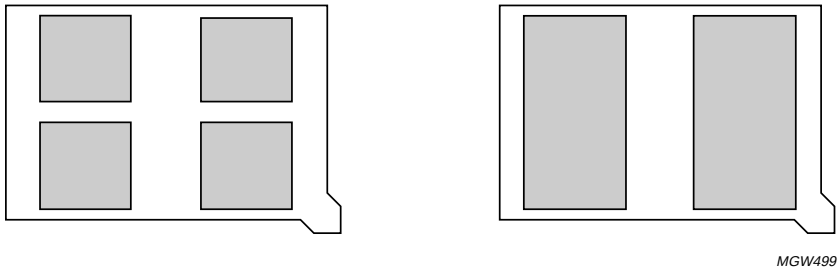
15.2.4 Stencil design for thermal pads

In order to remove the heat effectively from the package and to enhance electrical performance the die-attach paddle needs to be soldered to the PCB thermal pad, preferably with minimum voids.

It is therefore recommended that smaller, multiple openings in a stencil should be used instead of one large opening for printing solder paste in the thermal pad region. This results typically in 50% to 80% solder paste coverage. Two examples are shown in Fig.21.

15.2.5 Stencil thickness

A stencil thickness of 0.125 to 0.150 mm is recommended but this value needs to be optimized by the user to find the proper thickness according to application requirements.



a. Outline of 0.4 mm^2 2 $\times$ 2 array giving 44% solder paste coverage.

b. Outline of 1.2 mm^2 2 $\times$ 1 array giving 60% solder paste coverage.

Fig.21 Examples of thermal pad stencil design.

16 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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