T-52-13-90

GigaBit Logic

16G061

ADVANCE

Dual High Speed Pin Driver 1.5 GHz Operating Frequency

FEATURES

- DC to 1.5 GHz operation
- 600 ps propagation delay (ECL/GaAs)
- 150 ps output rise and fall times (ECL/GaAs)
- 200 ps output rise and fall times for up to 5Vp-p
- Selectable slow output edge rates for TTL/CMOS: 2ns rise and fall time at 5Volts peak to peak
- Programmable output voltages up to 5Vp-p over -2V to +5V range
- High impedance, three state output capability
- 100 mA output current drive capability
- High speed differential inputs, GaAs and ECL level compatible
- On chip VBBS (-1.2V) reference voltage
- Available in C-leaded or leadless chip carriers or in die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- ATE pin driver
- Switch Driver
- CRT preamplifier
- Laser driver
- Level comparator
- General purpose driver
- Differential Line Receiver
- Precision Pulse Generator

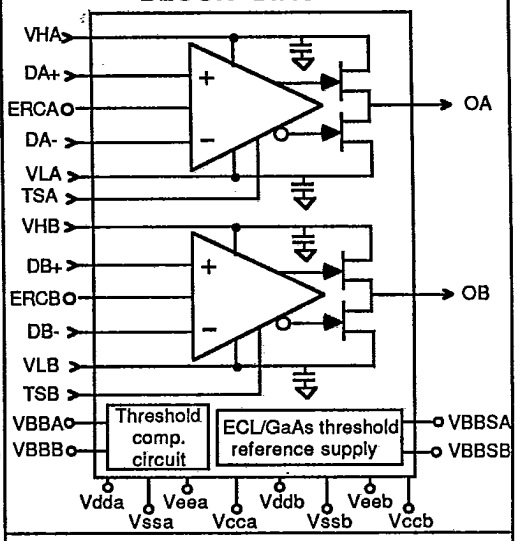
FUNCTIONAL DESCRIPTION

The 16G061 is a dual pin driver designed for use in very high speed GaAs/ECL as well as TTL/CMOS logic test systems. Each of the 16G061 driver is electrically independent and has separate power supplies. Under control of the differential inputs, the output is switched between the levels provided on the VH (V High) and VL (V Low) inputs. The differential inputs can be driven with ECL or GaAs levels. The 16G061 has an on-chip threshold voltage generator (VBBS). When VBBS is connected to the D- inputs, the D+ inputs of the 16G061 can be driven single-ended. The VHigh output level is adjustable from -1.1V to +5.0V and the VLow output level can be adjusted from -2.0V to +1.5V. The output amplitude extends to 5Vp-p. Controls are provided (TSA, TSB) to force the outputs into a high impedance, three state condition. An external series output resistor of typically 42Ω is recommended so that, in combination with the output MESFET on resistance (about 8Ω), the output impedance is 50Ω. External unity gain amplifiers such as the LM324 or higher current operational amplifiers such as the LM759 can be used to buffer the VHigh (VH) and VLow (VL) inputs when driven from DACs.

The 16G061 features an output Edge Rate Control (ERCA and ERCB) to vary the output rise and fall times. Rise and fall times are typically 150 ps for a 1V peak to peak output (GaAs/ECL) and 200 ps for a 5V peak to peak output when Edge Rate Control (ERC) is biased at VCC. This translates to a slew rate of 6.5V/ns for a 1V output and 25V/ns for a 5V output. Rise and fall times can be increased to 2ns for a 5V peak to peak output by connecting ERC to VEE. This translates to a slew rate of 2.5V/ns for a 5V output. System timing requirements are achieved through a specified 500ps driver propagation delay for ECL/GaAs levels, 600 ps delay for fast edge rate TTL/CMOS levels and 1.5 ns delay for slow edge rate TTL/CMOS levels.

The 16G061 is fabricated using GigaBit's high volume GaAs MESFET processing technology.

BLOCK DIAGRAM



Package Type	Speed (Min. 25°C) 1.5 GHz
C-leaded CC	16G061-2C
Leadless CC	16G061-2L
Die	16G061-2X

3081 C-10

T-52-13-90

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16G061

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ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDD	Output Driver Gnd Supply	VSS to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VCC	Supply Voltage	+0.5 V to +10.0V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	3
VOUT	Voltage Applied to Any Output	VL to VL+7.0 V	5
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTTC	VDD Internal Decoupling Cap. Return	-6.0 V to VDD	
VTT	Load Termination Supply	-6.0 V to VDD + 6.0 V	

Notes:
1. All voltages specified with VDD defined as Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.
5. Voltage applied through a 42Ω series resistor.

RECOMMENDED OPERATING CONDITIONS (Note 3)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
TC	Case Operating Temperature	0	25	85	°C	1
VDD	Supply Voltage		Gnd		V	
VCC	Supply Voltage	+3	VH + 2	7.5	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VH	High level set voltage	-1.1		5	V	
VL	Low level set voltage	-2.0		+1.5V	V	
VH - VL	Output voltage amplitude	0		5	V	2

Notes:
1. Tcase measured at case top. **User attention to device thermal management is recommended.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit.
2. For series terminations. For shunt termination: $Voh = VH \times \left(\frac{Rt}{Rt+Ron}\right)$; $Vol = VL \times \left(\frac{Rt}{Rt+Ron}\right)$; Rt: termination resistance.
3. Max. safe voltage applied to any output through a 42Ω series resistor is limited to VL to VL + 7.0V.

3082 C-11

T-52-13-90

GigaBit Logic

16G061

ADVANCE

DC CHARACTERISTICS (DC to 500 MHz - Note 1)

Tc = 0°C to 85°C, Vss = -3.5V to -3.3V, Vee = -5.5V to -5.1V, Vcc = 2.0V (ECL) or 7.0V (TTL), Vdd = Gnd

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Notes
Vih	Input voltage high	- 1.0		Vdd	V		
Vil	Input voltage low	Vss		- 1.6	V		
Vcm	Common mode Vin	-1.9	VBB	- 0.5	V		
Iin	Input current	- 100		100	µA	Vin = - 0.5V to - 1.9V	
Vbbs	Threshold Ref. voltage (ECL/GaAs)		- 1.2		V		3
Voh	Output voltage high	VH - .02	VH	VH	V	No DC load	
Vol	Output voltage low	VL	VL	VL + .02	V	No DC load	
Ioh	Output drive current	100			mA		2
Ron	Driver FET on rest.	7	8.5	10	Ω	At Voh, Vol	
Voffset	Input Offset Voltage		50		mV		
ICC	Supply Current		120		mA		
IEE	Supply Current		140		mA		
ISS	Supply Current		65		mA		
PdE	Power Dissipation		1.2		W	VCC = 2.0V (ECL)	4
PdT	Power Dissipation		1.8		W	VCC = 7.0V (TTL)	4
Izl	Three state output leakage		20		µA	@40°C	
Izls	Three state output leakage		40		µA	@40°C ; ERC = VEE	

Notes:
1. Test conditions unless otherwise indicated: -D input = -1.30V.
2. Test Conditions: VH - Vout ≥ 1V; VL - Vout ≤ - 1.0V.
3. Source impedance = 40Ω nominally. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
4. Measured at nominal supply voltages, 50% output duty cycle and both drivers powered.

AC CHARACTERISTICS (Note 1, 2)

Tc = 0°C to 85°C, Vss = -3.5V to -3.3V, Vee = -5.5V to -5.1V, Vcc = 2.0V (ECL) or 7.0V (TTL), Vdd = Gnd

		ECL/GaAs Output Levels			TTL Output Levels					
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Units	Test Cond.	Notes
F	Operating frequency	1000	1500		300	500		MHz		
td	Propagation delay		600			700		ps	ERC = VCC	
tds	Prop. delay, slow edge rates		1500			1500		ps	ERC = VEE	
td3	3-state delay		750			850		ps	ERC = VCC	
td3s	3-state delay, slow edge rates		1500			1500		ps	ERC = VEE	
Δtdm	Prop. Delay match; H-L, L-H		50	100		50	100	ps	ERC = VCC	
Δtdms	ΔProp.Delay match,slow mode		300			300		ps	ERC = VEE	
Δtd/Δdc	Δ Prop. delay with duty cycle			100			100	ps	ERC =VCC	
Δtd/ΔT	Prop. delay temp. coeff.		± 1.0			± 1.0		ps/°C	or VEE	
T	Output slew rate		7			25		V/ns	ERC = VCC	3
Tr,f	Output rise and fall times		150			200		ps	ERC = VCC	
Ts	Slow Output slew rate		0.7			2.5		V/ns	ERC = VEE	3
Tsr,sf	Slow Output rise and fall times		1500			2000		ps	ERC = VEE	
Tset	Settling time to 0.05 (Voh - Vol)		0.2	1.0		0.2	1.0	ns		
W	Output crosstalk		.05(Voh-Vol)			05(Voh-Vol)		V	@ 100MHz	

Notes:
1. VBB = -1.20V, Vih = -1.0V, Vil = -1.6V.
2. ECL Vp-p output = 1.0V; TTL Vp-p output = 5.0V.
3. Output rise and fall times are measured at 10% and 90% points.

3083 C-12

T-52-13-90

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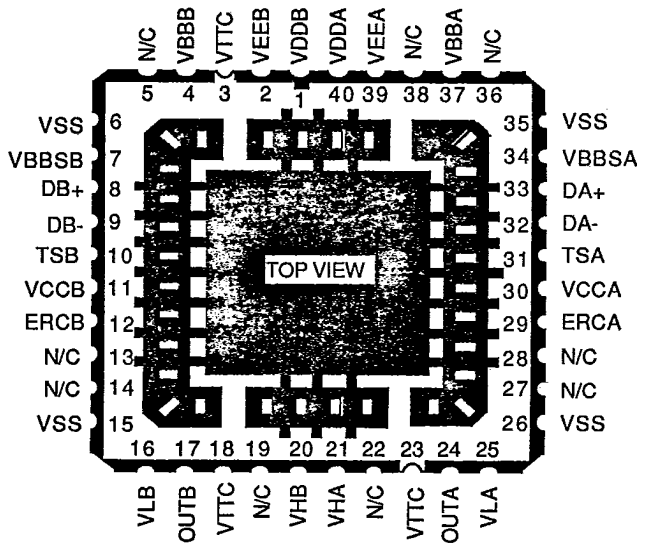
PIN DESCRIPTIONS

DA+, DA-	Differential data inputs A.
DB+, DB-	Differential data inputs B.
OA, OB	Output A, Output B.
VLA, VLB	Output Low level set voltages.
VHA, VHB	Output High level set voltages.
TSA, TSB	Three-State output controls. Output, OA or OB, is forced into a high impendance condition when TSA or TSB respectively is high.
ERCA, ERCB	Edge Rate Controls. Edge rates are slowed down when ERC is tied to VEE. Fast edge rates are obtained when ERC is tied to VCC.
VDDA, VDDB	Ground Pins (0V).
VSSA, VSSB	- 3.4V power supplies.
VEEA, VEEB	- 5.2V power supplies.
VCCA, VCCB	Positive power supplies. Nominally VH + 2V.
VTTCA, VTTCB	AC return pin for package internal decoupling capacitor tied to VH (VHigh) and VL (VLow) pins. VTTC is not brought onto the 16G061 substrate, and is typically tied to D.U.T. ground.
VBBA, VBBB	Reference input to the 10G061's input threshold compensation circuit. Connect the VBB supplied from ECL when driving from ECL. Otherwise connect to corresponding VBBS pin.
VBBSA, VBBSB	Picologic Threshold reference output voltage. Connect to VBB when driving form PicoLogic Δ VBBS/Δ Temp = 0.6mV/°C, Δ VBBS/ΔVSS = 0.2 mV/mV.

Pin Function Drawing
Package Types "L" and "C"



3084 C-13