T-51-09-08

HARRIS
SEMICONDUCTOR

AD7523
8–Bit Multiplying
D/A Converter

AD7523

GENERAL DESCRIPTION

The AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Harris' thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.
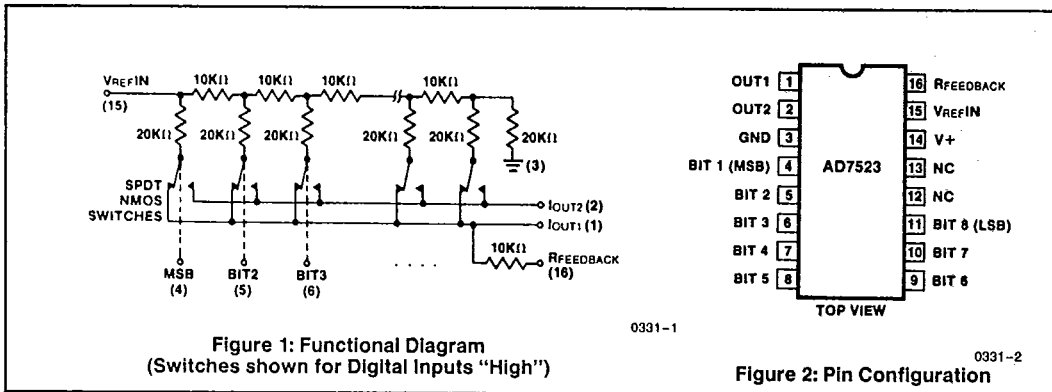
Low noise audio gain controls, motor speed controls, digitally controlled gain and attenuators are a few of the wide range of applications of the 7523.

FEATURES

- 8, 9 and 10 Bit Linearity
- Low Gain and Linearity Temperature Coefficients
- Full Temperature Range Operation
- Static Discharge Input Protection
- DTL/TTL/CMOS Compatible
- +5 to +15 Volts Supply Range
- Fast Settling Time: 150ns Max at 25°C
- Four Quadrant Multiplication

ORDERING INFORMATION

Nonlinearity	Part Number/Package	
	Plastic DIP	CERDIP
0.2% (8 Bit)	AD7523JN	
0.1% (9 Bit)	AD7523KN	AD7523TD/HR
0.05% (10 Bit)	AD7523LN	
TEMPERATURE RANGE	0°C to +70°C	−55°C to +125°C

Figure 1: Functional Diagram
(Switches shown for Digital Inputs "High")

0331–1

Figure 2: Pin Configuration

0331–2

NOTE: All typical values have been characterized but are not tested.

AD7523

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)   T-51-09-08

Supply Voltage (V⁺) .... +17V
V_{REF} .... ±25V
Digital Input Voltage Range .... V⁺ to GND
Output Voltage Compliance .... −100mV to V⁺
Power Dissipation:
Plastic Package —
  up to +70°C 670mW
  derate above +70°C by .... 8.3mW/°C

Ceramic Package —
  up to 75°C 450mW
  derate above 75°C by .... 6mW/°C
Operating Temperatures
  JN, KN, LN Versions .... 0°C to +70°C
  TD Version .... −55°C to +125°C
Storage Temperature .... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .... +300°C

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages higher than VDD and lower than GND to any terminal except $V_{REF} + R_{FEEDBACK}$.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V⁺ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise specified)

Parameter			Test Conditions	T_A +25°C	T_A Min−Max	Unit	Limit
DC ACCURACY (Note 1)							
Resolution				8	8	Bits	Min
Nonlinearity (Note 2)	J		−10V ≤ V_{REF} ≤ +10V V_{OUT1} = V_{OUT2} = 0V	±0.2	±0.2	% of FSR	Max
	K	T		±0.1	±0.1	% of FSR	Max
	L			±0.05	±0.05	% of FSR	Max
Monotonicity				Guaranteed			
Gain Error (Note 2)			All Digital Inputs high.	±1.5	±1.8	% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)			−10V V_{REF} +10V	±2		ppm of FSR/°C	Max
Gain Error Tempco (Notes 2 and 3)				±10		ppm of FSR/°C	Max
Output Leakage Current (either output)			V_{OUT1} = V_{OUT2} = 0	±50	±200	nA	Max
AC ACCURACY							
Power Supply Rejection (Note 2)			V⁺ = 14.0 to 15.0V	±0.02	±0.03	% of FSR/% ΔV⁺	Max
Output Current Settling Time (Note 3)			To 0.2% of FSR, R_L = 100Ω	150	200	ns	Max
Feedthrough Error (Note 3)			V_{REF} = 20V pp, 200kHz sine wave. All digital inputs low.	±½	±1	LSB	Max
REFERENCE INPUT							
Input Resistance (Pin 15)			All digital inputs high. I_{OUT1} at ground.	5K		Ω	Min
				20K			Max
Temperature Coefficient (Note 3)				−500		ppm/°C	Max
ANALOG OUTPUT							
Output Capacitance (Note 3)	C_{OUT1}		All digital inputs high	100		pF	Max
	C_{OUT2}			30		pF	Max
	C_{OUT1}		All digital inputs low	30		pF	Max
	C_{OUT2}			100		pF	Max

NOTE: All typical values have been characterized but are not tested.

AD7523

AD7523

T-51-09-08

ELECTRICAL CHARACTERISTICS

(V $^+$ = +15V, V$_{REF}$ = +10V, V$_{OUT1}$ = V$_{OUT2}$ = 0V unless otherwise specified) (Continued)

Parameter	Test Conditions	T$_A$ +25°C	T$_A$ Min–Max	Unit	Limit
DIGITAL INPUTS					
Low State Threshold		0.8		V	Max
High State Threshold		2.4		V	· Min
Input Current (Low or high)	V$_{IN}$ = 0V or +15V	±1		μA	Max
Input Coding	See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)		4		pF	Max
POWER REQUIREMENTS					
Power Supply Voltage Range	Accuracy is tested and guaranteed at V $^+$ = +15V, only.	+5 to +16		V	
I $^+$ (Excluding Ladder Network)	All digital inputs High or Low	2	2.5	mA	Max

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, R$_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

DETAILED DESCRIPTION

The AD7523 is a monolithic multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS SPDT switches steer the ladder leg currents between I$_{OUT1}$ and I$_{OUT2}$ buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 4). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.
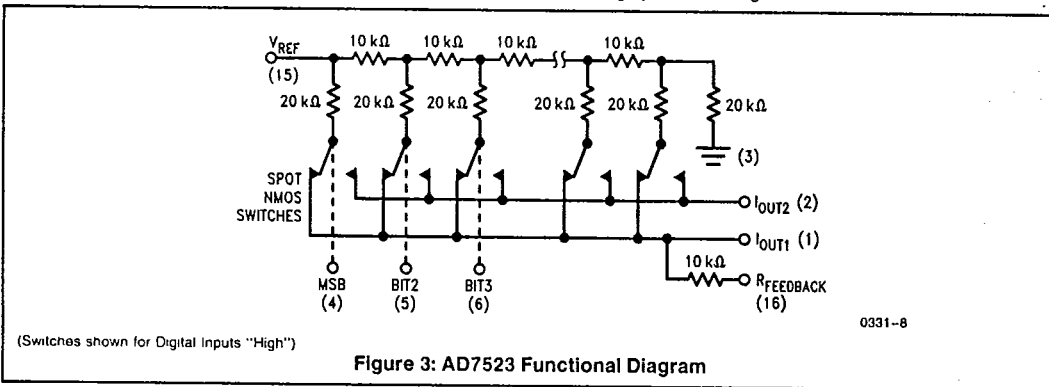

(Switches shown for Digital Inputs "High")

0331–8

Figure 3: AD7523 Functional Diagram

NOTE All typical values have been characterized but are not tested.
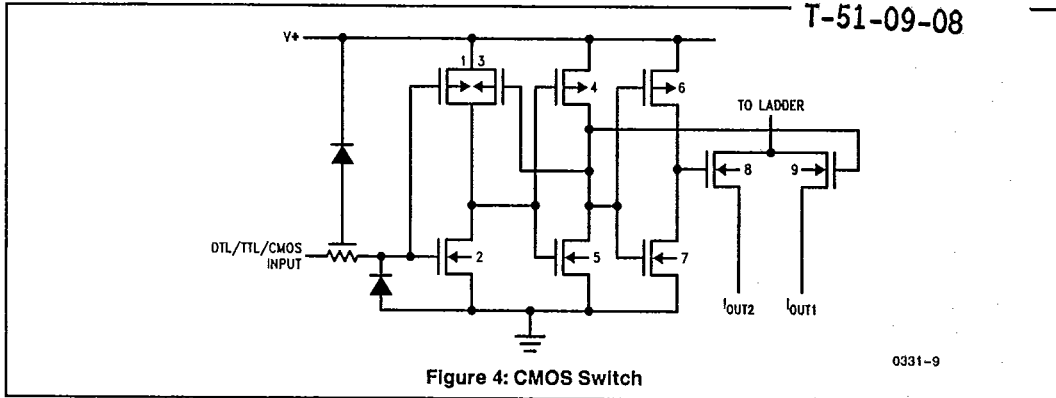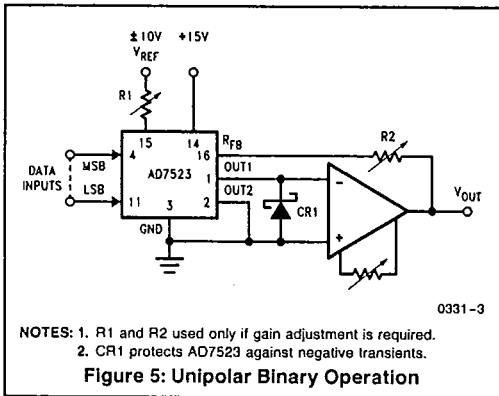
AD7523

T-51-09-08

Figure 4: CMOS Switch

0331-9

APPLICATIONS

UNIPOLAR OPERATION

NOTES: 1. R1 and R2 used only if gain adjustment is required.
2. CR1 protects AD7523 against negative transients.

Figure 5: Unipolar Binary Operation

0331-3

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7523 in unipolar mode is shown in Figure 5. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

ZERO OFFSET ADJUSTMENT
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ± 1 mV (max) at V_{OUT}.

GAIN ADJUSTMENT
1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}(1 - \frac{1}{2}^8)$ reading.
3. To increase V_{OUT}, connect a series resistor, R2, (0 to 250Ω) in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, R1, (0 to 250Ω) between the reference voltage and the V_{REF} terminal.

Table 1. Unipolar Binary Code Table

Digital Input MSB LSB	Analog Output
11111111	$-V_{REF}\left(\dfrac{255}{256}\right)$
10000001	$-V_{REF}\left(\dfrac{129}{256}\right)$
10000000	$-V_{REF}\left(\dfrac{128}{256}\right) = -\dfrac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\dfrac{127}{256}\right)$
00000001	$-V_{REF}\left(\dfrac{1}{256}\right)$
00000000	$-V_{REF}\left(\dfrac{0}{256}\right) = 0$

NOTE: 1 LSB = $(2^{-8})\ (V_{REF}) = \left(\dfrac{1}{256}\right)\ (V_{REF})$

6

NOTE: All typical values have been characterized but are not tested.

BIPOLAR OPERATION

T-51-09-08

NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

**Figure 6: Bipolar Operation
(4-Quadrant Multiplication)**

0331-4
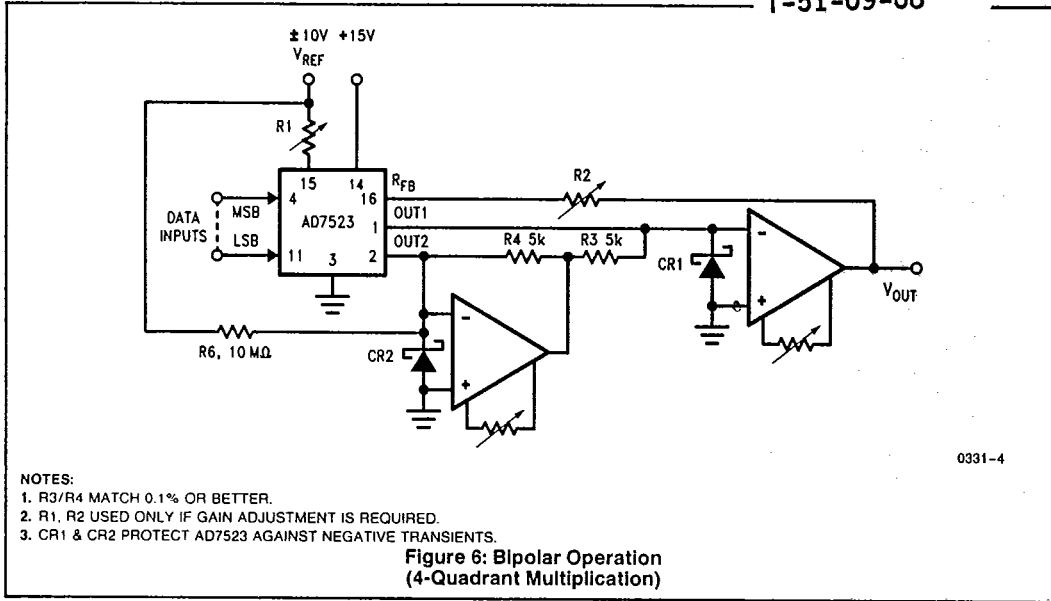
Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7523 in the bipolar mode is given in Figure 6. Using offset binary digital input codes and positive and negative reference voltage values, Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

Table 2. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Analog Output
11111111	$-V_{REF} \left(\dfrac{127}{128} \right)$
10000001	$-V_{REF} \left(\dfrac{1}{128} \right)$
10000000	0
01111111	$+V_{REF} \left(\dfrac{1}{128} \right)$
00000001	$+V_{REF} \left(\dfrac{127}{128} \right)$
00000000	$+V_{REF} \left(\dfrac{128}{128} \right)$

NOTE: $1\,LSB = (2^{-7})\,(V_{REF}) = \left(\dfrac{1}{128} \right)\,(V_{REF})$

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 MΩ), from V_{REF} to I_{OUT2} (Figure 6).

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2}. amplifier offset adjust trimpot for 0V ±1 mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V⁺.
2. Monitor V_{OUT} for a $-V_{REF}\,(1 - \frac{1}{2}^7)$ volts reading.
3. To increase V_{OUT}, connect a series resistor, R2, of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor, R1, of up to 250Ω between the reference voltage and the V_{REF} terminal.

NOTE. All typical values have been characterized but are not tested.

AD7523

POWER DAC DESIGN USING AD7523   T-51-09-08

$$V_{OUT} = -V_{IN}/D$$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \dots \frac{BIT8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256} \right)$$

0331-6
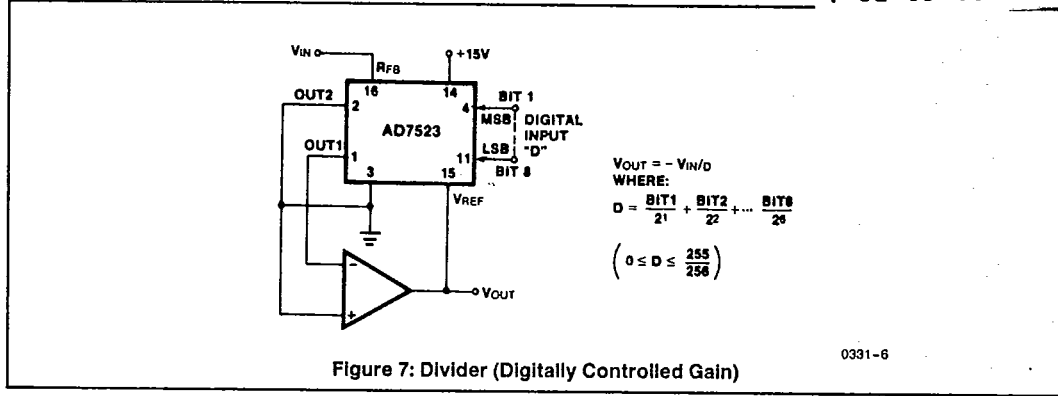
Figure 7: Divider (Digitally Controlled Gain)

$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right) \right]$$

$$\text{Where } D = \frac{Bit\ 1}{2^1} + \frac{Bit\ 2}{2^2} + \dots \frac{Bit\ 8}{2^8}$$

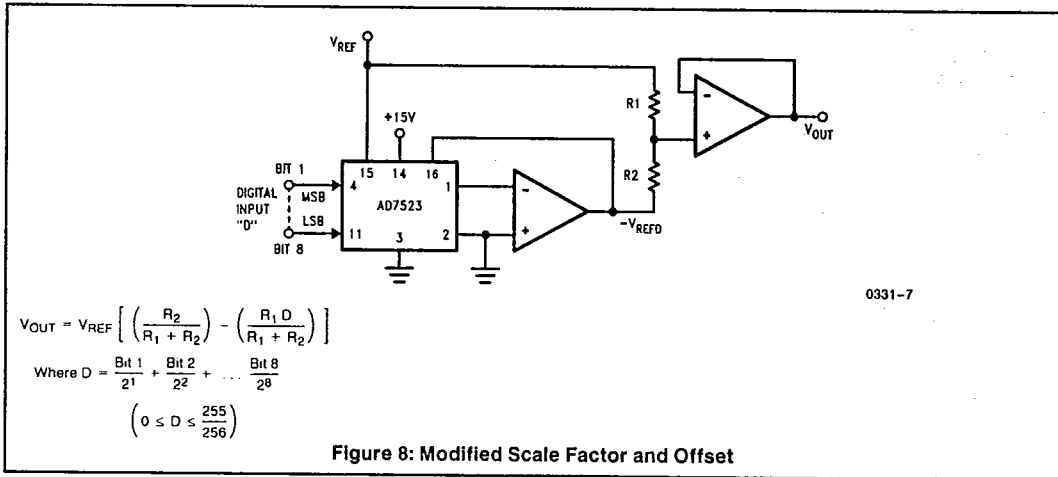$$\left(0 \le D \le \frac{255}{256} \right)$$

0331-7

Figure 8: Modified Scale Factor and Offset

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g. 2^{-n} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within specified error band around its final value (e.g. ½ LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

A002 "Principles of Data Acquisition and Conversion"

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A042 "Interpretation of Data Conversion Accuracy Specifications"