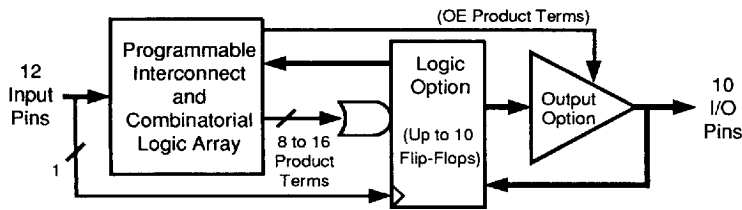


Features

- High Performance Programmable Logic Device
 - 7.5 ns Max Propagation Delay
 - Up to 166 MHz Operation
 - 5 V ± 10% Operation
- Fully Compatible with Standard 22V10
 - Identical Functionality/Fuse-Map
- CMOS and TTL Compatible Inputs and Outputs
 - 10 µA Leakage Maximum
- Reprogrammable - Tested 100% for Programmability
- High Reliability
 - Proven UV Erasable CMOS Technology
 - 2000 V ESD Protection
- Full Military, Commercial and Industrial Temperature Ranges
- Dual-In-Line and Surface Mount Packages with Standard Pinouts

**High Speed
UV Erasable
Programmable
Logic Device**

Logic Diagram



Description

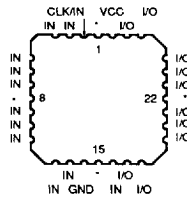
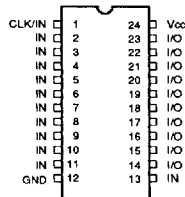
The AT22V10B is an ultra-high performance CMOS Erasable Programmable Logic Device (EPLD). Speeds down to 7.5 ns and operation up to 166 MHz are offered. All pins offer a low ± 10 µA leakage.

The AT22V10B logic functionality is fully compatible with the standard 22V10. The 12 dedicated inputs and ten configurable I/O pins allow implementation of logic requiring up to 22 input signals. The AT22V10B also provides individual output enable product terms for each of the ten I/Os.

Continued on next page.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply



1074177 0005441 34T

Description (Continued)

The AT22V10B incorporates a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

The AT22V10B includes two additional product terms to provide synchronous preset and asynchronous reset. These terms

are common to all ten registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

Absolute Maximum Ratings*

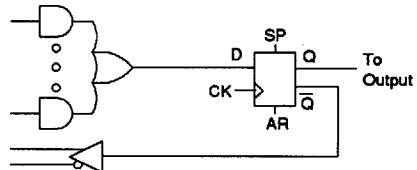
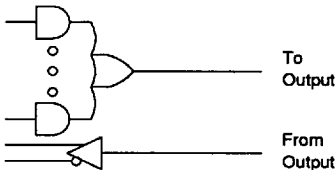
Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0 V to +7.0 V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0 V to +14.0 V ⁽¹⁾
Programming Voltage with Respect to Ground.....	-2.0 V to +14.0 V ⁽¹⁾
Integrated UV Erase Dose.....	7258 W-sec/cm ²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

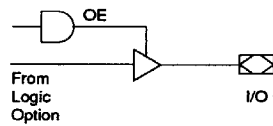
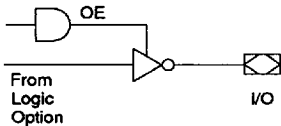
Note:

1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}+0.75$ V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Logic Options



Output Options



D.C. and A.C. Operating Conditions

	Commercial AT22V10B -7	Commercial AT22V10B -10, -12	Industrial AT22V10B -10, -12	Military AT22V10B -10, -12
Operating Temperature (Case)	0°C - 70°C	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V _{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	24-Pin DIP	1	5	8	13	I/O's	V _{CC} (24)
	28-Pin JLC	2	6	10	16	I/O's	V _{CC} (28)
"EPLD"	X ⁽¹⁾	X	X	X	X	I/O	5V
Program	V _{PP}	X / V _H ⁽²⁾	X	V _{PP}	DIN	6V	
PGM Verify	V _{PP}	X/V _H	X	V _{IL}	DOUT	6V	
PGM Inhibit	V _{PP}	X/V _H	X	V _{IH}	High Z	6V	
Preload	X	X	V _H	X	DIN	5V	

Notes: 1. X can be V_{IL} or V_{IH}.

2. V_H = 11.0 V to 14.0 V

7

D.C. Characteristics

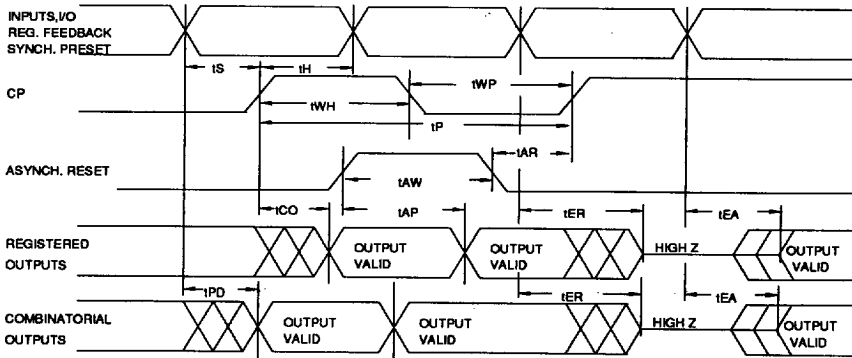
Symbol	Parameter	Condition	Min	Max	Units	
I _{LI}	Input Load Current	V _{IN} = -0.1 V to V _{CC} +1 V		10	μA	
I _{LO}	Output Leakage Current	V _{OUT} = -0.1 V to V _{CC} +0.1 V		10	μA	
I _{CC}	Power Supply Current	V _{CC} = MAX, V _{IN} = GND, Outputs Open	Com.	140	mA	
			Ind., Mil.	160	mA	
I _{OS} ⁽¹⁾	Output Short Circuit Current	V _{OUT} = 0.5 V	-30	-120	mA	
V _{IL}	Input Low Voltage		-0.6	0.8	V	
V _{IH}	Input High Voltage		2.0	V _{CC} +0.75	V	
V _{OL}	Output Low Voltage	V _{IN} = V _{IH} or V _{IL} , V _{CC} = MIN	I _{OL} = 16 mA	Com., Ind.	0.5	V
			I _{OL} = 12 mA	Mil.	0.5	V
			I _{OL} = 24 mA	Com.	0.8	V
V _{OH}	Output High Voltage	V _{IN} = V _{IH} or V _{IL} , V _{CC} = MIN	I _{OH} = -4.0 mA	2.4	V	

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.



1074177 0005443 112

A.C. Waveforms ⁽¹⁾



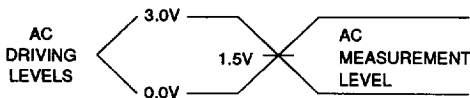
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	AT22V10B-7			AT22V10B-10			AT22V10B-12			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PD}	Input or Feedback to Non-Registered Output		5	7.5		6	10		7	12	ns
t _{EA}	Input to Output Enable		5	7.5		6	10		7	12	ns
t _{ER}	Input to Output Disable		5	7.5		6	10		7	12	ns
t _{CF} ⁽¹⁾	Clock to Feedback	0	1	2	0	1	2	0	1.5	2	ns
t _{CO}	Clock to Output	0	3.5	6.0	0	4	7	0	5	7.5	ns
t _S	Input or Feedback Setup Time	4	2.5		5	3		6	5		ns
t _H	Hold Time	0			0			0			ns
t _P	Clock Period	6			7			8			ns
t _{WL} ⁽¹⁾	Clock Width Low	3			3.5			4			ns
t _{WH}	Clock Width High	3			3.5			4			ns
F _{MAX}	External Feedback 1/(t _S +t _{CO})			100			83			74	MHz
	Internal Feedback 1/(t _S + t _{CF})			166			142			125	MHz
	No Feedback 1/(t _P)			166			142			125	MHz
t _{AW}	Asynchronous Reset Width	6	3		7	4		8	5		ns
t _{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	7.5	4		8	5		8.5	5		ns
t _{AP}	Asynchronous Reset to Registered Output Reset		7	13		8	14		9	15	ns

Note: 1. This parameter is only sampled and is not 100% tested.

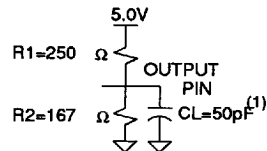
Input Test Waveforms and Measurement Levels



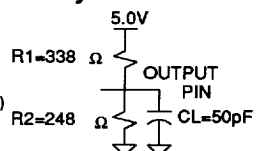
t_R, t_F < 2 ns (10% to 90%)

Output Test Loads:

Commercial

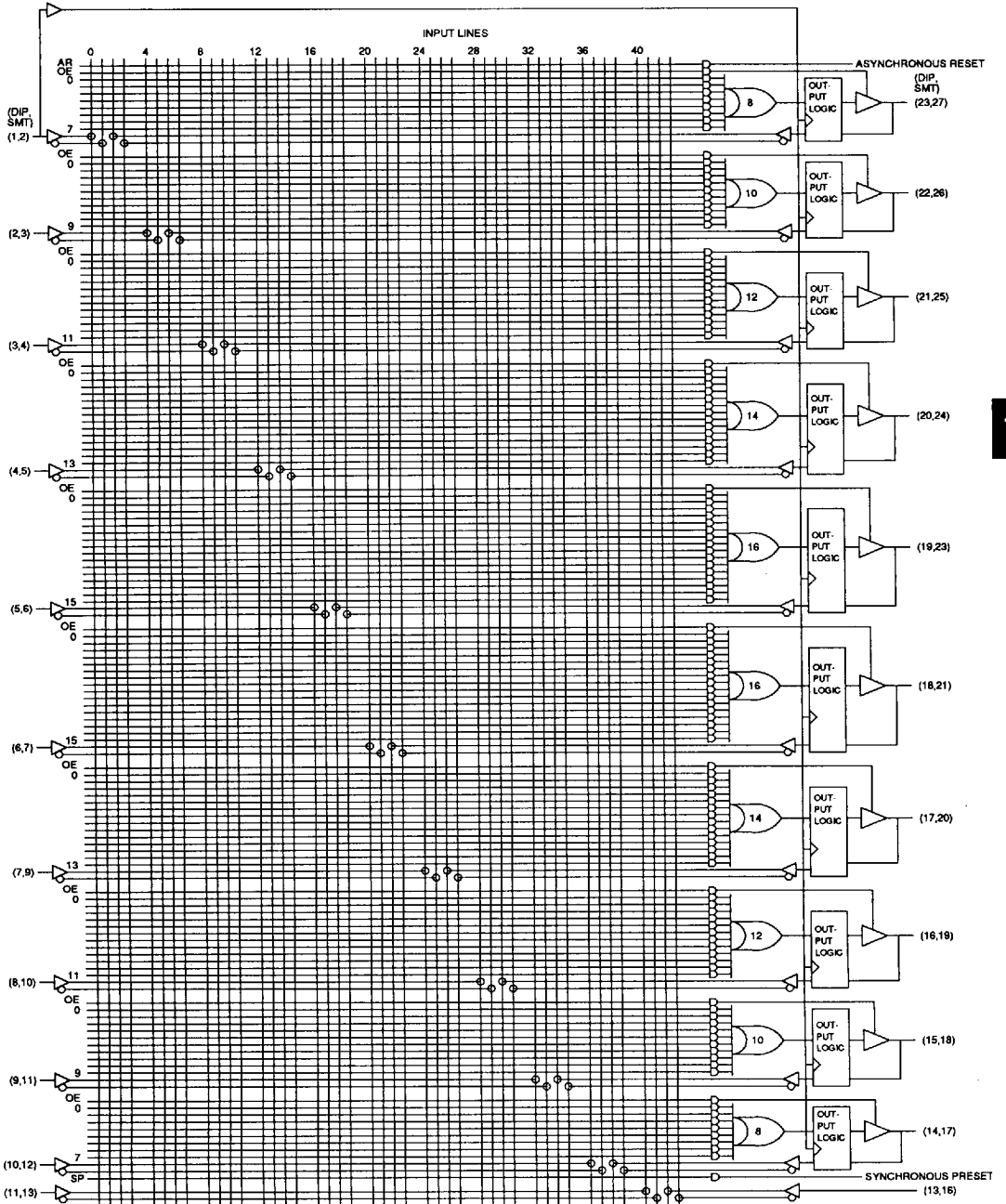


Military



Note: 1. CL = 30 pF for AT22V10B-7

Functional Logic Diagram AT22V10B



7

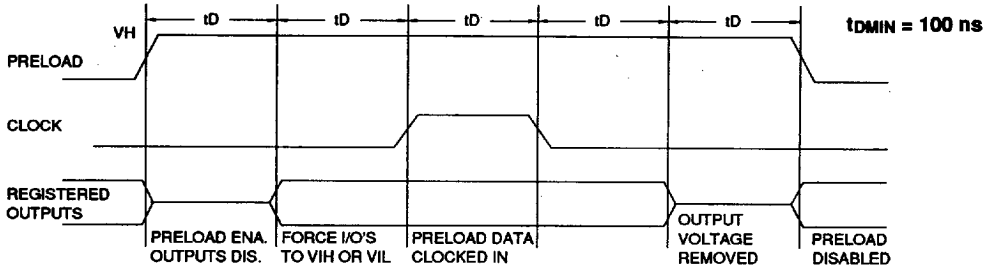


1074177 0005445 T95

Preload of Registered Outputs

The registers in the AT22V10B are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (CO) setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low

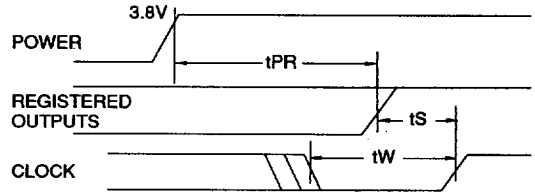


Power Up Reset

The registers in the AT22V10B are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

- 1) The V_{CC} rise must be monotonic,
- 2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
- 3) The clock must remain stable during t_{PR} .



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) ⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	$V_{IN} = 0$ V
C_{OUT}	6	8	pF	$V_{OUT} = 0$ V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

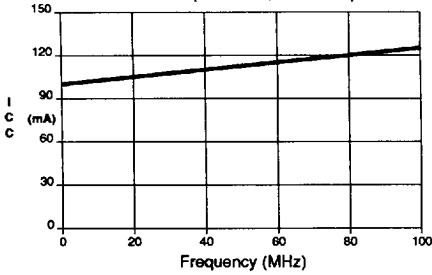
Erasure Characteristics

The entire fuse array of an AT22V10B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu\text{W}/\text{cm}^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be

calculated from the minimum integrated erasure dose of 15 $\text{W}\cdot\text{sec}/\text{cm}^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPD which will be subjected to continuous fluorescent indoor lighting or sunlight.

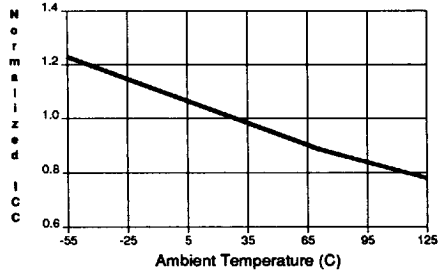
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10B (TA = 25C, VCC = 5V)

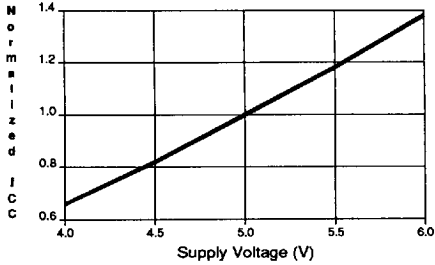


NORMALIZED ICC vs. AMBIENT TEMP.

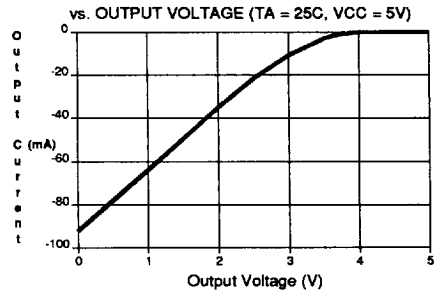
f = 50 MHz



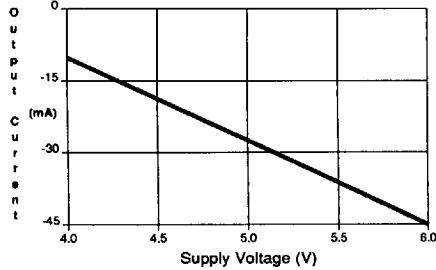
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



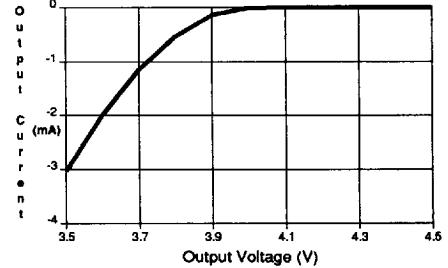
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



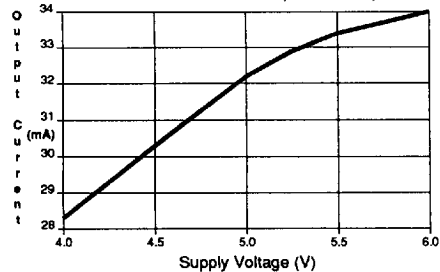
OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE (VOH = 2.4V)



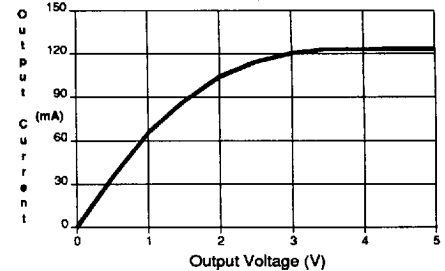
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE (VOL = 0.5V)

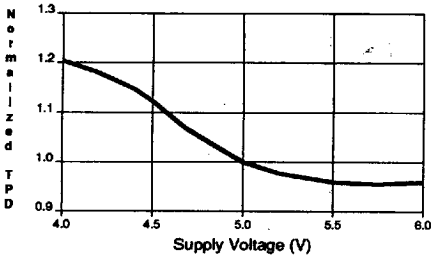


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)

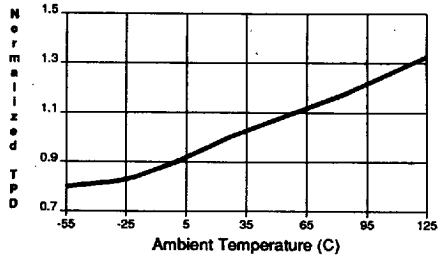


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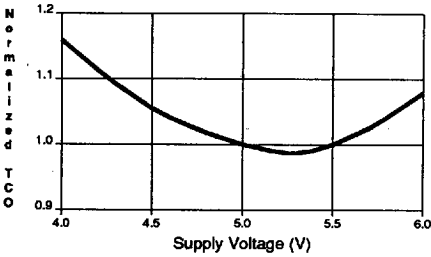
**NORMALIZED TPD
vs. SUPPLY VOLTAGE**



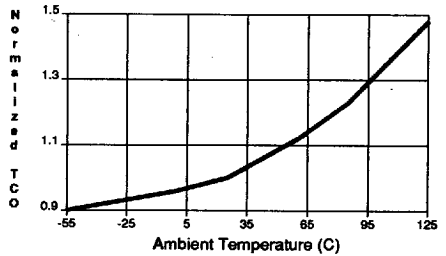
**NORMALIZED TPD
vs. TEMPERATURE**



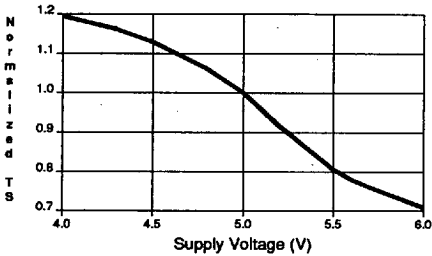
**NORMALIZED TCO
vs. SUPPLY VOLTAGE**



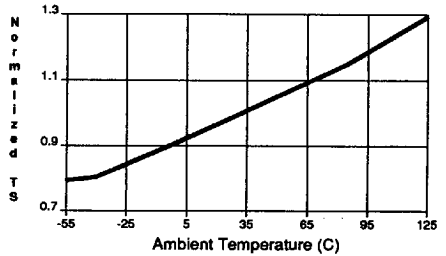
**NORMALIZED TCO
vs. TEMPERATURE**



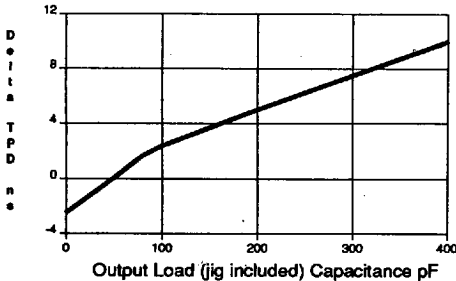
**NORMALIZED TS
vs. SUPPLY VOLTAGE**



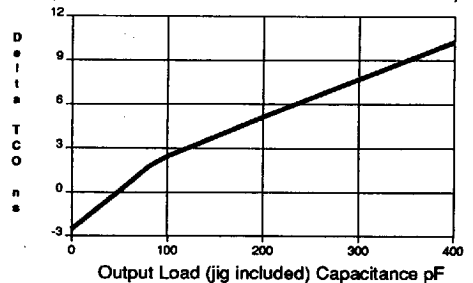
**NORMALIZED TS
vs. TEMPERATURE**



**DELTA TPD vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)**



**DELTA TCO vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)**



Ordering Information

tpd (ns)	ts (ns)	tco (ns)	Ordering Code	Package	Operation Range
7.5	4	6	AT22V10B-7DC AT22V10B-7GC AT22V10B-7JC AT22V10B-7KC AT22V10B-7LC AT22V10B-7NC AT22V10B-7PC AT22V10B-7SC	24DW3 24D3 28J 28KW 28LW 28L 24P3 24S	Commercial (0°C to 70°C)
10	5	7	AT22V10B-10DC AT22V10B-10GC AT22V10B-10JC AT22V10B-10KC AT22V10B-10LC AT22V10B-10NC AT22V10B-10PC AT22V10B-10SC	24DW3 24D3 28J 28KW 28LW 28L 24P3 24S	Commercial (0°C to 70°C)
			AT22V10B-10DI AT22V10B-10GI AT22V10B-10JI AT22V10B-10KI AT22V10B-10LI AT22V10B-10NI AT22V10B-10PI AT22V10B-10SI	24DW3 24D3 28J 28KW 28LW 28L 24P3 24S	Industrial (-40°C to 85°C)
			AT22V10B-10DM AT22V10B-10GM AT22V10B-10KM AT22V10B-10LM AT22V10B-10NM	24DW3 24D3 28KW 28LW 28L	Military (-55°C to 125°C)
			AT22V10B-10DM/883 AT22V10B-10GM/883 AT22V10B-10KM/883 AT22V10B-10LM/883 AT22V10B-10NM/883	24DW3 24D3 28KW 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
12	6	7.5	AT22V10B-12DC AT22V10B-12GC AT22V10B-12JC AT22V10B-12KC AT22V10B-12LC AT22V10B-12NC AT22V10B-12PC AT22V10B-12SC	24DW3 24D3 28J 28KW 28LW 28L 24P3 24S	Commercial (0°C to 70°C)
			AT22V10B-12DI AT22V10B-12GI AT22V10B-12JI AT22V10B-12KI AT22V10B-12LI AT22V10B-12NI AT22V10B-12PI AT22V10B-12SI	24DW3 24D3 28J 28KW 28LW 28L 24P3 24S	Industrial (-40°C to 85°C)

7



1074177 0005449 630



Ordering Information

t _{PD} (ns)	t _s (ns)	t _{CO} (ns)	Ordering Code	Package	Operation Range
12	6	7.5	AT22V10B-12DM AT22V10B-12GM AT22V10B-12KM AT22V10B-12LM AT22V10B-12NM	24DW3 24D3 28KW 28LW 28L	Military (-55°C to 125°C)
			AT22V10B-12DM/883 AT22V10B-12GM/883 AT22V10B-12KM/883 AT22V10B-12LM/883 AT22V10B-12NM/883	24DW3 24D3 28KW 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

7-44

AT22V10B

■ 1074177 0005450 352 ■