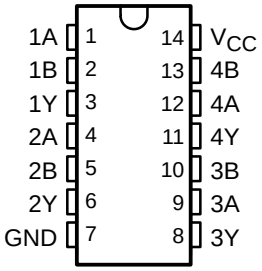
CD74HC08-Q1
QUADRUPLE 2-INPUT POSITIVE-AND GATES

- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Buffered Inputs**
- **Typical Propagation Delay 7 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Extended Temperature Performance of –40°C to 125°C**

† Contact factory for details. Q100 qualification data available on request.

- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction, Compared to LSTTL Logic ICs**
- **2-V to 6-V V_{CC} Operation**
- **High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC} at V_{CC} = 5 V**
- **CMOS Input Compatibility, $I_I \leq 1\ \mu A$ at V_{OL}, V_{OH}**

M PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC08 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. The device can drive 10 LSTTL loads.

ORDERING INFORMATION

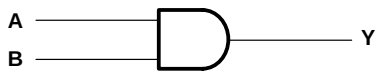
T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC08QM96Q1	HC08Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < –0.5 V or V_I > V_{CC} + 0.5 V) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < –0.5 V or V_O > V_{CC} + 0.5 V) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O (V_O > –0.5 or V_O < V_{CC} + 0.5 V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 180°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	T_A = 25°C			CD74HC08-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	–0.02	2 V	1.9			1.9		V
			–0.02	4.5 V	4.4			4.4		
			–0.02	6 V	5.9			5.9		
		TTL loads	–4	4.5 V	3.98			3.7		
			–5.2	6 V	5.48			5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V			0.1		0.1	V
			0.02	4.5 V			0.1		0.1	
			0.02	6 V			0.1		0.1	
		TTL loads	4	4.5 V			0.26		0.4	
			5.2	6 V			0.26		0.4	
I_I	$V_I = V_{CC}$ or GND			6 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V			2		40	µA
C_i							10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

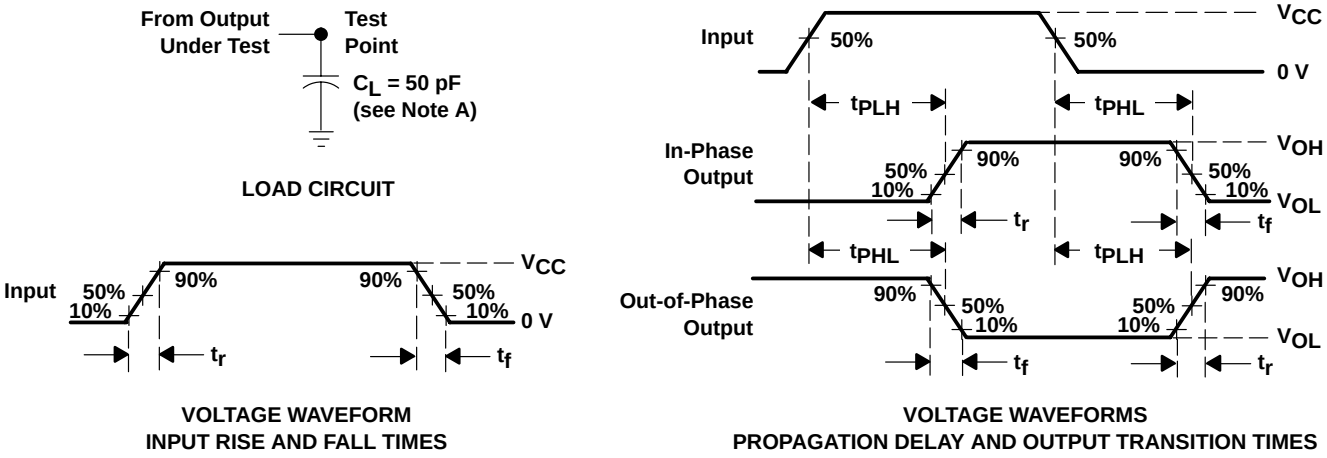
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	V_{CC}	T_A = 25°C			CD74HC08-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 50 pF	2 V			90		135	ns
				4.5 V			18		27	
				6 V			15		23	
			C_L = 15 pF	5 V		7				
t_t		Y	C_L = 50 pF	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	

operating characteristics, T_A = 25°C, V_{CC} = 5V

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate (see Note 4)	No load	37	pF

NOTE 4: C_{pd} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_I (C_{pd} + C_L)$
f_I = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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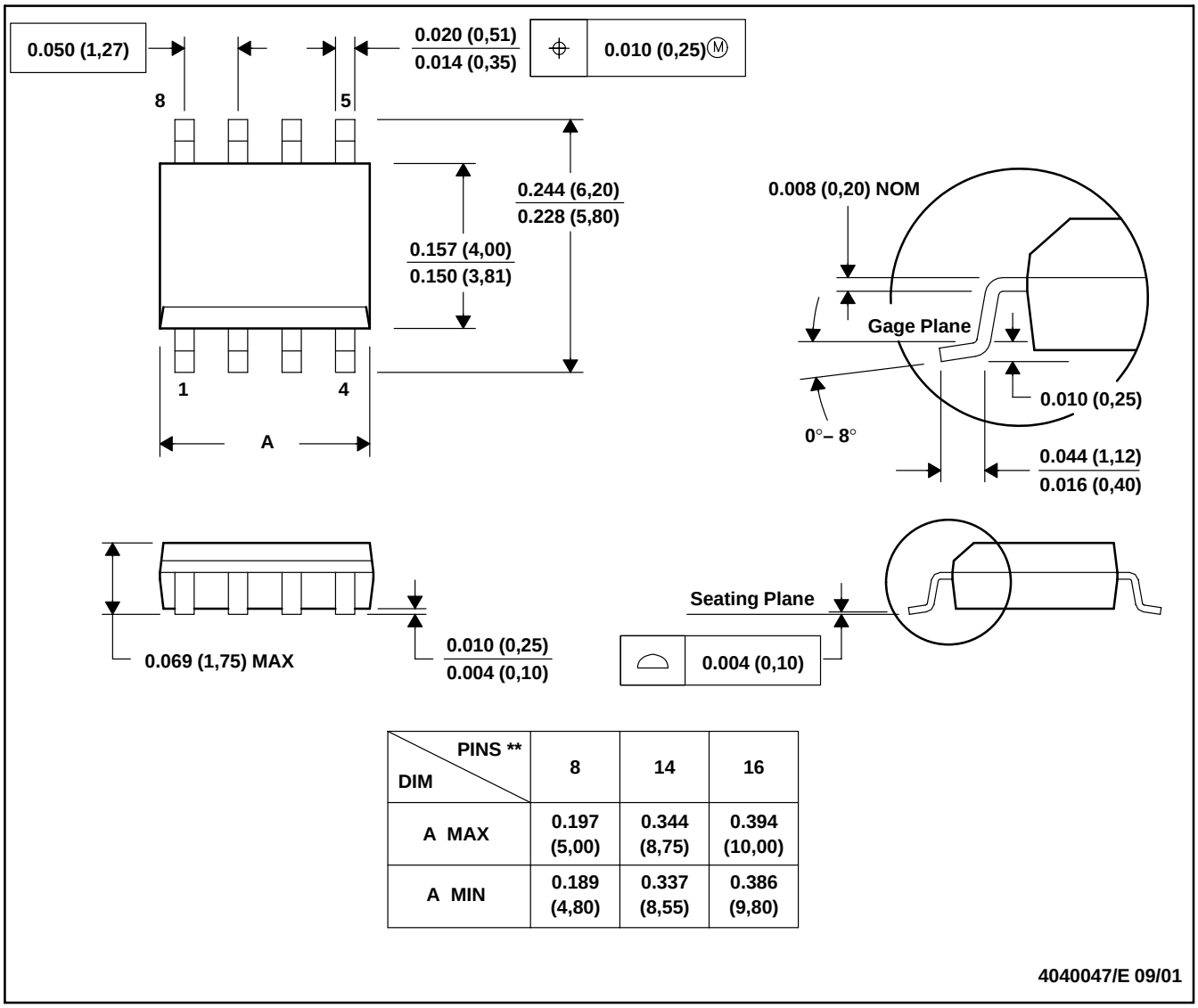
D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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