CYPRESS SEMICONDUCTOR

64K x 4 Static R/W RAM with Separate I/O

Features

- **High speed**
  - **— 10 ns t_{AA}**
- **Automatic power-down when deselected**
- **Transparent write (7B191)**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 850 mW**
- **Low standby power**
  - **— 200 mW**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B191 and CY7B192 are high-performance BiCMOS static RAMs organized as 64K words by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 60% when deselected.

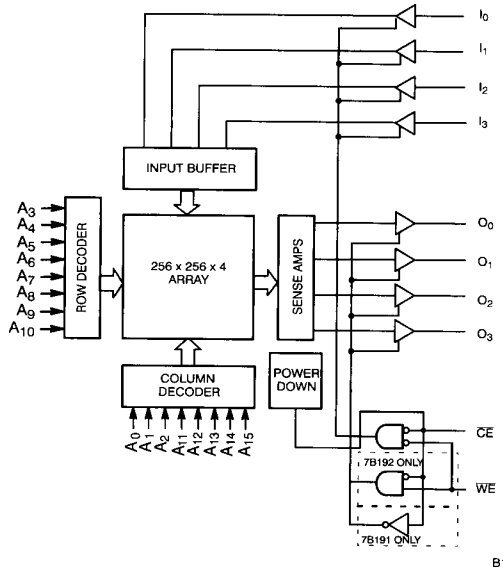
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data output pins.

The four output pins (O_0 through O_3) are in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). During a write operation ($\overline{WE}$ and $\overline{CE}$ LOW), the outputs of the 7B192 are in a high-impedance state and the outputs of the 7B191 track the inputs after a specified delay.

The CY7B191 and CY7B192 are available in space-saving 300-mil-wide DIPs and SOJs.

Logic Block Diagram



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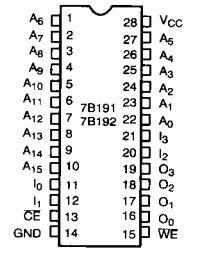
Pin Configuration

DIP/SOJ
Top View



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Selection Guide

		7B191-10 7B192-10	7B191-12 7B192-12	7B191-15 7B192-15	7B191-20 7B192-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	170	160	150	
	Military		170	160	160
Maximum Standby Current (mA)	Commercial	40	35	30	
	Military		40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		.7B191−10 7B192−10 Min.	.7B191−10 7B192−10 Max.	7B191−12 7B192−12 Min.	7B191−12 7B192−12 Max.	7B191−15, 20 7B192−15, 20 Min.	7B191−15, 20 7B192−15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		170		160		150	mA
			Mil				170		160	
I_{SB}	Automatic CE Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		40		35		30	mA
			Mil				40		40	

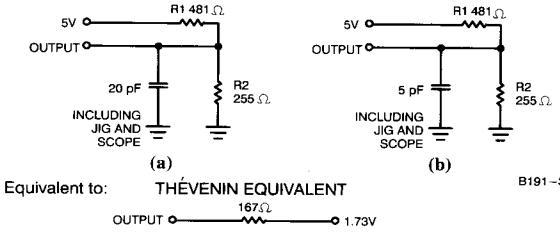
Capacitance[5]

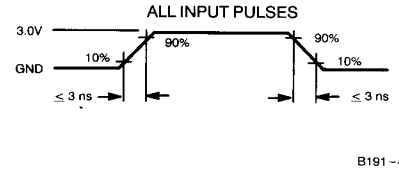
Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}, $C_{I/O}$	Output Capacitance		8	pF

Notes:

1. $V_{IL\,(min.)}$ = − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. For PDIP (P21) and CDIP (D22), C_{IN}=C_{OUT}=10pF.

AC Test Loads and Waveforms





Switching Characteristics[3,7] Over the Operating Range

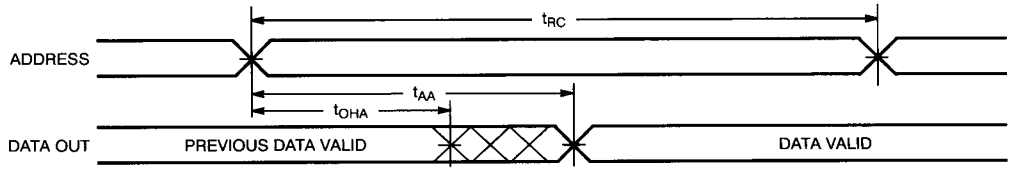
Parameter	Description	7B191–10 7B192–10		7B191–12 7B192–12		7B191–15 7B192–15		7B191–20 7B191–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,9]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[10]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8,9]		6		7		7		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7B191)		10		12		15		20	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7B191)		10		12		15		20	ns
t_{ADV}	Data Valid to Output Valid (7B191)		10		12		15		20	ns

Notes:

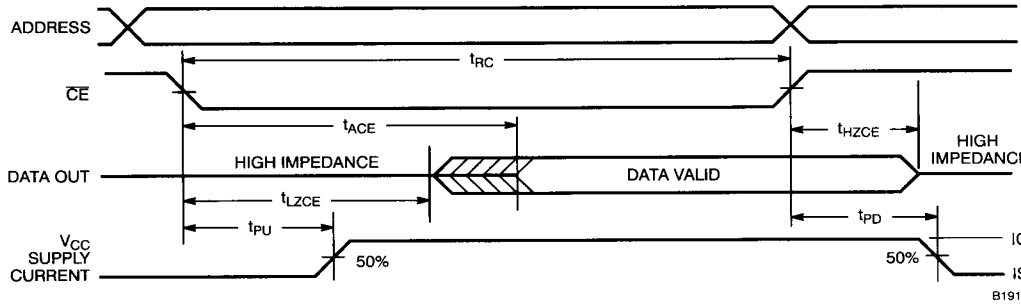
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
9. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

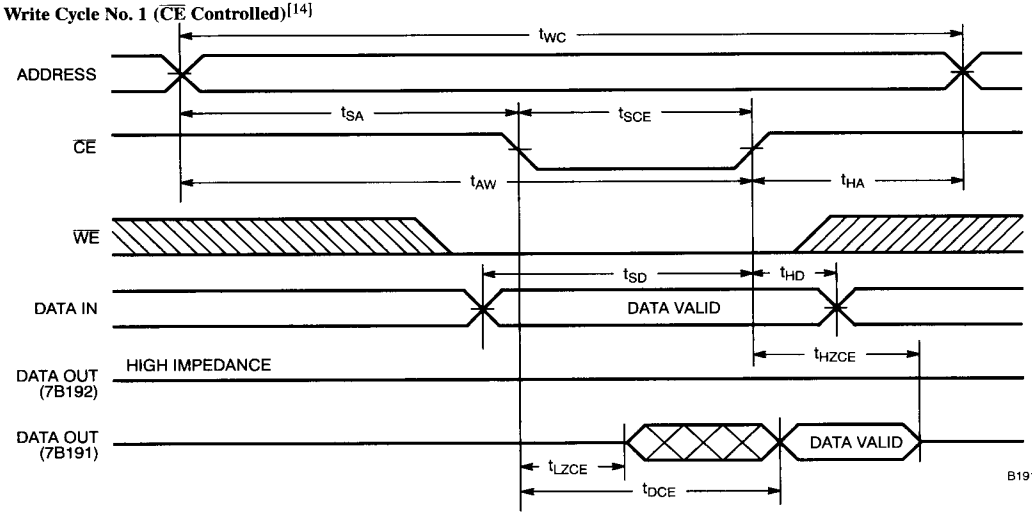
Read Cycle No. 1[11,12]



Read Cycle No. 2[12,13]



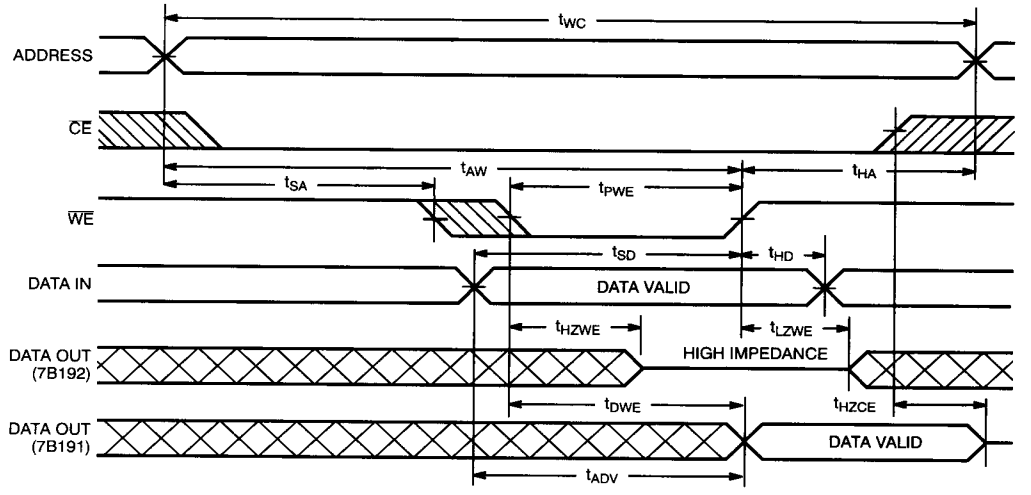
Write Cycle No. 1 (CE Controlled)[14]



Notes:
11. Device is continuously selected. $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Write Cycle No. 2 ($\overline{WE}$ Controlled)[14]



Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7B192: Standard Write	Active (I_{CC})
L	L	Data In	7B191: Transparent Write[15]	Active (I_{CC})

Notes:
15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B191-10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B191-10VC	V21	28-Lead Molded SOJ	
12	CY7B191-12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B191-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B191-12VC	V21	28-Lead Molded SOJ	
	CY7B191-12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B191-15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B191-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B191-15VC	V21	28-Lead Molded SOJ	
	CY7B191-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B191-20DMB	D22	28-Lead (300-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B192–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B192–10VC	V21	28-Lead Molded SOJ	
12	CY7B192–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B192–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B192–12VC	V21	28-Lead Molded SOJ	
	CY7B192–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B192–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B192–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B192–15VC	V21	28-Lead Molded SOJ	
	CY7B192–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B192–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}	7, 8, 9, 10, 11

Note:
16. 7B191 only.

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