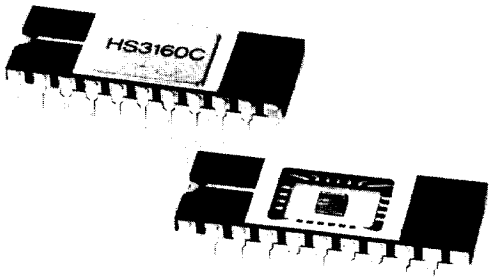
HS3160

MONOLITHIC 16-BIT MDAC

FEATURES

- Monolithic CMOS circuit
- Linearity ±0.003%
- Linearity TC 1.0ppm/°C max
- Latch-up protected
- Small size: 22 pin ceramic DIP
- Commercial and MIL-STD-883 Rev. C processing
- Single power supply: +15VDC
- Low power: 30mW



DESCRIPTION

The HS3160 is a 16-bit CMOS multiplying D/A converter integrated in a single monolithic chip. It represents a major advance in the field of monolithic converter technology, extending resolution to 16 bits and with linearity to 14 bits and 0.003%. The HS3160 accepts AC or DC reference voltages, multiplies in all four quadrants, has latch-up protection, and is packaged in a hermetic 22 pin DIP. Outstanding features of the HS3160 include:

14-Bit Linearity — HS3160 offers a 0.003% integral linearity and a 0.003% differential linearity and is monotonic over the entire specified operating temperature range. The excellent differential linearity is achieved by using a unique bit decoding technique. The transfer function is actually divided into 16 segments (determined by bits 1 to 4), each consisting of 4096 discrete voltage levels (determined by bits 5 to 16). Bits 1 to 4 are digitally decoded into 15 control signals, driving 15 equal current sources, rather than 4 binarily weighted sources; thus, reducing the matching accuracy requirement on the resistors and CMOS switches.

Monolithic Construction — HS3160 is a single chip CMOS circuit using advanced design and manufacturing techniques.

Processing — The HS3160 is offered in two versions. The -C version is commercially processed for applications in the 0°C to 70°C range. The -B version operates in the −55°C to +125°C temperature range and is processed and screened to the requirements of MIL-M-38510 and MIL-STD-883C.

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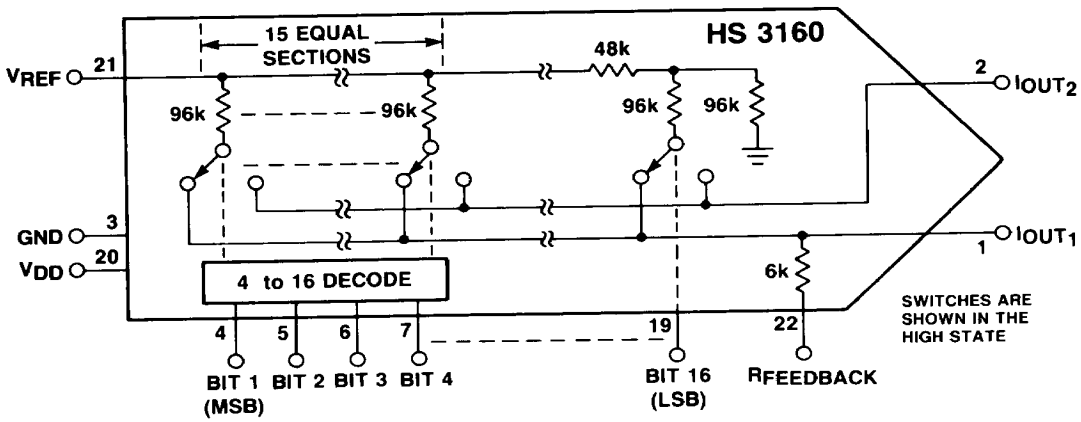
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C, nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

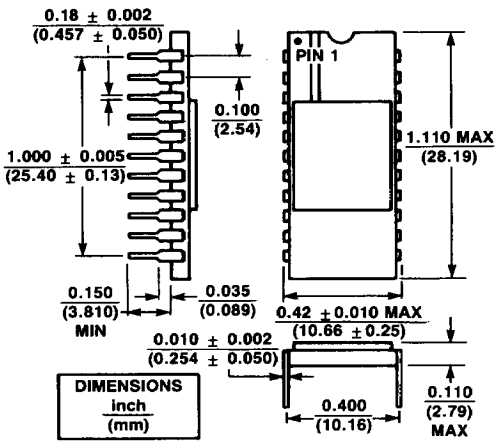
MODEL	HS 3160
TYPE	4 Quadrant Multiplying
DIGITAL INPUTS	
Resolution	16-Bits
2-Quad. Unipolar Coding	Binary
4-Quad. Bipolar Coding	Offset Binary
Logic Compatibility[1]	CMOS, TTL
Input Current	<1μA
REFERENCE INPUT[2]	
Voltage Range	±25V (max), AC or DC
Input Impedance	6.5kΩ ± 50%
ANALOG OUTPUT[7]	
Scale Factor	150μA/V_{REF} ± 50%
Scale Factor Accuracy[3,4]	±1% (max)
Output Leakage	
@ +25°C	10nA (max)
@ +125°C	200nA (max)
Output Capacitance	
C_{out} 1, all inputs high	100 pF
C_{out} 1, all inputs low	50 pF
C_{out} 2, all inputs high	50 pF
C_{out} 2, all inputs low	100 pF
STATIC PERFORMANCE	
Integral Linearity[5]	
HS 3160-3	±0.006% F.S.R. (typ)
	±0.012% F.S.R. (max)
HS 3160-4	±0.003% F.S.R. (typ)
	±0.006% F.S.R. (max)
Differential Linearity[6]	
HS 3160-3	±0.006% F.S.R. (typ)
	±0.012% F.S.R. (max)
HS 3160-4	±0.003% F.S.R. (typ)
	±0.006% F.S.R. (max)
Monotonicity	
HS 3160-3	Guaranteed to 13-Bits
HS 3160-4	Guaranteed to 14-Bits
DYNAMIC PERFORMANCE	
Digital Small Signal Settling	1μS
Digital Full Scale	
Transition Settling	2μS
Reference Feedthrough Error	
(V_{REF} = 20Vpp)	
@ 1kHz	200μV
@ 10kHz	2mV
Reference Input Bandwidth	1MHz
STABILITY (Over specified temp. range)	
Scale Factor[3]	4ppm/°C (typ)
Integral Linearity	0.5ppm F.S.R./°C (typ)
	1ppm F.S.R./°C (max)
Differential Linearity	0.5ppm F.S.R./°C (typ)
	1ppm F.S.R./°C (max)
Monotonicity Temp. Range	
HS 3160C-3/-4	0°C to +70°C
HS 3160B-3/-4	−25°C to +85°C
POWER SUPPLY (V_{DD})[8]	
Nominal Voltage	+15V ±5%
Voltage Range	+8V to +18V
Current	2mA
Rejection Ratio	0.005% F.S.R./%V
TEMPERATURE RANGE	
Operating HS 3160C-3/-4	0°C to +70°C
Operating HS 3160B-3/-4	−55°C to +125°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	22 pin DIP, ceramic

NOTES

1. −0.5V < "0" < +0.8V, 2.4V < "1" ≤ V_{DD}. Worst Case.
2. We recommend our HS REF 01 or R675B-1 for fixed reference application.
3. Using the internal feedback resistor and an external Opamp.
4. The Scale Factor can be adjusted externally by variable resistors in series with the reference input and/or in series to the internal feedback resistor (See APPLICATIONS INFORMATION).
5. Integral Linearity is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
6. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
7. The HS 3160 has been used successfully with OP-07, OP-27 and LF441A. For high speed application HA2525, LF411ACN and OP-01 are recommended.
8. Use series 470Ω resistor to limit startup current — See applications schematics.

CAUTION: ESD (Electro-Static-Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed.

CASE DIMENSIONS



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1, $I_{OUT\ 1}$	22	R FEEDBACK
2	OUTPUT 2, $I_{OUT\ 2}$	21	V_{REF}
3	GND	20	V_{DD}
4	BIT 1 (MSB)	19	BIT 16 (LSB)
5	BIT 2	18	BIT 15
6	BIT 3	17	BIT 14
7	BIT 4	16	BIT 13
8	BIT 5	15	BIT 12
9	BIT 6	14	BIT 11
10	BIT 7	13	BIT 10
11	BIT 8	12	BIT 9

PRINCIPLES OF OPERATION

The HS 3160 achieves true 14 bit accuracy coupled with 16 bit resolution by using a decoded or segmented DAC scheme to implement this function. The following is a brief description of this approach.

The most common technique for building a D/A converter of n bits is to use n switches to turn n current or voltage sources on or off. The n switches and n sources are designed so that each switch or bit contributes twice as much to the D/A converter's output as the preceding bit. This technique is commonly known as binary weighting and allows an n-bit converter to generate 2^n output levels by turning on the proper combination of bits.

In such binary-weighted converter, the switch with the smallest contribution (the LSB) accounts for only 2^{-n} of the converter's full-scale value. Similarly, the switch with the largest contribution (the MSB) accounts for 2^{-1} or half of the converter's full-scale output. Thus it is easy to see that a given percent change in the MSB will have a greater effect on the converter's output than would a similar percent change in the LSB. For example, a 1% change in the LSB of a 10 bit converter would only affect the output by 0.001% of full-scale. A 1% change in the MSB of the same converter would affect the output by 0.5% of F.S.R.

In order to overcome the problem which results from the large weighting of the MSB, the two MSB's can be decoded to three equally weighted sources. Table 1 shows that all combinations of the two MSB's of a converter result in four output levels. So by replacing the two MSB's with three bits equally weighted at ¼ full-scale and decoding the two MSB digital inputs into three lines which drive the equally weighted bits. The same functional performance can be obtained. Thus by replacing the two MSB switches of a conventional converter with three switches properly decoded, the contribution of any switch is reduced from ½ to ¼. This reduction in sensitivity also reduces the accuracy required of any switch for a given overall converter accuracy.

Table 1. Contribution of the two MSB's

2^{-1}(MSB)	2^{-2}	Output
0	0	0
0	1	¼ Full-Scale
1	0	½ Full-Scale
1	1	¾ Full-Scale

With the decoded converter described above, a 1% change in any of the converter's switches will affect the output by no more than 0.25% of full-scale as compared to 0.5% for a conventional converter. In other words the conventional d-a converter can be made less sensitive to the quality of it's individual bits by decoding.

In the HS 3160 the first four MSB's are decoded into 16 levels which drive 15 equally weighted current sources. The sensitivity of each switch on the output is reduced by a factor of 8. Each of the 15 sources contributes 6.25% output change rather than an MSB change of 50% for the common approach.

Following the decoded section of the DAC a standard binary weighted R-2R approach is used. This divides each of the 16 levels (or 6.25% of F.S.) into 4096 discrete levels (the 12 LSB's).

OUTPUT CAPACITANCE

The HS 3160 has very low output capacitance (C_O). This is specified both with all switches ON and all switches OFF. Output capacitance varies from 50pf to 100pf over all input codes. This low capacitance is due in part to the decoding technique used. Smaller switches are used with resulting less capacitance. Three important system characteristics are affected by C_O and ΔC_O; namely digital feedthrough, settling time, and bandwidth. The DAC output equivalent circuit can be represented as shown in Figure 1.

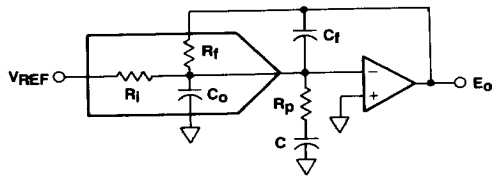


Figure 1. HS 3160 Equivalent Output Circuit

Digital feedthrough is the change in analog output due to the toggling conditions on the converter input data lines when the analog input V_{REF} is at 0V. The HS 3160 has very low C_O and therefore will yield low digital feedthrough. Inputs to the HS 3160 can be buffered. This input latch with microprocessor control is shown in Figure 5.

Settling time is directly affected by C_O. In Figure 1, C_O combines with R_f to add a pole to the open loop response, reducing bandwidth and causing excessive phase shift — which could result in ringing and/or oscillation. A feedback capacitor, C_f must be added to restore stability. Even with C_f, there is still a zero-pole mismatch due to R_iC_O which is code dependent. This code dependent mismatch is minimized when $C_OR_i = R_fC_f$. However C_f must now be made larger to compensate for worst case ΔR_iC_O — resulting in reduced bandwidth and increased settling time. With the HS 3160 small values for C_f must be used. Resistor R_p can be added, this will parrallel R_i decreasing the effective resistance. If C_f is reduced the bandwidth will be increased and settling time decreased. However a system penalty for lowering C_f is to increase noise gain. The tradeoff is noise vs. settling time. If R_p is added then a large value (1mF or greater) non-polarized capacitor C_p should be added in series with R_p to eliminate any DC drifts. If settling time is not important, eliminate R_p and C_p, and adjust C_f to prevent overshoot.

OUTPUT OFFSET

In most applications, the output of DAC is fed into an amplifier to convert the DAC's current output to voltage. A little known and not commonly discussed parameter is the linearity error versus offset voltage of the output amplifier. All CMOS DAC's must operate into a virtual ground, i.e., the summing junction of an op amp. Any amplifier's offset from the amplifier will appear as an error at the output (which can be related to LSB's of error).

Most all CMOS DAC's currently available are implemented using an R-2R ladder network. The formula for nonlinearity is typically $0.67mV/mV_{OS}$ (not derived here). However the HS 3160 has a coefficient of only $0.065mV/mV_{OS}$!! This is due to the decoding technique described earlier. CMOS DAC applications notes (including this one) always show a potentiometer used to null out the amplifier's offset. If an amplifier is chosen having 'pretrimmed' offset it may be possible to eliminate this component. Consider the following calculations:

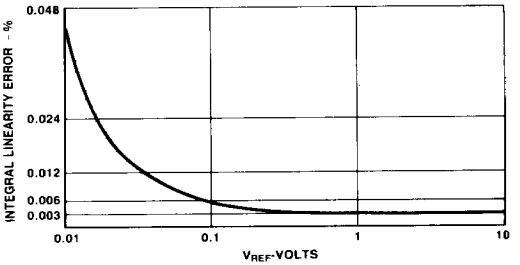
1. Using LF441A amplifier (low power — 741 pinout)
2. Specified offset: 0.5mV max
3. Temperature coefficient of input offset: 10μV/°C max

V_{OS} max (0°C to 70°C) = 0.5mV + (70μV)10 = 1.2mV
Additional nonlinearity (max) = 1.2mV × 0.065mV/mV
= 78μV (½LSB @ 16 Bits!)

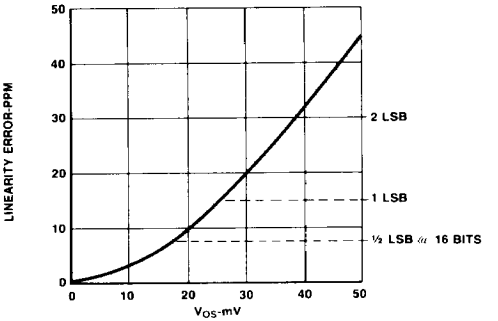
Where: 78μV ≅ ½LSB @ 16 Bits (10V range)

CHARACTERISTIC CURVES

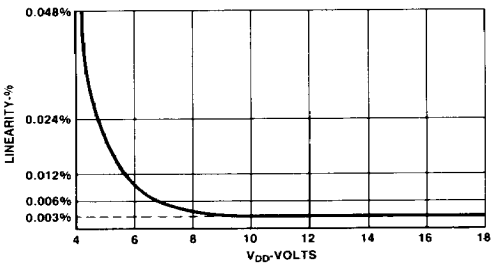
(Typical @ +25°C, V_{DD} = +15VDC, V_{REF} = +10VDC, unless otherwise noted.)



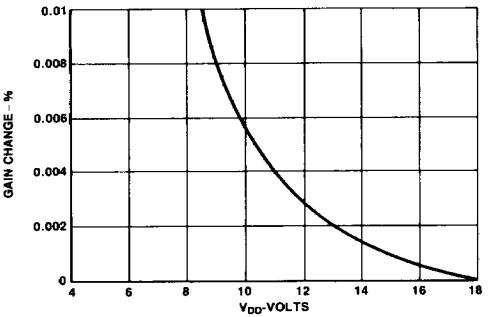
Integral Linearity Error vs. Reference Voltage



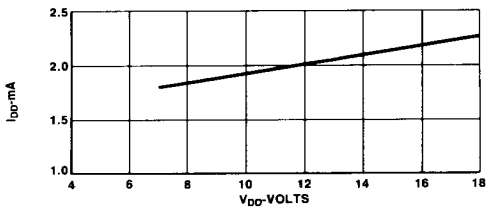
Additional Linearity Error vs. Output-Amplifier Offset-Voltage
(V_{REF} = + 10V)



Linearity vs. Supply Voltage

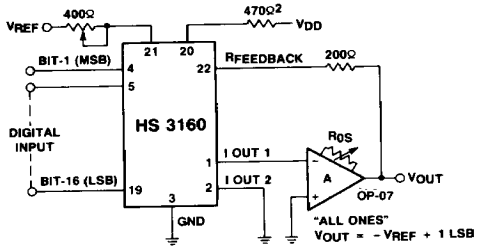


Gain Change vs. Supply Voltage



Power Supply Current vs. Voltage

APPLICATIONS INFORMATION

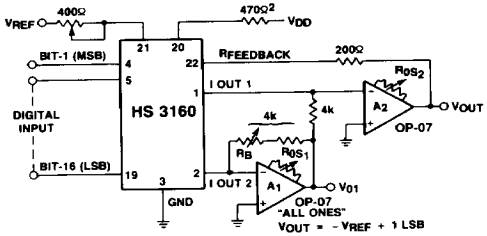


NOTES:
1. To maintain specified HS 3160 linearity, the external amplifier (A) must be zeroed.
   Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ± 1mV.
2. Series resistor recommmended to limit current during 'turn-on'.

Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-N})$
100...001	$-V_{REF}(½+2^{-N})$
100...000	$-V_{REF}/2$
011...111	$-V_{REF}(½-2^{-N})$
000...001	$-V_{REF}(2^{-N})$
000...000	0

Figure 2. Unipolar Operation (2-Quadrant Multiplication)

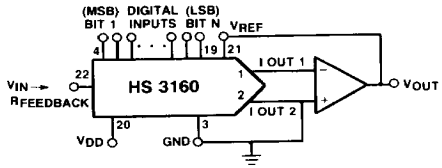


NOTES:
1. To maintain specified HS 3160 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:
   a) Set R_{OS1} for V_{01} = 0
   b) Set R_{OS2} for V_{OUT} = 0
   c) Set V_{REF} to + 10V and adjust R_B for V_{OUT} to be 0 Volts
2. Series resistor recommended to limit current during 'turn-on.'

Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-(N-1)})$
100...001	$-V_{REF}(2^{-(N-1)})$
100...000	0
011...001	$V_{REF}(2^{-(N-1)})$
000...001	$V_{REF}(1-2^{-(N-1)})$
000...000	V_{REF}

Figure 3. Bipolar Operation (4-Quadrant Multiplication)

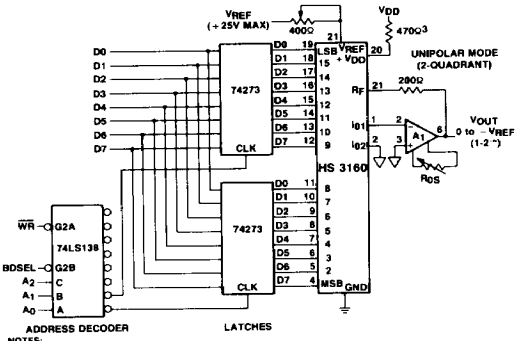


Via the above configuration, the HS 3160 can be used to divide an analog signal by a digital code (i.e, for digitally controlled gain). The transfer function is given as:

$$V_{OUT} = \frac{-V_{IN}}{\frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \frac{\text{Bit 3}}{2^3} + \ldots + \frac{\text{Bit N}}{2^N}}$$

where the value of each bit is 0 or 1. Division by all "0"s is undefined and causes the op amp to saturate.

Figure 4. Analog/Digital Division



NOTES:
1. A_1 can be selected with low pretrimmed offset. R_{OS} could then be replaced with a fixed R.
2. HS REF-01 recommended for fixed reference applications.
3. Series resistor recommmended to limit current during 'turn-on'.

Figure 5. Microprocessor Interface to HS 3160

APPLICATIONS INFORMATION

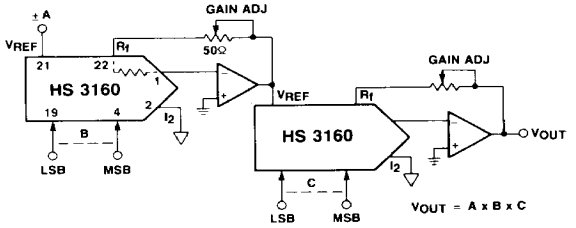


Figure 6. Cascade Multiplication

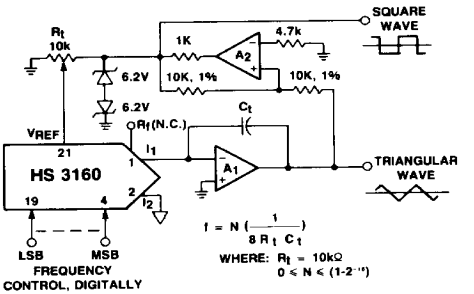


Figure 7. Programmable Function Generator

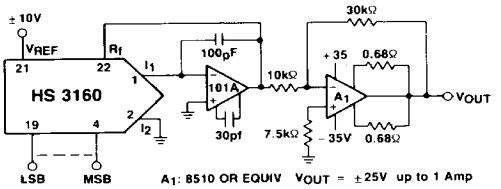


Figure 8. DAC Controlled Power Output

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	LINEARITY RESOLUTION	LINEARITY ERROR (MAX)	MONOTONIC RANGE	TEMP RANGE	SCREENING
HS 3160C-3	16 BITS	0.012%	0°C to +70°C	0°C to +70°C	—
HS 3160C-4	16 BITS	0.006%	0°C to +70°C	0°C to+ 70°C	—
HS 3160B-3	16 BITS	0.012%	−25°C to +85°C	−55°C to +125°C	883C
HS 3160B-4	16 BITS	0.006%	−25°C to +85°C	−55°C to +125°C	883C

Specifications subject to change without notice.