Document Title

512K x 8 Bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Data Sheet 1997.	April 10th 1997	
1.0	Data Sheet 1998.	April 10th 1998	
1.1	Data Sheet 1998.	July 14th 1998	Final

512K x 8 Bit NAND Flash Memory

FEATURES

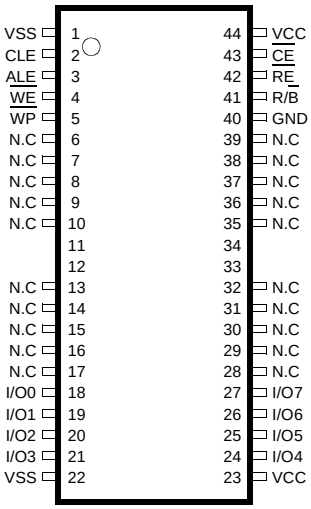
- Single 5.0 - volt Power Supply
- Organization
  - Memory Cell Array : 512K x 8
  - Data Register : 32 x 8 bit
- Automatic Program and Erase
  - Frame Program : 32Byte in 500 µs
  - Block Erase : 4K Byte in 6ms
- 32-Byte Frame Read Operation
  - Random Access : 15 µs(Max.)
  - Serial Frame Access : 120ns(Min.)
- Command/Address/Data Multiplexed I/O port
- Low Operation Current (Typical)
  - 10µA Standby Current
  - 10mA Read/ Program/Erase Current
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
- 44(40) - Lead TSOP Type II (400mil / 0.8 mm pitch)

GENERAL DESCRIPTION

The KM29N040 is a 512Kx8bit NAND Flash Memory. Its NAND cell structure provides the most cost-effective solution for Digital Audio Recording. A Program operation programs a 32-byte frame in typically 500µs and an Erase operation erase a 4K-byte block in typically 6ms. Data in a frame can be read out at a burst cycle rate of 120ns/byte. The I/O pins serve as the ports for address and data input/output as well as for command inputs. The on-chip write controller automates the Program and Erase operations, including Program or Erase pulse repetition, where required, and performs internal verification of cell data.

The KM29N040 is an optimum solution for flash memory application that do not require the high performance levels or capacity of larger density flash memories. These application include data storage in digital Telephone Answering Devices(TAD) and other consumer applications that require voice data storage.

PIN CONFIGURATION



44(40) TSOP (II)

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC}, V_{SS} or GND inputs disconnected.

PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	Data Inputs/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
GND	Ground Input
$R/\overline{B}$	Ready/Busy output
V_{CC}	Power
V_{SS}	Ground
N.C	No Connection

Figure 1. FUNCTIONAL BLOCK DIAGRAM

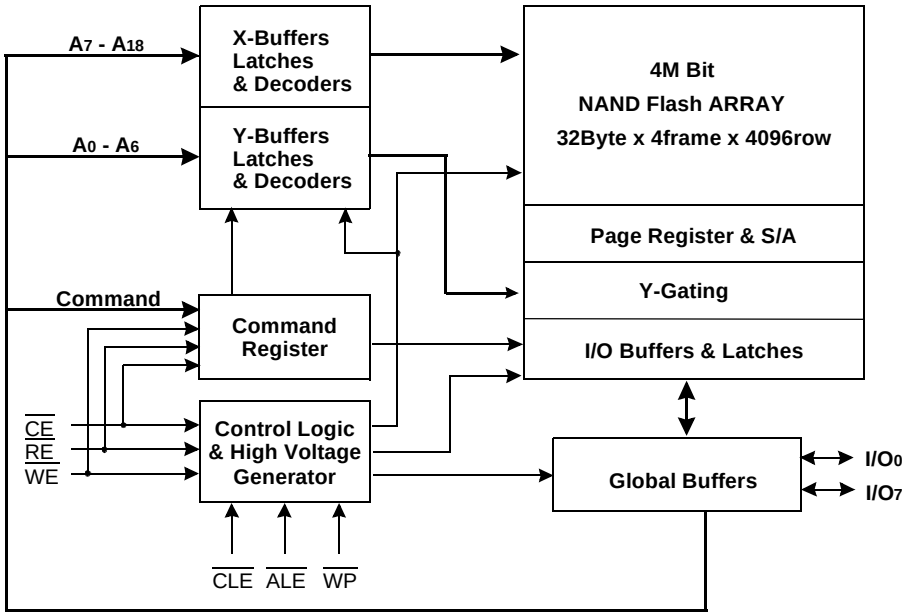
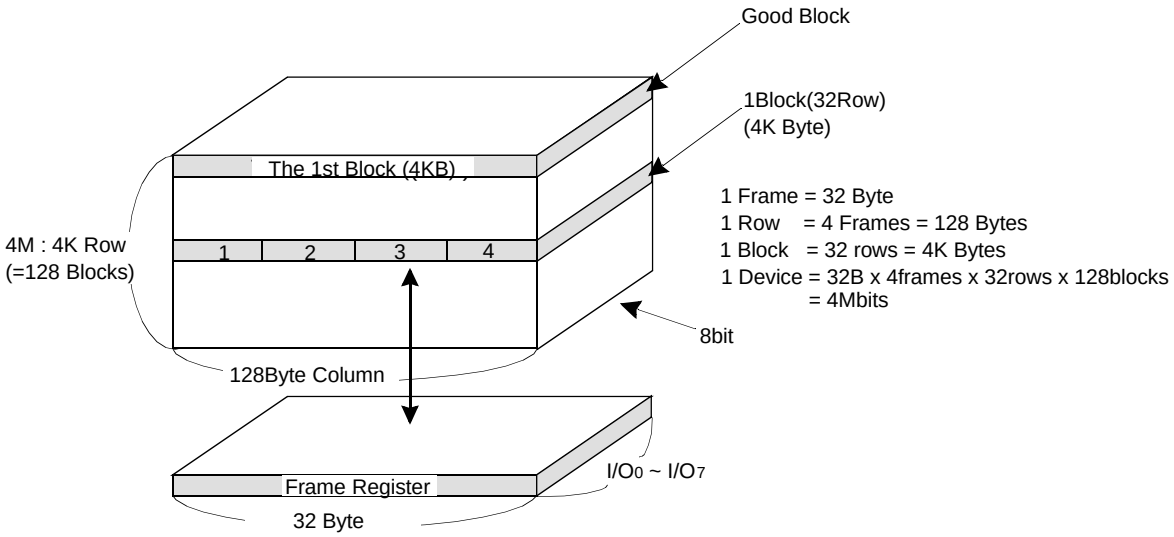


Figure 2. ARRAY ORGANIZATION



	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address (A0-A4) Frame Address (A5-A6)
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	A15	Row Address (A7-A11)
3rd Cycle	A16	A17	A18	X*	(1)X*	X*	*X	*X	Block Address (A12-A18)

NOTE : *(1) : X can be V_{IL} or V_{IH}

PRODUCT INTRODUCTION

The KM29N040 is a 4M bit memory organized as 4096 rows by 1024 columns. A 256-bit data register is connected to memory cell arrays accommodating data transfer between the registers and the cell array during frame read and frame program operations. The memory array is composed of unit NAND structures in which 8 cells are connected serially.
Each of the 8 cells reside in a different row. A block consists of the 32 rows, totaling 4096 NAND structures of 8bits each. The array organization is shown in Figure 2. The program and read operations are executed on a frame basis, while the erase operation is e xecuted on a block basis. The memory array consists of 128 separately erasable 4K-byte blocks.

The KM29N040 has addresses multiplexed into 8 I/O pins. This scheme not only reduces pin count but allows systems upgrades to higher density flash memories by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles. For byte-level addressing, the 512K byte physical space requires a 19-bit address, low row address and high row address. Frame Read and frame Program require the same three address cycles following by a command input. In the Block Erase operation, however, only the two row address cycles are required.
Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the KM29N040.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read	00h	-	
Reset	FFh	-	O
Frame Program	80h	10h	
Block Erase	60h	D0h	
Status read	70h	-	O
Read ID	90h	-	

PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the path activation for address and input data to the internal address/data register. Addresses are latch ed on the rising edge of $\overline{WE}$ with ALE high, and input data is latched when ALE is low.

Chip Enable($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

I/O Port : I/O_0 ~ I/O_7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high- z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/$\overline{Busy}$($R/\overline{B}$)

The $R/\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	-0.6 to +7.0	V
Temperature Under Bias	KM29N040T	T_{BIAS}	-10 to +125	°C
	KM29N040IT		-40 to +125	
Storage Temperature		T_{STG}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

NOTE:
1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, KM29N040T:T_A=0 to 70°C, KM29N040IT:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Current	Burst Read Cycle	I_{CC1}	tcycle=120ns	$\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	20	mA
	Command, Address Input	I_{CC3}	tcycle=120ns		-	10	20	
	Data Input	I_{CC4}	tcycle=120ns		-	10	20	
	Program	I_{CC5}	-		-	10	20	
	Erase	I_{CC6}	-		-	10	20	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}		-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}		-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to 5.5V		-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to 5.5V		-	-	±10	
Input High Voltage, All inputs		V_{IH}	-		2.4	-	V_{CC}+0.5	V
Input Low Voltage, All inputs		V_{IL}	-		-0.3	-	0.8	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA		2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA		-	-	0.4	
Output Low Current(R/$\overline{B}$)		$I_{OL}(R/\overline{B})$	V_{OL}=0.4V		8	10	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	125	-	128	Block

NOTE :
1. The KM29N040 may or may not include bad blocks. Bad blocks are defined as blocks that contain one or more bad bits. Do not try to access these bad blocks for program and erase. The Minimum valid blocks are guaranteed for 10 years data retention or 1M program erase cycling. (Refer to the attached technical notes)
2. The 1st block, which is placed on 00h block address, is guaranteed to be a good block.

AC TEST CONDITION

(KM29N040T:T_A=0 to 70°C, KM29N040IT:T_A=-40 to 85°C, V_{CC}=5V±10% unless otherwise noted)

Parameter	Value
Input Pulse Levels	0.4V to 2.6V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and CL=100pF

CAPACITANCE (T_A=25°C, V_{CC}= 5V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(3clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(3clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Sequential Read & Data Output	
L	L	L	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2]	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	0.5	1	ms
Number of Partial Program Cycles in the Same Frame	Nop	-	-	10	cycles
Block Erase Time	t_{BERS}	-	6	10	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	50	-	ns
CLE Hold Time	t_{CLH}	50	-	ns
$\overline{CE}$ Setup Time	t_{CS}	50	-	ns
$\overline{CE}$ Hold Time	t_{CH}	50	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	60	-	ns
ALE Setup Time	t_{ALS}	50	-	ns
ALE Hold Time	t_{ALH}	50	-	ns
Data Set-up Time	t_{DS}	40	-	ns
Data Hold Time	t_{DH}	20	-	ns
Write Cycle Time	t_{WC}	120	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	40	-	ns

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	15	µs
ALE to $\overline{RE}$ Delay	t_{AR}	250	-	ns
$\overline{CE}$ low to $\overline{RE}$ low (ID read)	t_{CR}	250	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	100	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	60	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	200	ns
Read Cycle Time	t_{RC}	120	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	50	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	0	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	50	ns
$\overline{RE}$ High Hold Time	t_{REH}	40	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read)(1)	t_{CRY}	-	100+tr(R/$\overline{B}$)(2)	ns
$\overline{RE}$ Low to Status Output	t_{RSTO}	-	60	ns
$\overline{CE}$ Low to Status Output	t_{CSTO}	-	70	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	50	-	ns
$\overline{RE}$ access time(Read ID)	t_{WHRID}	100	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	5/10/500	µs

NOTE : 1. If $\overline{CE}$ goes high within 50ns after the third address input, R/$\overline{B}$ will not return to V_{OL}.
2. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.

KM29N040 Technical Notes

INVALID BLOCKS

The KM29N040 Flash device may or may not contain up to 3 invalid blocks. Invalid blocks are defined as blocks that contain one o r more invalid bits. Typically, an invalid block will contain a single bad bit. Devices with invalid block(s) have the same qualit y levels as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance o f valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design mus t be able to mask out the invalid block(s) via address mapping. The 1st block of the KM29N040, however, is fully guaranteed to be a g ood block.

Identifying Invalid Block(s) in the KM29N040

All device locations are erased(FFh) prior to shipping. Device with invalid Block(s) will be randomly written with 00h data with in the first or second page in the invalid Block(s). This page may or may not contain the invalid cell(s). The 00h data just marks the block(s) that contains the invalid cell(s). A system that can utilize these devices must be able to recognize invalid block(s) via the fo llowing suggested flow chart
(Figure 1).

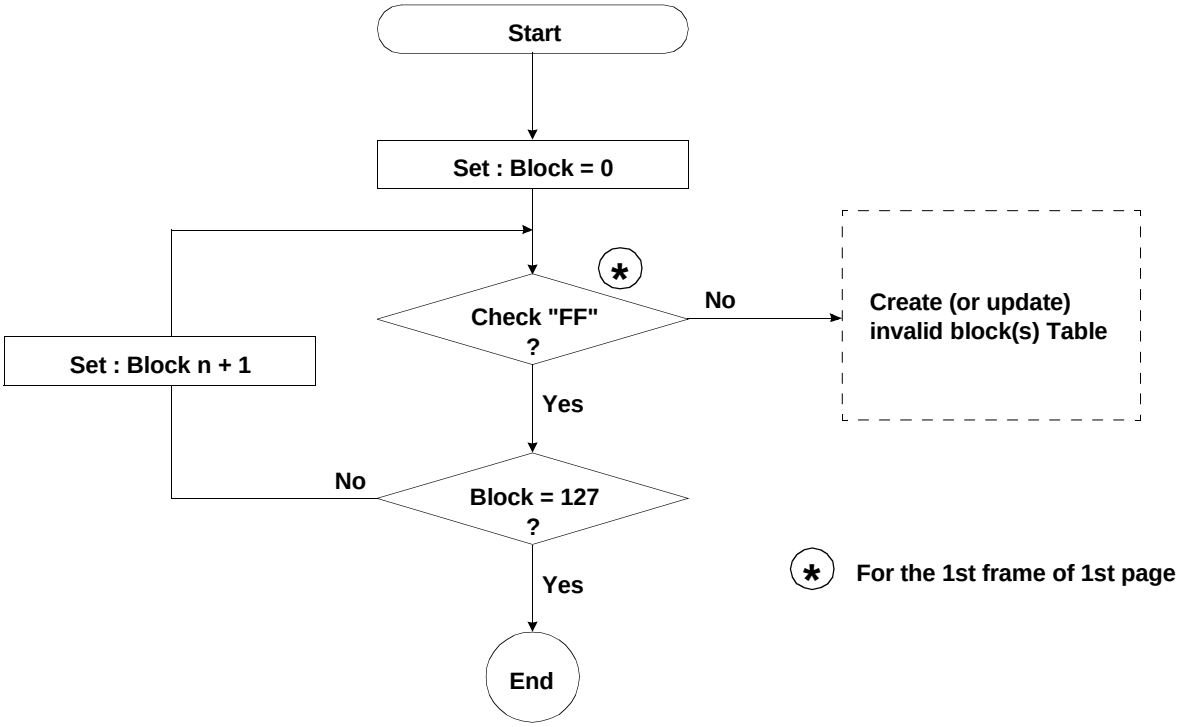


Figure 1. Flow chart to create invalid block table.

KM29N040 Technical Notes(Continued)

Error in program or erase operation

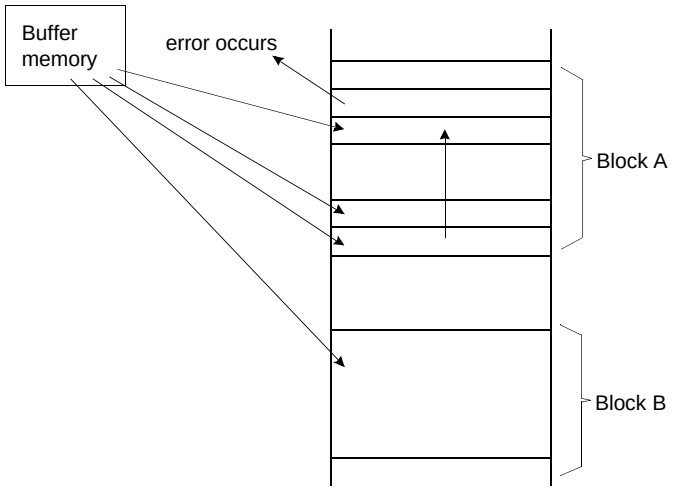
The device may fail during a program or erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

Failure Mode		Detection and Countermeasure sequence
Block	Erase Failure	Read after Erase --> Block Replacement
Frame	Program Failure	Status Read after Program --> Block Replacement
Single Bit	Program Failure ("1" --> "0")	Block Verify after Program --> Retry or ECC

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Block Replacement

During Program operation ;

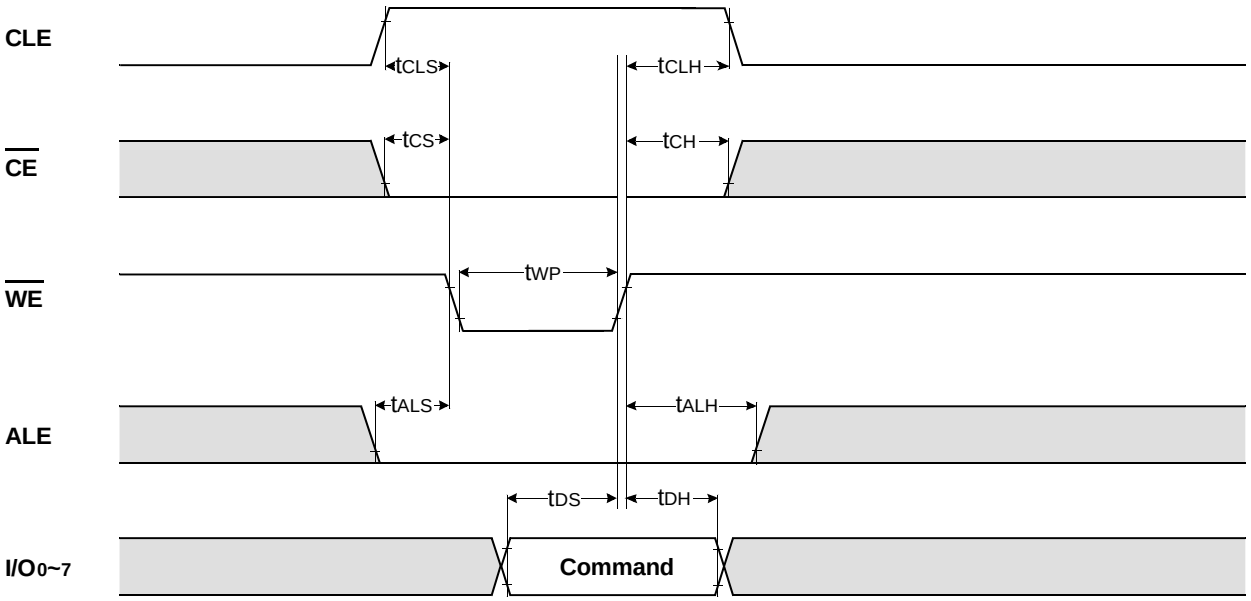


When the error happens in Block "A", try to reprogram the data into another Block "B" by reloading from an external buffer. Then, prevent further system access to Block "A"(by creating a "bad block" table or other appropriate scheme.)

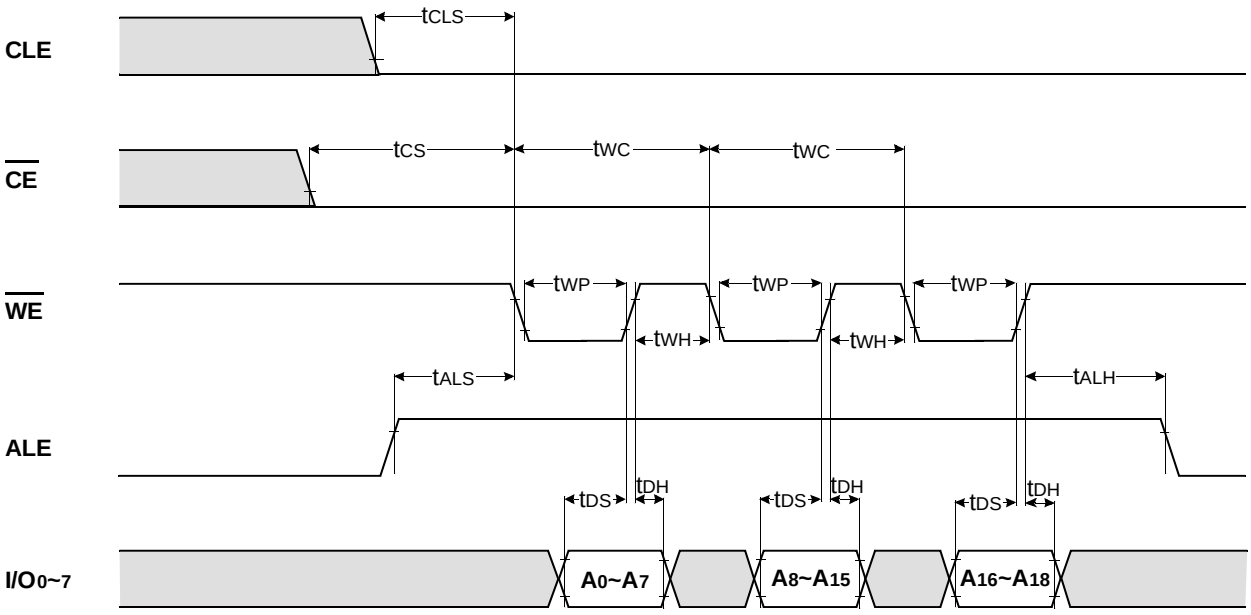
During Erase operation ;

When the error occurs after an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme.)

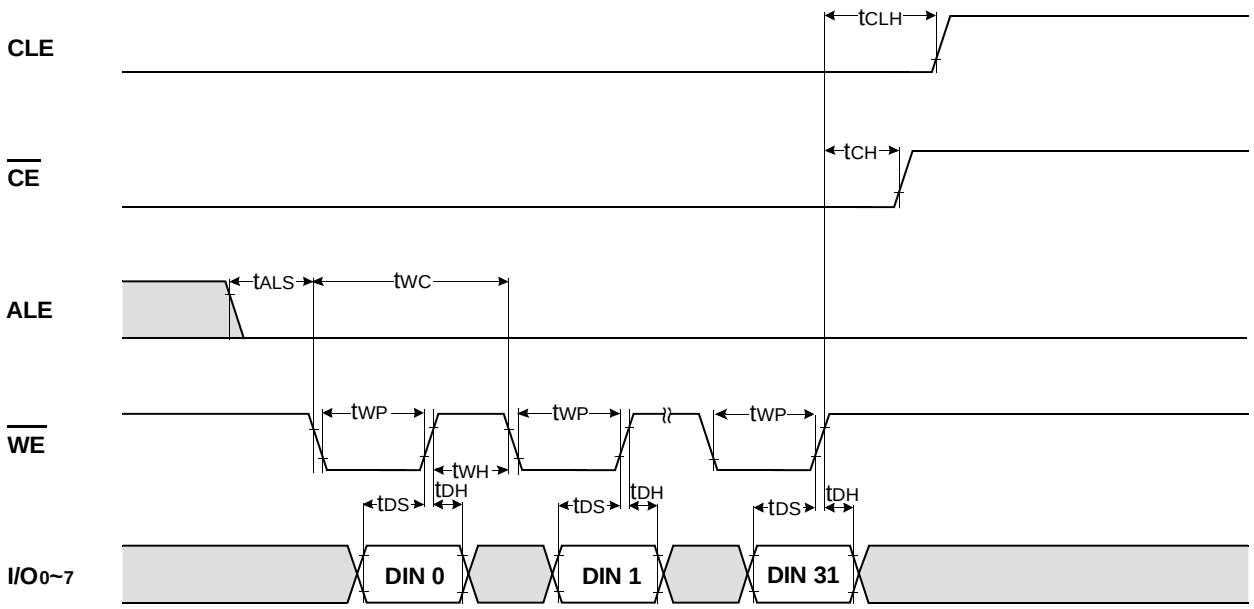
*** Command Latch Cycle**



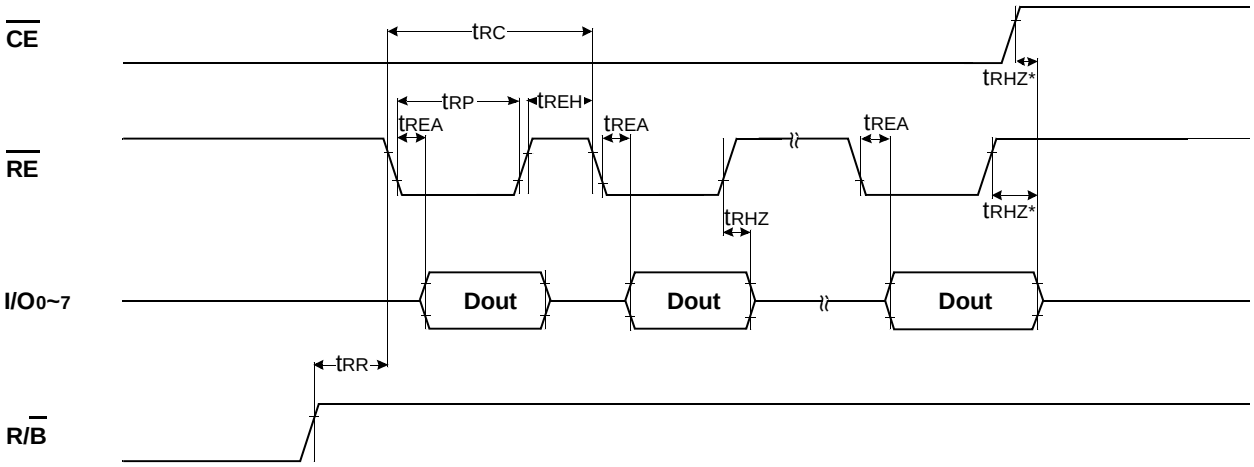
*** Address Latch Cycle**



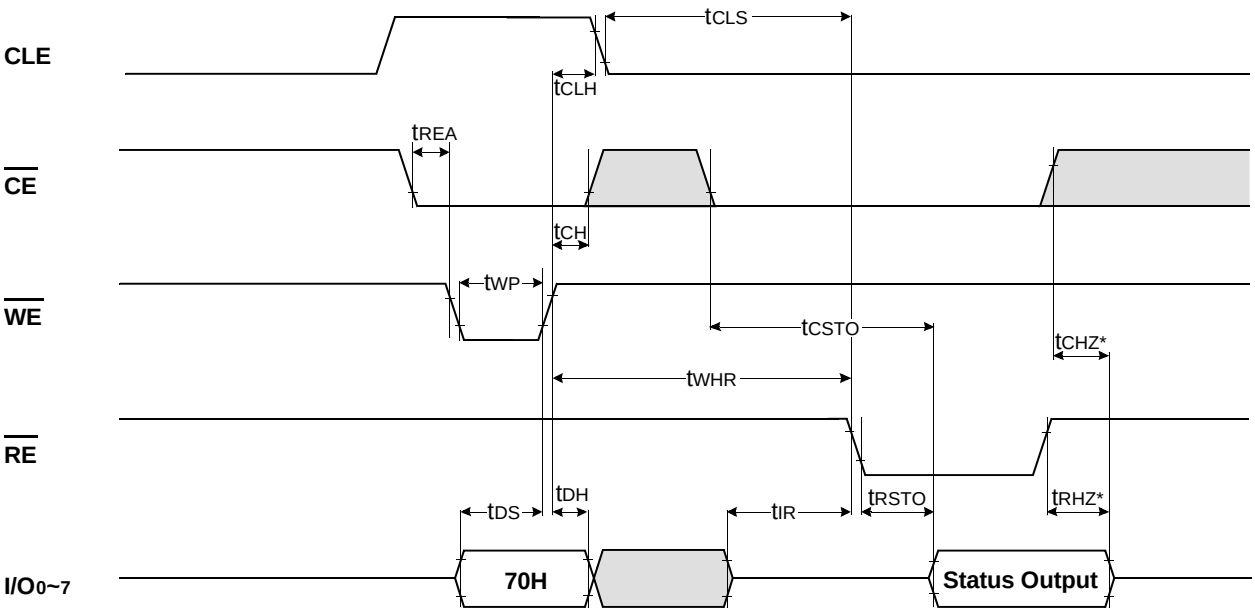
*** Input Data Latch Cycle**



*** Burst Read Cycle After Frame Access** (CLE=L, $\overline{WE}$=H, ALE=L)

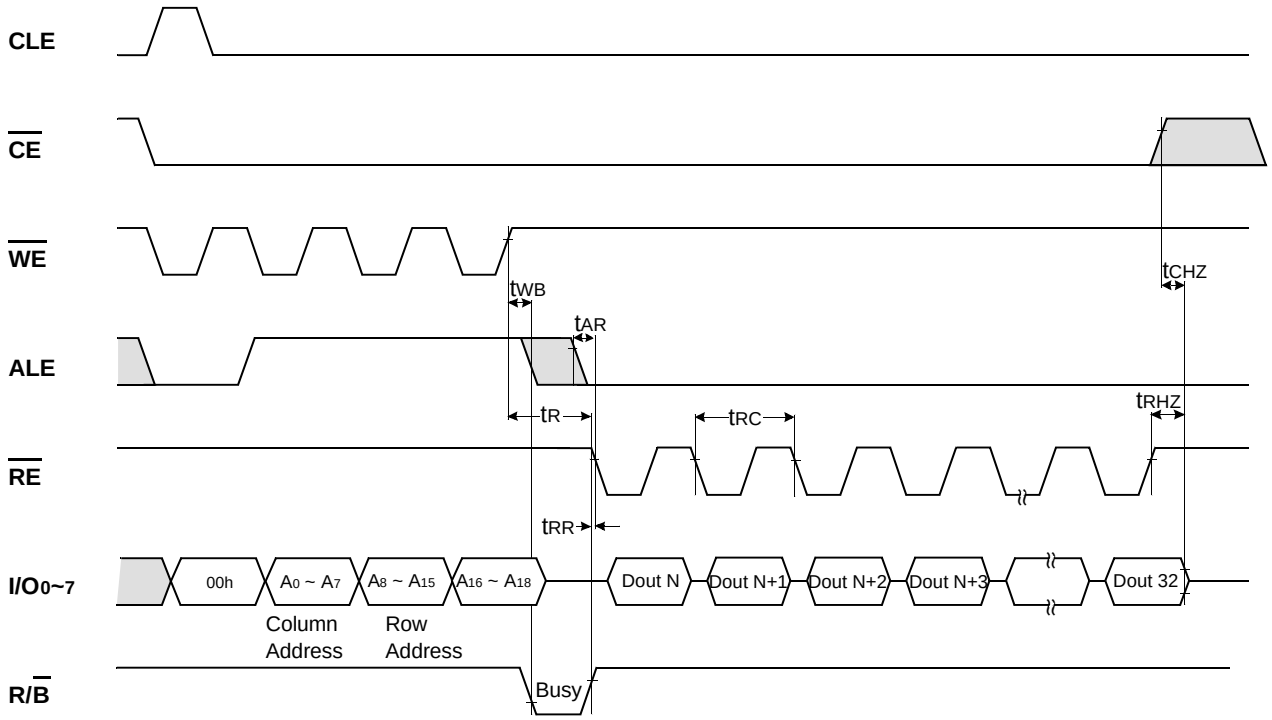


*** Status Read Cycle**

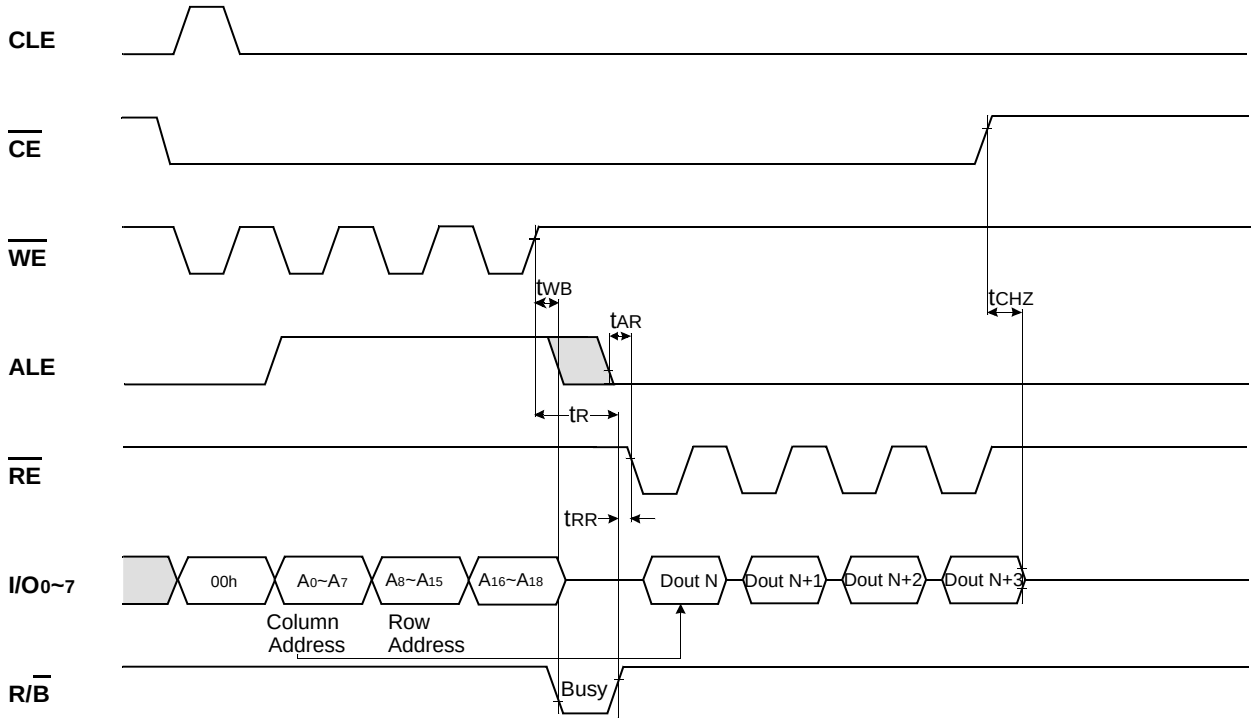


NOTES : Transition is measured±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

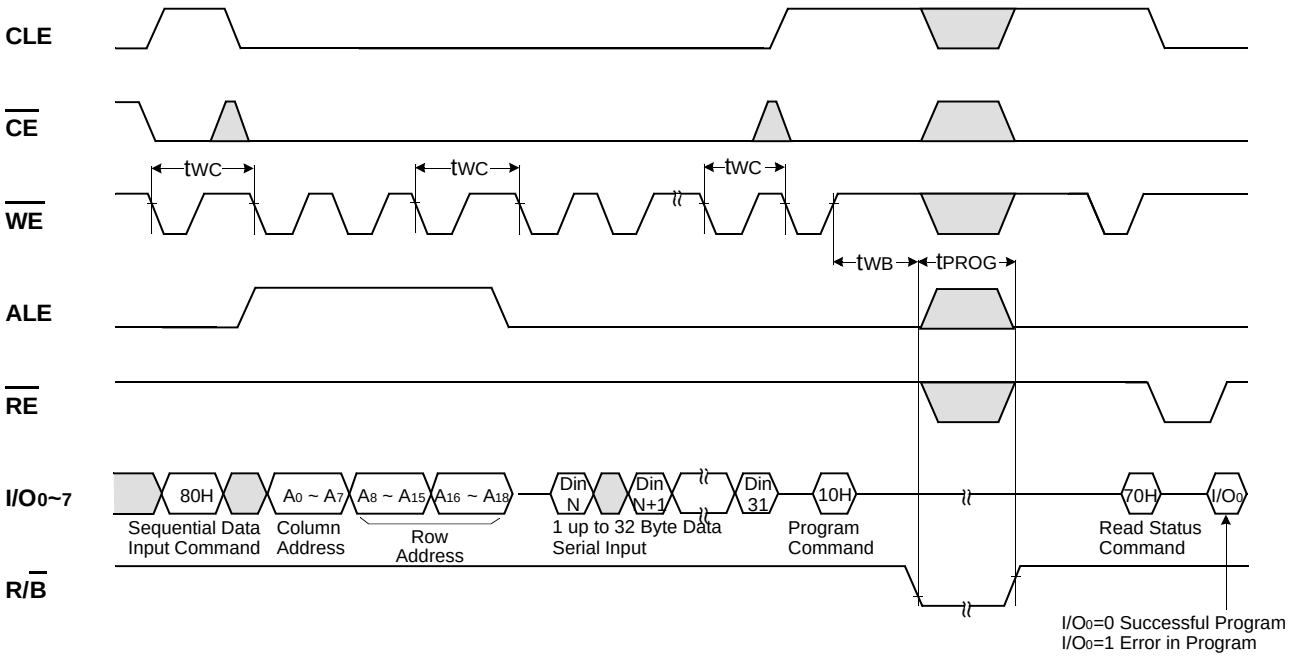
READ OPERATION (READ ONE FRAME)



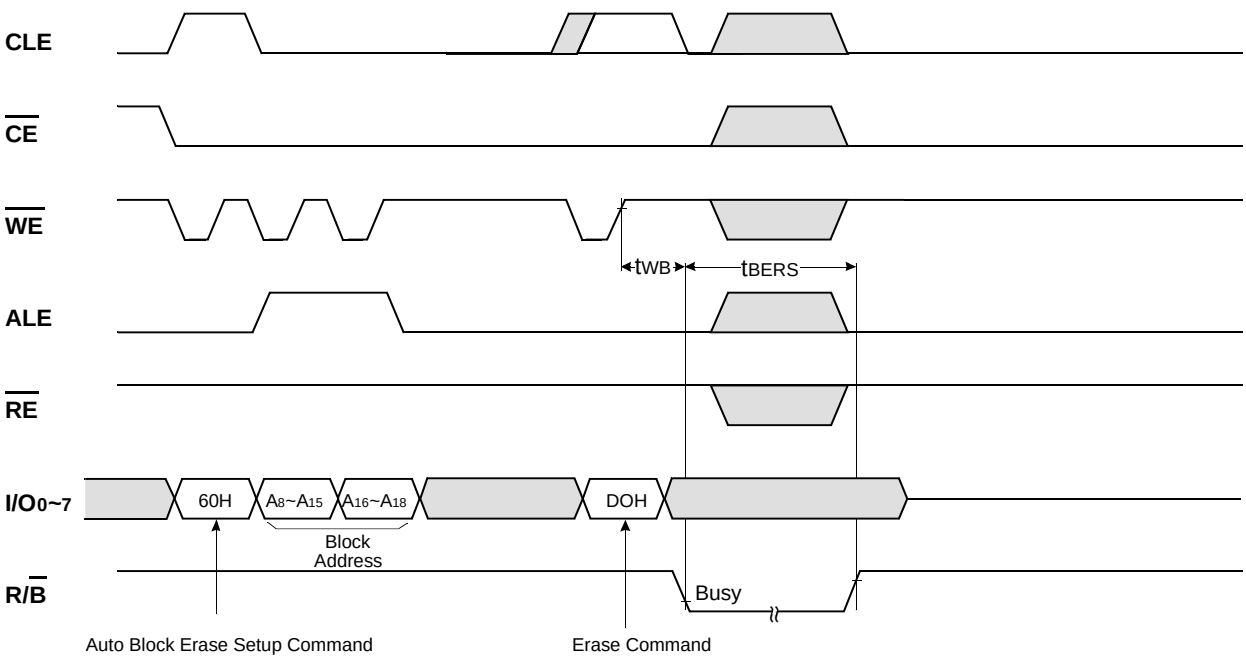
READ OPERATION (INTERCEPTED BY $\overline{CE}$)



PROGRAM OPERATION



BLOCK ERASE OPERATION



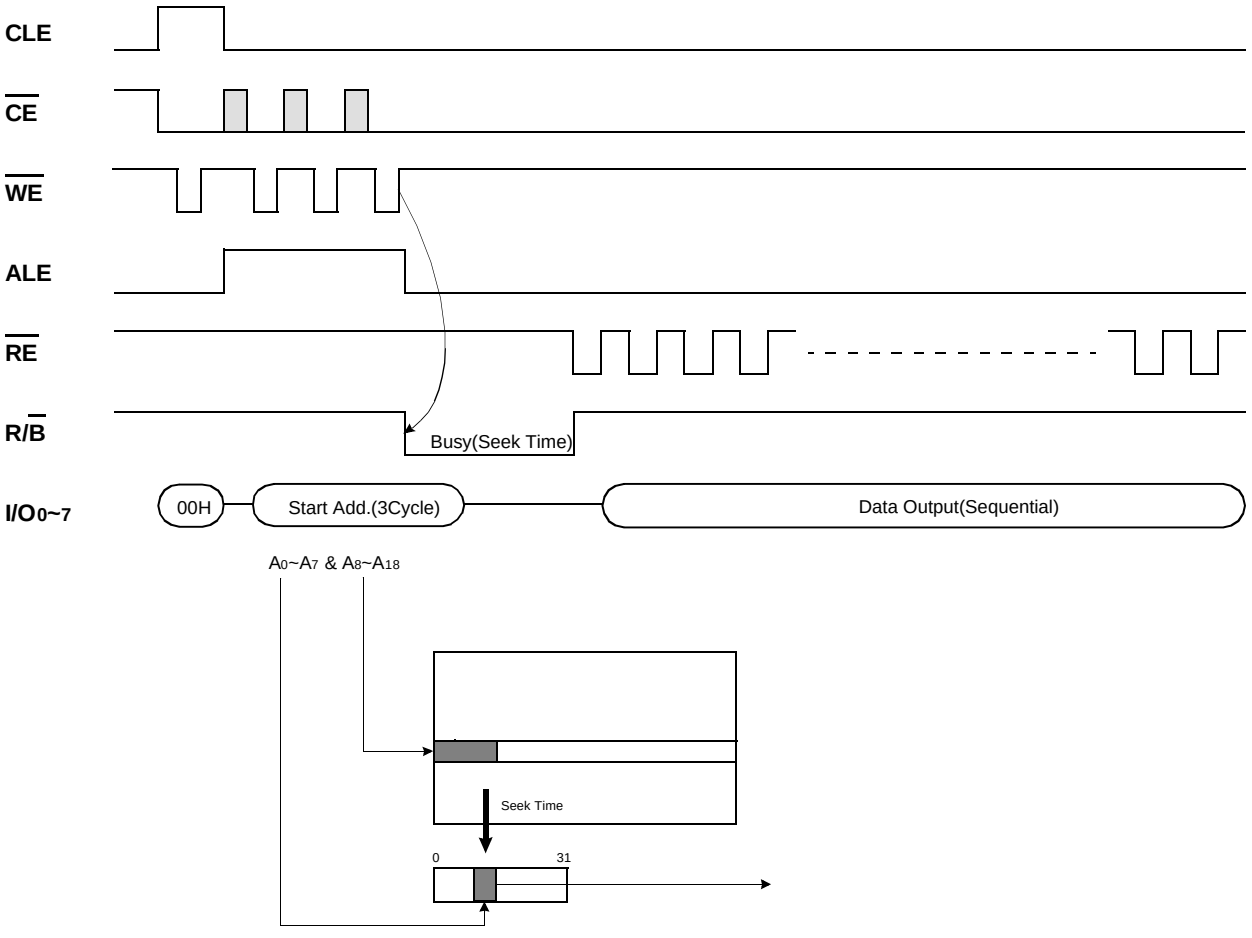
DEVICE OPERATION

FRAME READ

Upon initial device power up or after excution of Reset(FFh) command, the device defaults to Read mode. This operation is also i ni-tiated by writing 00H to the command register along with three address cycles. The three cycle address input must be given for access to each new frame.

The read mode is enabled when the frame address is changed. 32 bytes of data within the selected frame are transferred to the d ata registers in less than 15µs(t_R). The CPU can detect the completion of this data transfer(t_R) by analyzing the output of R/$\overline{B}$ pin. Once the data in a frame is loaded into the registers, they may be read out in 120ns cycle time by sequentially pulsing $\overline{RE}$ with $\overline{CE}$ staying low. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address within the frame(column 32).

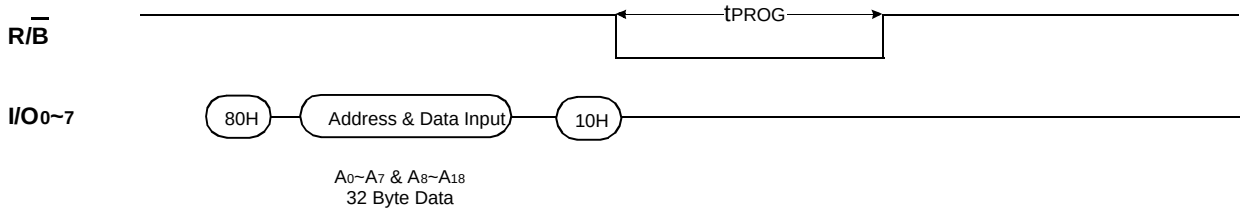
Figure 3. Read Operation



FRAME PROGRAM

The device is programmed on a frame basis. The addressing may be done in random order in a block. A frame program cycle consist of a serial data loading period in which up to 32 bytes of data must be loaded into the device, and a nonvolatile programming p eriod in which the loaded data is programmed into the appropriate cells.
The sequential data loading period begins by inputting the frame program setup command(80H), followed by the three cycle address input and then sequential data loading. The bytes other than those to be programmed do not need to be loaded.
The frame Program confirm command(10H) initiates the programming process. Writing 10H alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and t imings necessary for program and verify, thereby freeing the CPU for other tasks. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the frame Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

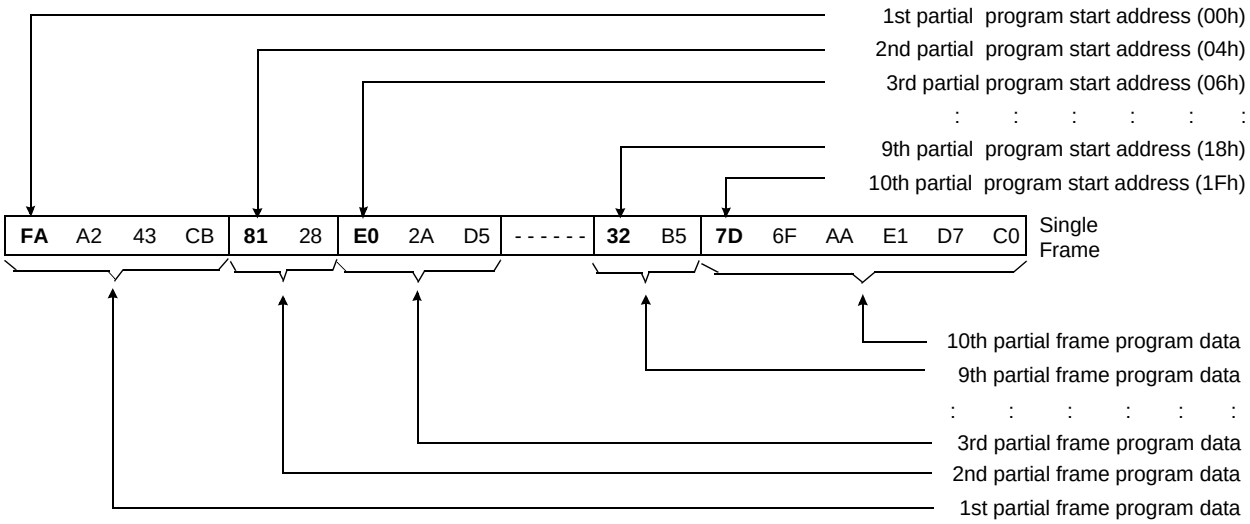
Figure 4. Frame Program Operation



FRAME PROGRAM

While the frame size of the device is 32 Bytes, not all the bytes in a frame have to be programmed at once. The device supports partial frame programming in which a frame may be partially programmed up to 10 separate program operations. The program size in each of the 10 partial program operations is freely determined by the user and do not have to be equal to each other or to any p reset size. However, the user should ensure that the partial program units within a frame do not overlap as "0" data cannot be changed to "1" data without an erase operation. To perform a partial frame program operation, the user only writes the partial frame data t hat is to programmed. Just as in the standard frame program operation, an 80H command is followed by start address data. However, only the partial program data need be divided when programming a frame in 10 partial program operations.

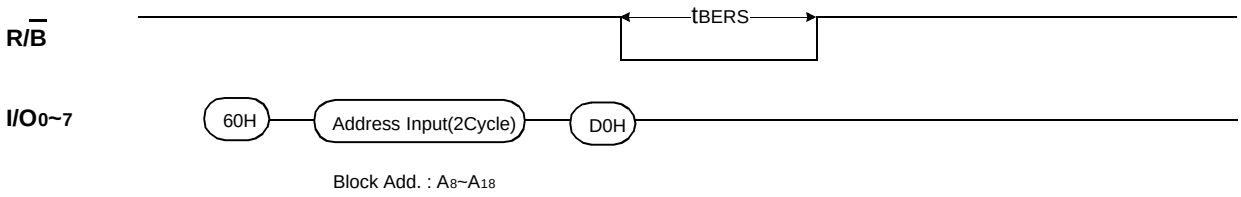
Figure 5. Example of Dividing a Frame into 10 Partial Program Units



BLOCK ERASE

The Erase operation is done 4K Bytes(1 block) at a time. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60H). Only address A_{12} to A_{18} are valid while A_8 to A_{11} is ignored. The Erase Confirm command(D0H) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase, erase-verify and pulse repetition where required.

Figure 6. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is complete, and whether the program or erase operation completed successfully. After writing 70H command to the command register, a read cycle outputs the contents of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the required read command(00H) should be input before serial page read cycle.

Table2. Status Register Definition

SR	Status	Definition
I/O_0	Program	"0" : Successful Program
		"1" : Error in Program
I/O_1	Reserved for Future Use	"0"
I/O2		"0"
I/O_3		"0"
I/O_4		"0"
I/O_5		"0"
		"0"
I/O_6	Device Operation	"0" : Busy "1" : Ready
I/O_7	Write Protect	"0" : Protected "1" : Not Protected

RESET

The device offers a reset feature, executed by writing FFH to the command register. When the device is in Busy state during the read, program or erase mode, the reset operation will abort these operation. In the case of Reset during Program or Erase operations, the contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The device enters the Read mode after completion of Reset operation as shown Table 3. If the device is already in reset state a new reset command will not be accepted to by the command register. The R/$\overline{B}$ pin transitions to low for t_{RST} after the Reset command is written. Reset command is not necessarily for normal device operation. Refer to Figure 7 below.

Figure 7. RESET Operation

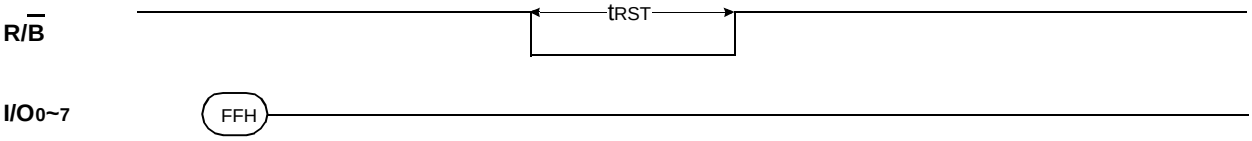
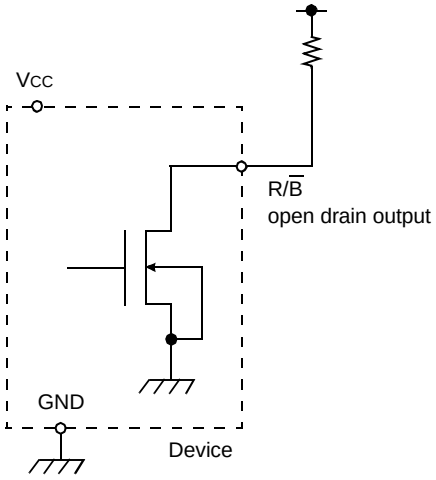


Table3. Device Status

	After Power-up	After Reset
Operation Mode	Read	Read

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a frame program, erase or read seek completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or a random read is begin after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by following equation.



$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{Note*}{8mA + \Sigma I_L}$$

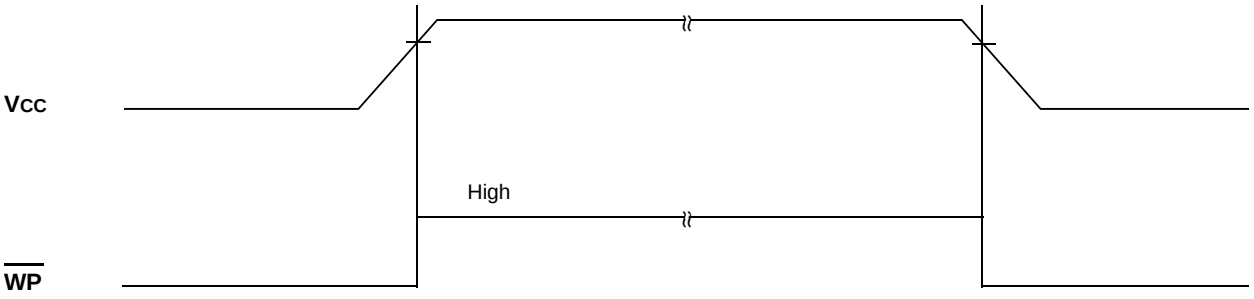
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Note* KM29N040 ; 5.1V
KM29V040 ; 3.2V
KM29W040A ; 5.1V when Vcc=3.6V~5.5V
3.2V when Vcc=3.0V~3.6V

DATA PROTECTTION

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage dete ctor disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down as shown in Figure 8. The two step command sequence for program/erase provides additional software protection.

Figure 8. AC Waveforms for Power Transition

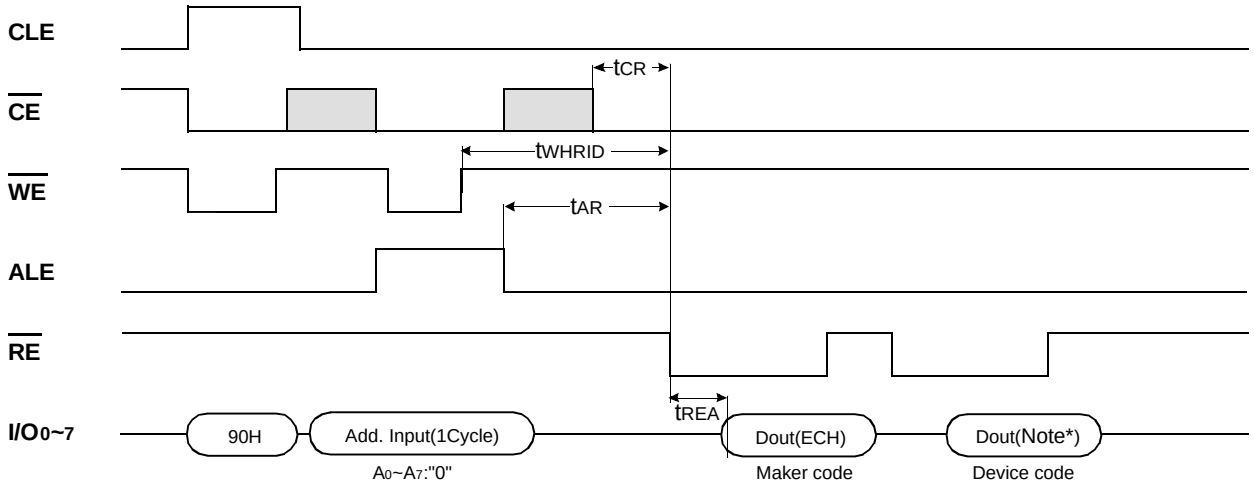


READ ID

The device contains a product identification mode, initiated by writing 90H to the command register, followed by an address inpu t of 00H. Two read cycles sequentially output the manufacture code(ECH), and the device code (Note*). The command register remains in Read ID mode until further commands are issued to it. Figure 9 shows the operation sequence.

Note* : KM29V040 : A4H
KM29N040 : A4H
KM29W040 : A4H

Figure 9. Read ID Operation



PACKAGE DIMENSIONS

44(40) LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)

44(40) - TSOP2 - 400F

Unit :mm/Inch