Q2510/ Q2520

DIGITAL-TO-ANALOG CONVERTERS

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FEATURES

Q2510 Features

- 100 Msps Update Rate
- 10-bit TTL Compatible Digital Input Interface
- Low Glitch Impulse: <1.5 pV-s
- Fast Settling: <4.5 ns to ½ LSB
- Power Dissipation: <1.2 W

Q2520 Features

- 80 Msps Update Rate
- 12-bit TTL Compatible Digital Input Interface
- Low Glitch Impulse: <28 pV-s
- Fast Settling: <27 ns to ±.024%
- Power Dissipation: <790 mW

APPLICATIONS

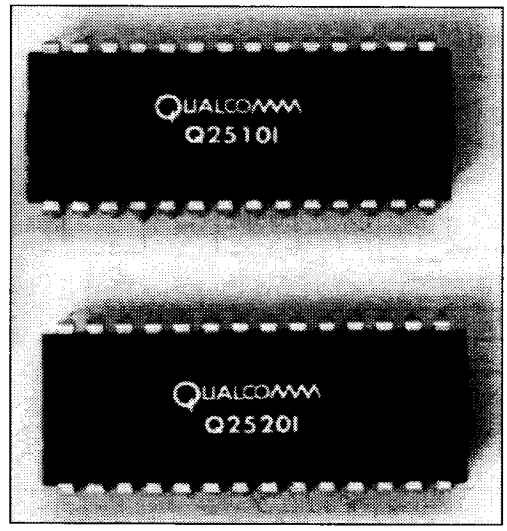
- DDS Synthesizers
- Radar and Sonar Systems
- Programmable Frequency Synthesizers
- Baseband Transmitters and Receivers
- Frequency Hopping Radios

INTRODUCTION

The Q2510/Q2520 High Speed Digital-to-Analog Converters (DAC) are designed with Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain 10 or 12-bit linearity without trimming. The Q2510/Q2520 DACs are ideal for use with the QUALCOMM family of DDS synthesizers where high resolution, good spectral purity, and fast switching times are required.

GENERAL DESCRIPTION

As shown in the functional block diagram for the Q2510 (Figure 1) the design is based on five main subsections: the Decoders and Drivers, the Edge Triggered Data Register, the Current Switch Network, the Control Amplifier and the Internal Voltage Reference.



The Q2510 and Q2520 Digital-to-Analog Converters (DAC) (The 28-pin PDIP Packages are shown)

The Q2520 also has five main subsections: the Decoders and Drivers, the Transparent Latches, the Current Switch Network, the Control Amplifier and the Internal Voltage Reference. The functional block diagram for the Q2520 (Figure 2) shows these.

DIGITAL INPUTS/TIMING

On the Q2510/Q2520 DACs, a TTL translator is added at each input to allow for simple interfacing to QUALCOMM DDSs. In the Decoder/Driver section , the four Most Significant Bits (MSBs — D6-D9 on Q2510 and D8-D11 on Q2520) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the clock signal and the six Least Significant Bits (LSBs) on the Q2510 (Latch Enable and eight LSBs on the Q2520). This delay minimizes data skew, and data setup and hold times at the register inputs on the Q2510 and the latch inputs on the Q2520. This is important when operating the latches in the transparent mode with the Q2520. Without the delay, skew caused by the decoding circuits would degrade glitch impulse.

Refer to Figures 3 & 4 for Pinout Diagrams and Tables 1 & 2 for Pin Descriptions of the Q2510/Q2520 DACs.

The Q2520 latches operate in their

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Figure 1. Q2510 Functional Block Diagram

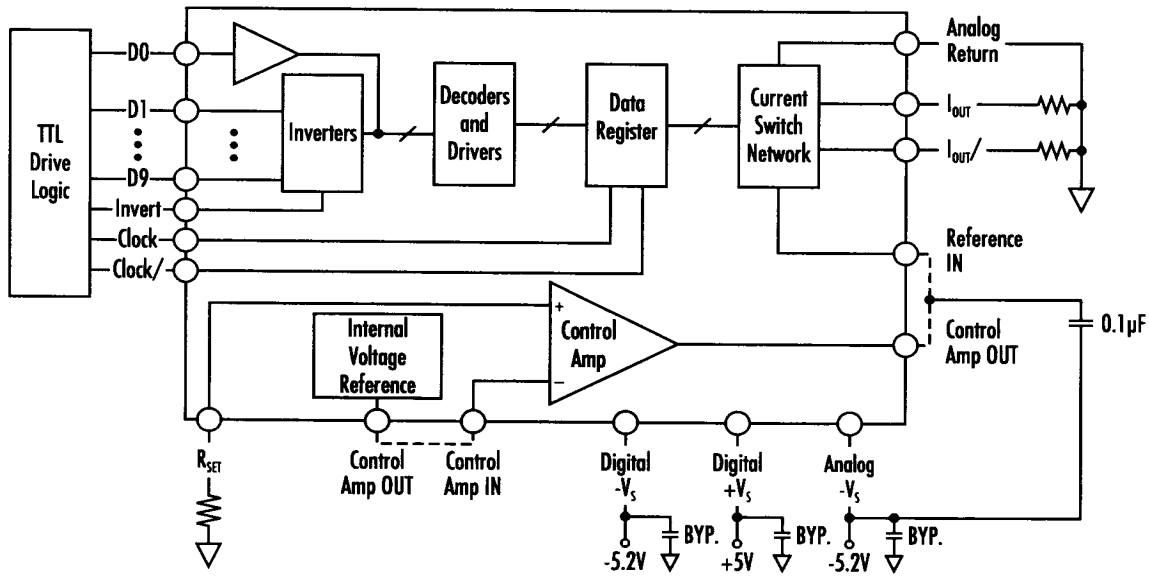
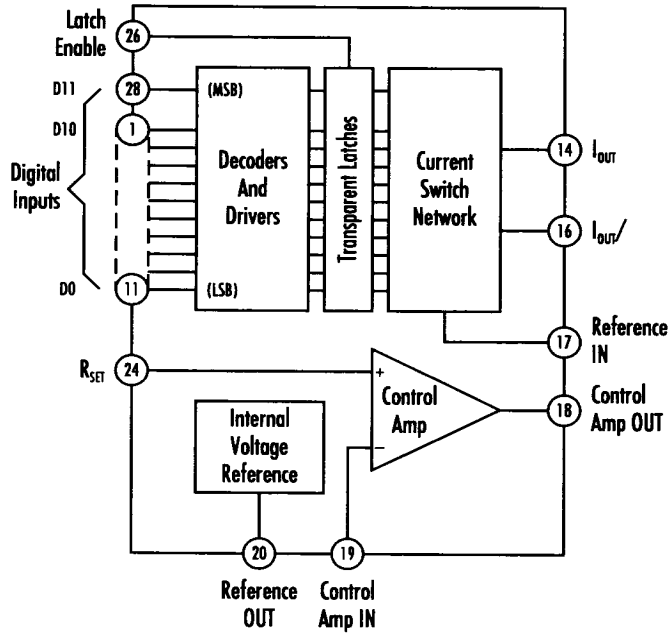


Figure 2. Q2520 Functional Block Diagram



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transparent mode when Latch Enable (Pin 26) is at logic level "0". The latches should be used to synchronize data to the current switches by applying a narrow Latch Enable pulse with proper data setup and hold times as shown in the Q2520 Timing Diagram (Figure 6). An external latch at each data input, clocked out of phase with the Latch Enable, operates the Q2520 in a master slave (edge-triggered) mode. This is the optimum way to operate the DAC because data is always stable at the DAC input. An external latch eases timing constraints when using the converter.

Although the Q2510/Q2520 DACs are designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the DAC. Digital feedthrough can be reduced by forming a low-pass filter using a (130Ω) series resistor in series with the capacitance of each digital input; this rolls off the slew rate of the digital inputs.

REFERENCES

As shown in the Q2510/Q2520 functional block diagrams (Figures 1&2), the internal band-gap reference, control amplifier, and reference input are pinned out for maximum user flexibility.

Figures 9 and 10 show the suggested DAC interconnect schematics for the Q2510 and the Q2520. The 0.1μF ceramic capacitor from Reference IN to $-V_S$ improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET}. The full-scale output current is determined by Control Amp IN and R_{SET} according to the following equation for Q2510:

$$I_{out}\,(FS) = (\text{Control Amp IN}/R_{SET}) \times 32$$

The equation for Q2520 is:

$$I_{out}\,(FS) = (\text{Control Amp IN}/R_{SET}) \times 128$$

The internal reference is nominally -1.25 V with a tolerance of ±8% and typical drift over temperature of 100 ppm/°C for Q2510. The internal reference is nominally -1.18 V with a tolerance of ±3.5% and typical drift over temperature of 50 ppm/°C for Q2520. If greater accuracy or better temperature stability is required, an external reference can be utilized.

Two modes of multiplying operation are possible with the Q2510/Q2520. Signals with small signal bandwidths up to 1 MHz for Q2510 and 300kHz for Q2520 and input swings from - 0.6V to -1.2V can be applied to the Control Amp input as shown in Figure 7. Because the control amplifier is internally compensated, the 0.1 μF capacitor at Reference IN can be reduced to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

The Reference IN pin can also be driven directly for wider bandwidth multiplying operation.

The analog signal for this mode of operation must have a signal swing in the range of -3.3 V to -4.25 V for Q2510 and -3.75 V to -4.25 V for Q2520. This can be implemented by capacitively coupling into Reference IN a signal with a dc bias as shown in Figure 8. Reference IN can also be driven with a low impedance op amp whose signal swing is limited to the stated range.

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Figure 3. Q2510 Pinout Diagram

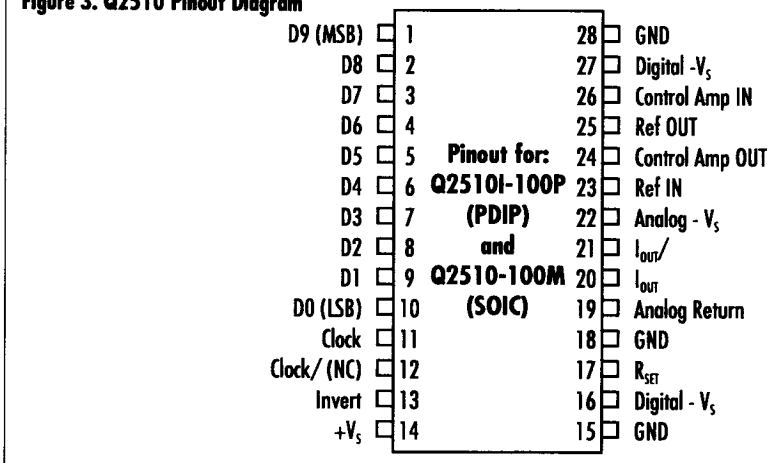

Table 1. Q2510 Pin Descriptions

Pin #	Name	Function
1	D9 (MSB)	Most Significant Bit (MSB) of digital word. TTL Compatible.
2 thru 9	D8-D1	Eight of Ten digital input bits. TTL Compatible.
10	D0 (LSB)	Least Significant Bit (LSB) of digital input word. Input Coding vs. Current Output Input Code D9-D0 / I_{OUT} (mA) / I_{OUT}/ (mA) 1111111111 / -20.48 / 0 0000000000 / 0 / -20.48
11	Clock	Edge-triggered latch enable signal for on-board registers. TTL compatible. Register loads data on rising edge of Clock signal.
12	Clock/(NC)	Not Connected.
13	Invert	Normally connected to logic LOW; inverters are transparent in this mode. Logic HIGH inverts the 9 LSB's (D8-D0) when the MSB is LOW.
14	+ V_S	+5VDC.
15	GND	Converter ground return.
16	Digital - V_S	-5.2 VDC.
17	R_{SET}	Connection for external resistance reference; nominally 1,960 Ω. Full-scale current out = 32 x (Control Amp IN/R_{SET}) when using internal amplifier. DAC load is virtual ground.
18	GND	Converter ground return.
19	Analog Return	Analog current return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground.)
20	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1". With external load resistor output voltage = I_{OUT} x ($R_{LOAD} \| R_{INTERNAL}$). $R_{INTERNAL}$ is nominally 210 Ω.
21	I_{OUT}/	Complementary analog current output; zero-scale output occurs with digital inputs at all "0".
22	Analog - V_S	Negative analog supply; -5.2VDC.
23	Ref IN	Normally connected to Control Amp OUT (Pin 24). Direct line to DAC current source network. Voltage changes (noise) at this point have a direct effect on the full-scale output current of DAC. Full-scale current output = 32 x (Control Amp IN/R_{SET}) when using internal amplifier. DAC load is Virtual ground.
24	Control Amp OUT	Normally connected to Ref IN (Pin 23). Output of internal control amplifier, which provides a reference for the current switch network.
25	Ref OUT	Normally connected to Control Amp IN (Pin 26). Internal voltage reference, nominally -1.25V.
26	Control Amp IN	Normally connected to Ref OUT (Pin 25) if not connected to external reference.
27	Digital - V_S	-5.2VDC.
28	GND	Converter ground return.

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Figure 4. Q2520 Pinout Diagram

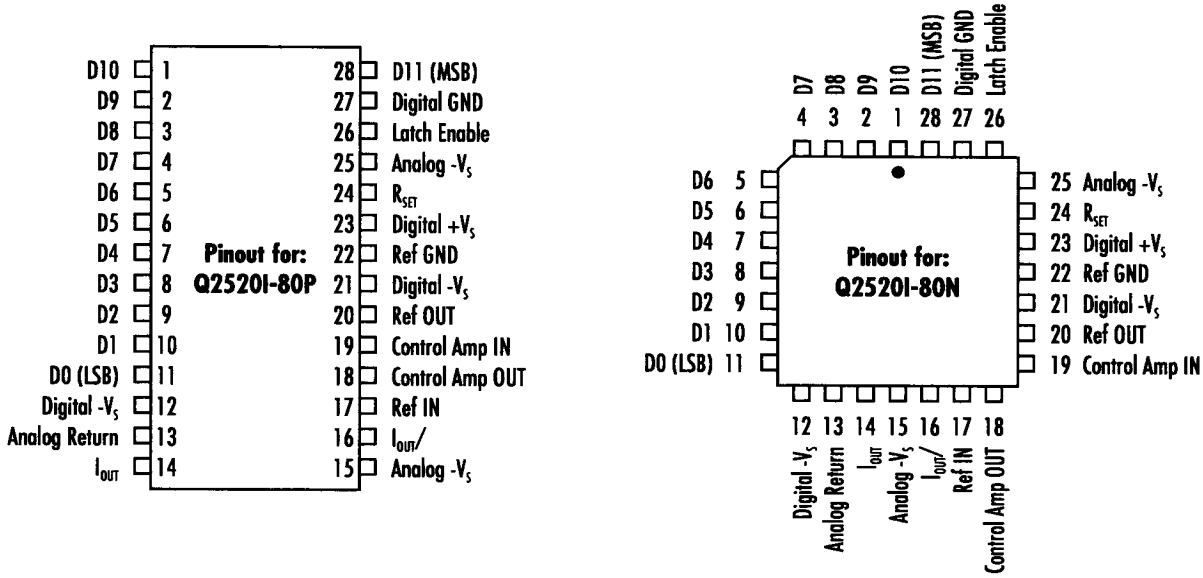

Table 2. Q2520 Pin Descriptions

Pin #	Name	Function
1 thru 10	D10-D1	Ten of Twelve digital input bits. TTL Compatible.
11	D0 (LSB)	Least Significant Bit (LSB) of digital input word. Input Coding vs. Current Output Input Code D11-D0 / I_{OUT} (mA) / I_{OUT}/ (mA) 111111111111 / -20.475 / 0 000000000000 / 0 / -20.475
12	Digital - V_S	One of two negative digital supply pins; nominally - 5.2 V.
13	Analog Return	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same Potential (nominally ground.)
14	I_{OUT}	Analog Current output; full-scale output occurs with digital inputs at all "1".
15	Analog - V_S	One of two negative analog supply pins; nominally - 5.2 V.
16	I_{OUT}/	Complementary analog current output; zero scale output occurs with digital inputs at all "0".
17	Ref IN	Normally connected to Control Amp OUT (Pin 18). Direct line to DAC current source network. Voltage changes at this point have a direct effect on the full-scale output value of unit. Full-scale current output = 128 (Reference Voltage/R_{SET}) when using internal amplifier.
18	Control Amp OUT	Normally Connected to Ref IN (Pin 17). Output of internal control amplifier, which provides a temperature-compensated drive level to the current switch network.
19	Control Amp IN	Normally connected to Ref OUT (Pin 20) if not connected to external reference.
20	Ref OUT	Normally connected to Control Amp IN (Pin 19). Internal voltage reference, nominally -1.18 V.
21	Digital -V_S	One of two negative digital supply pins; nominally - 5.2V.
22	Ref GND	Ground return for the internal voltage reference and amplifier.
23	Digital +V_S	Posotive digital supply pin nominally +5V.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier. Nominally - 7.5 kΩ.
25	Analog -V_S	One of two negative analog supply pins; nominally - 5.2 V.
26	Latch Enable	Transparent Latch control line. Register is transparent when Latch Enable is LOW.
27	Digital GND	Digital Ground Return.
28	D11 (MSB)	Most Significant Bit (MSB) of digital input word.

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Figure 5. Q2510 Timing Diagram

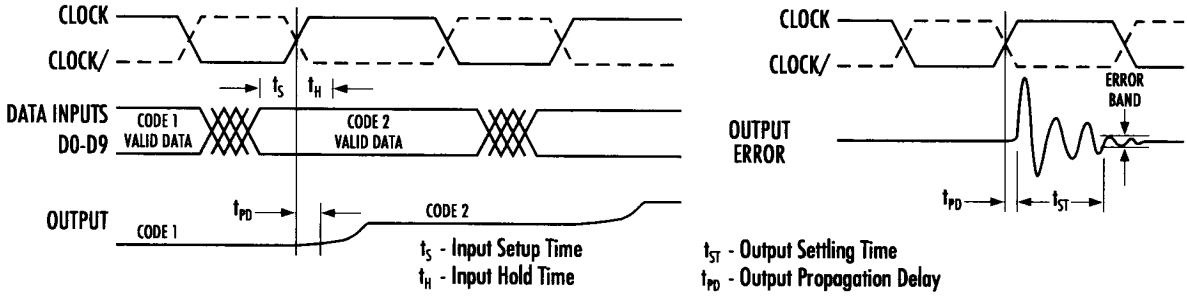


Figure 6. Q2520 Timing Diagram

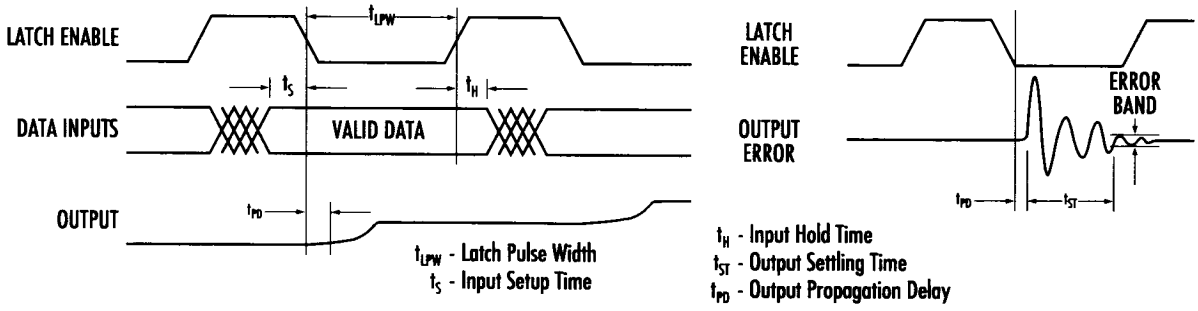


Figure 7. Low Frequency Multiplying Circuit

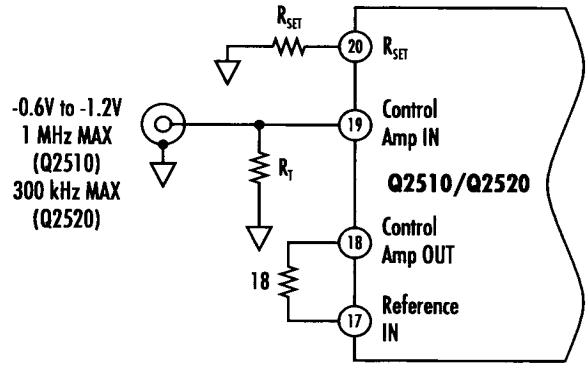
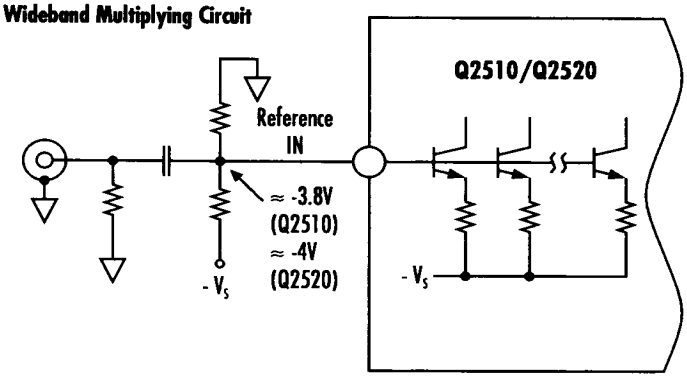


Figure 8. Wideband Multiplying Circuit



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DAC OUTPUTS

The Switch Network provides complementary current outputs I_{OUT} and I_{OUT}/. These current outputs are based on statistical current source matching which provides 10-bit and 12-bit linearity without trim. Current is steered to either I_{OUT} or I_{OUT}/ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in Figures 9 & 10. Both I_{OUT} and I_{OUT}/ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

An operational amplifier can also be used to perform the I-to-V conversion of the DAC output.

Figure 9. Typical Device Interconnect Schematic for Q2510

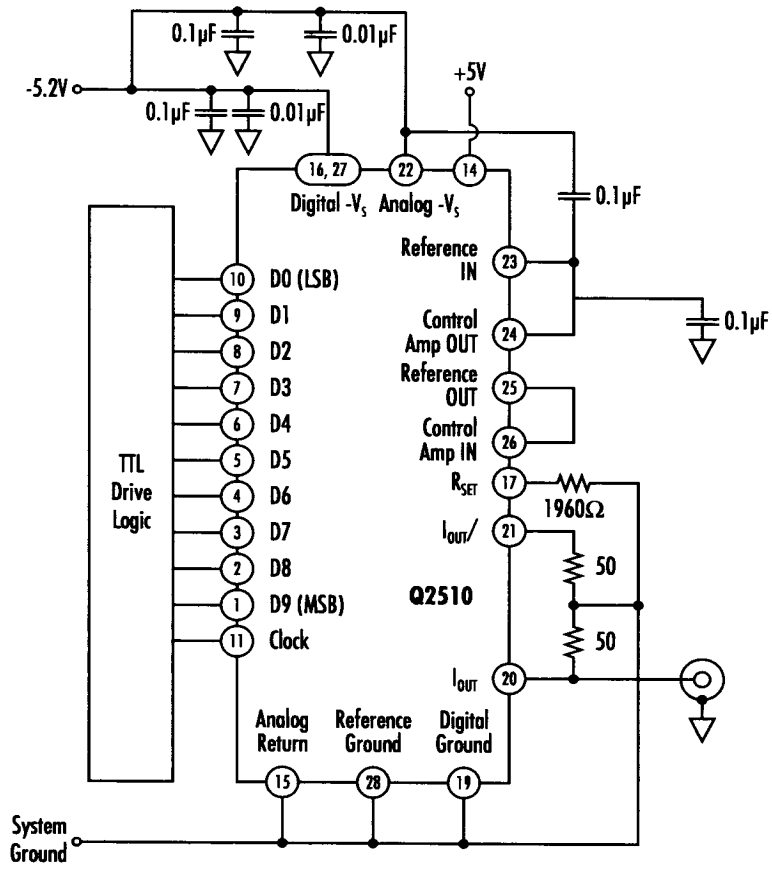

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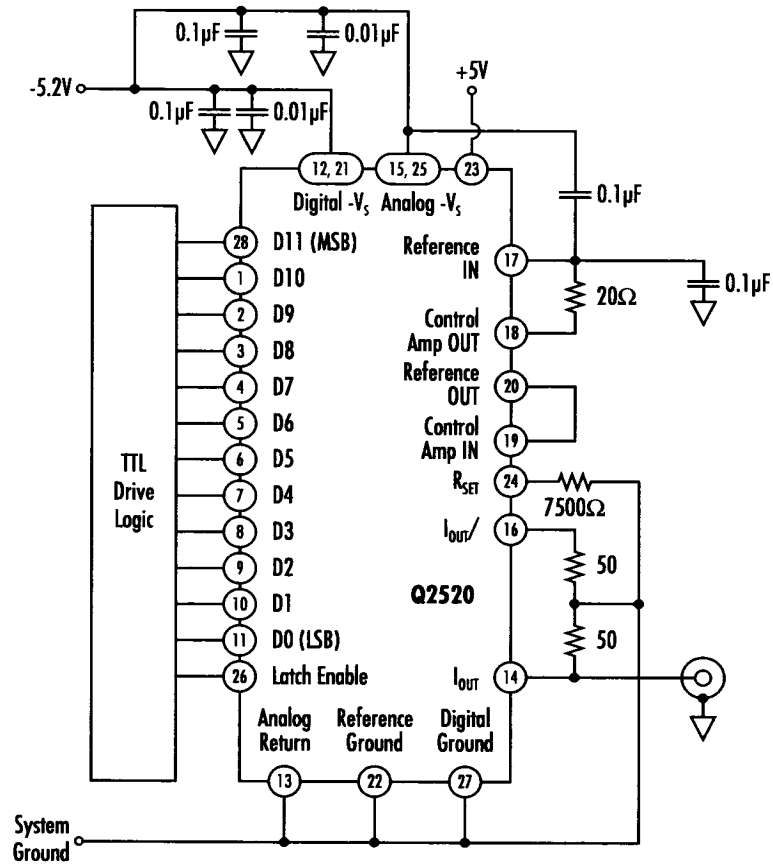
Figure 10. Typical Device Interconnect Schematic for Q2520



POWER AND GROUNDING

Maintaining low noise on power supplies and ground is critical for obtaining optimum results with the Q2510 and Q2520. DACs are most often used in circuits which are predominantly digital. To preserve 10-bit and12-bit performance, especially at conversion speeds at the DACs maximum frequency, special precautions are necessary for power supplies and grounding.

Ideally, the DAC should have a separate analog ground plane. All ground pins of the DAC, as well as reference and analog output components, should be tied directly to this analog ground plane. The DAC's ground plane should be connected to the system ground plane at a single point.

Ferrite beads such as the Stackpole 57-1392 or Amodon FB-43B-101, along with high frequency, low-inductance decoupling capacitors, should be used for the supply connections to isolate digital switching currents from the DAC supply pins. Separate isolation networks for the digital and analog supply connections will further reduce supply noise coupling to the output.

Molded socket assemblies should be avoided even when prototyping circuits with the DACs. When the DAC cannot be directly soldered into the board, individual pin sockets such as AMP #6-330808-0 (knock-out-end), or #60330808-3 (open end) should be used. These have much less effect on inter-lead capacitance than do molded assemblies.

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TECHNICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	$+V_S$		+6	V
Negative Supply Voltage	$-V_S$		-7	V
Voltage Differential Between Digital and Analog Ground			0.5	V
Digital Input Voltages for Q2510	D0-D9, Clock, Clock/	-0.5	V_S	V
Digital Input Voltages for Q2520	D0-D11, Latch Enable	-0.5	$+V_S$	V
Internal Reference Output Current			500	µA
Control Amplifier Input Voltage Range		0	-4	V
Control Amplifier Output Current		-2.5	+2.5	mA
Reference Input Voltage Range	V_{REF}	-3.7	$-V_S$	V
Analog Output Current			30	mA
Operating Temperature Range		-25	+85	°C
Maximum Junction Temperature[2]			+150	°C
Lead Temperature (Soldering, 10 sec)			+300	°C
Storage Temperature Range		-65	+150	°C

NOTES:

1. Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
2. Typical thermal impedances with parts soldered in place:
Q2510I-100P and Q2520I-80P — 28-pin PDIP: Θ_{JA} = 37°C/W, Θ_{JC} = 10°C/W;
Q2520I-80P — 28-pin PLCC: Θ_{JA} = 44°C/W, Θ_{JC} = 14°C/W
Q2510I-100M — 28-pin SOIC: Θ_{JA} = 46°C/W, Θ_{JC} = 10°C/W

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Table 4. Q2510 Specifications

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
Resolution			10		Bits
DC Accuracy					
Differential Nonlinearity	+25°C			1.0	LSB
Integral Nonlinearity ("Best Fit" Straight Line)	+25°C			1.5	LSB
Initial Offset Error					
Zero-Scale Offset Error	Full		20.0	75.0	µA
Full-Scale Gain Error[1]	Full			15	%
Offset Drift Coefficient	+25°C		0.04		µA/°C
Reference/Control Amp					
Internal Reference Voltage	Full	-1.15		-1.24	V
Internal Reference Voltage Drift	Full		100		ppm/°C
Internal Reference Output Current	Full	-50		+500	µA
Amplifier Input Impedance	+25°C		50		kΩ
Amplifier Bandwidth	+25°C		1		MHz
Reference Input[2]					
Reference Input Impedance	+25°C		4.6		kΩ
Reference Multiplying Bandwidth[3]	+25°C		75		MHz
Dynamic Performance					
Full-Scale Output Current[2,4]	+25°C		20.48		mA
Output Compliance Range	+25°C	-1.5		+3	V
Output Resistance	+25°C		210		Ω
Output Capacitance	+25°C		6		pF
Output Update Rate	+25°C		100		MSPS
Output Voltage Settling Time to ½ LSB(t_{ST})[5]	+25°C		4.5		ns
Output Propogation Delay (t_{PD})[6]	+25°C		4.5		ns
Glitch Impulse[7]	+25°C		1.5		pV_S
Output Rise Time[8]	+25°C		675		ns
Output Fall Time[8]	+25°C		470		ns
Digital Inputs					
Logic "1" Voltage	Full	2.0			V
Logic "0" Voltage	Full			0.8	V
Logic "1" Current	Full			400	µA
Logic "0" Current	Full			700	µA
Input Capacitance	Full		3		pF
Input Setup Time (t_S)[9]	Full	0.8	-0.3		ns
Input Hold Time (t_H)[10]	Full	2.0	1.2		ns
Clock Pulse Width (LOW)	+25°C	1.0	0.85		ns
Clock Pulse Width (HIGH)	+25°C	1.0	0.85		ns
Power Supplies[11]					
Positive Supply Current (+5.0V)	Full		14	30	mA
Negative Supply Current (-5.2V)	Full		218	290	mA
Nominal Power Dissipation	+25°C		1.2		W
Power Supply Rejection Radio (PSRR)[12]	+25°C		50	100	µA/V

NOTES:

1. Measured as error in ratio of full-scale current to current through R_{SET} (640 µA nominal); ratio is nominally 132. DAC Load is virtual ground.
2. Full-scale variations among devices are higher when driving REFERENCE INPUT directly.
3. Frequency at which a 3dB change to DAC output is observed. R_L = 50Ω and 100mV modulation at midscale.
4. Based on I_{FS} = 32 (V_{REF}/R_{SET}) when using internal amplifier.
5. Measured as voltage settling at midscale transition to ±0.%; R_L = 50Ω.
6. Measured as the time between the 50% point of the rising edge of CLOCK to ½ LSB change in output signal.
7. Peak glitch impulse is measured as the largest area under a single positive or negative transient.
8. Measured with R_L = 50Ω.
9. Data must remain stable for specified time prior to rising edge of CLOCK signal.
10. Data must remain stable for specified time after rising edge of CLOCK signal.
11. Supply voltages should remain stable within ±5% for normal operation.
12. Measured at ±5% of $+V_S$ and $-V_S$ using external reference.

Specifications subject to change without notice.

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Table 5. Q2520 Specifications

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
Resolution			12		Bits
DC Accuracy					
Differential Nonlinearity	+25°C	-1.25	1.0	2.0	LSB
Integral Nonlinearity ("Best Fit" Straight Line)	+25°C	-1.5	1.0	2.0	LSB
Initial Offset Error					
Zero-Scale Offset Error	Full		0.5	5.0	µA
Full-Scale Gain Error[1]	Full		1.0	8.0	%
Offset Drift Coefficient	+25°C		0.01		µA/°C
Reference/Control Amp					
Internal Reference Voltage	Full	-1.12		-1.24	V
Internal Reference Voltage Drift	Full		50		ppm/°C
Internal Reference Output Current	Full	-50		+500	µA
Amplifier Input Impedance	+25°C		50		kΩ
Amplifier Bandwidth	+25°C		300		kHz
Reference Input[2]					
Reference Input Impedance	+25°C		3		kΩ
Reference Multiplying Bandwidth[3]	+25°C		40		MHz
Dynamic Performance					
Full-Scale Output Current[4]	+25°C		20.48		mA
Output Compliance Range	+25°C	-1.2		+2	V
Output Resistance	+25°C	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C		15		pF
Output Update Rate[5]	+25°C	80	100		MSPS
Output Settling Time(t_{ST})[6]	+25°C		27		ns
Output Propogation Delay (t_{PD})[7]	+25°C		7		ns
Glitch Impulse[8]	+25°C		28		pV_S
Output Rise Time[9]	+25°C		2		ns
Output Fall Time[9]	+25°C		2		ns
Digital Inputs					
Logic "1" Voltage	Full	2.0			V
Logic "0" Voltage	Full			0.8	V
Logic "1" Current	Full			20	µA
Logic "0" Current	Full			600	µA
Input Capacitance	+25°C		3		pF
Input Setup Time (t_S)[10]	Full	0.8	-0.3		ns
Input Hold Time (t_H)[11]	Full	2.0	1.2		ns
Latch Pulse Width (t_{LPW}) (LOW) (Transparent)	Full	2.8	1.7		ns
Power Supplies[12]					
Positive Supply Current (+5.0V)	Full		6	14	mA
Negative Supply Current (-5.2V)	Full		145	188	mA
Nominal Power Dissipation	+25°C		784		mW
Power Supply Rejection Radio (PSRR)[13]	+25°C		30	100	µA/V

NOTES:

1. Measured as error in ratio of full-scale current to current through R_{SET} (160 µA nominal); ratio is nominally 128.
2. Full-scale variations among devices are higher when driving REFERENCE INPUT directly.
3. Frequency at which the gain is flat ±0.5 dB; R_L = 50Ω; 50% modulation at midscale.
4. Based on I_{FS} = 128 (V_{REF}/R_{SET}) when using internal amplifier.
5. Data registered into DAC accurately at this rate; does not imply settling to 12-bit accuracy.
6. Measured as voltage settling at midscale transition to ±0.024%; R_L = 50Ω.
7. Measured as the time between the 50% point of the falling edge of LATCH ENABLE and the point where the output signal has left a 1 LSB error band around its previous value.
8. Peak glitch impulse is measured as the largest area under a single positive or negative transient.
9. Measured with R_L = 50Ω and DAC operating in latched mode.
10. Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.
11. Data must remain stable for specified time after rising edge of LATCH ENABLE signal.
12. Supply voltages should remain stable within ±5% for normal operation.
13. Measured at ±5% of $+V_S$ and $-V_S$ using external reference.

Specifications subject to change without notice.

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APPLICATION INFORMATION

A recommended application circuit is shown in Figure 11. The schematic shows the interface connections between the 85 MHz Q2230 Direct Digital Synthesizer and the Q2510/Q2520 DACs. The Q2230 DDS produces the digital sine anplitude values by digitally integrating the frequency at a higher clock rate and translating the resulting phase to a sinusoided waveform via an algorithmic lookup table. The DDS sine amplitude values are converted to analog format using the DAC. The DAC is usually followed by a Low Pass Filter (LPF) to filter out the image response.

Since sampling theory states that at least two samples per cycle are required to reconstruct an output waveform, the maximum DDS fundamental frequency is (SYS CLK)/2. In general, the maximum output frequency is somewhat less than this to permit filtering of the image response.

Figure 11. Q2510/Q2520 DAC and Q2230 DDS Synthesizer Interface Schematic

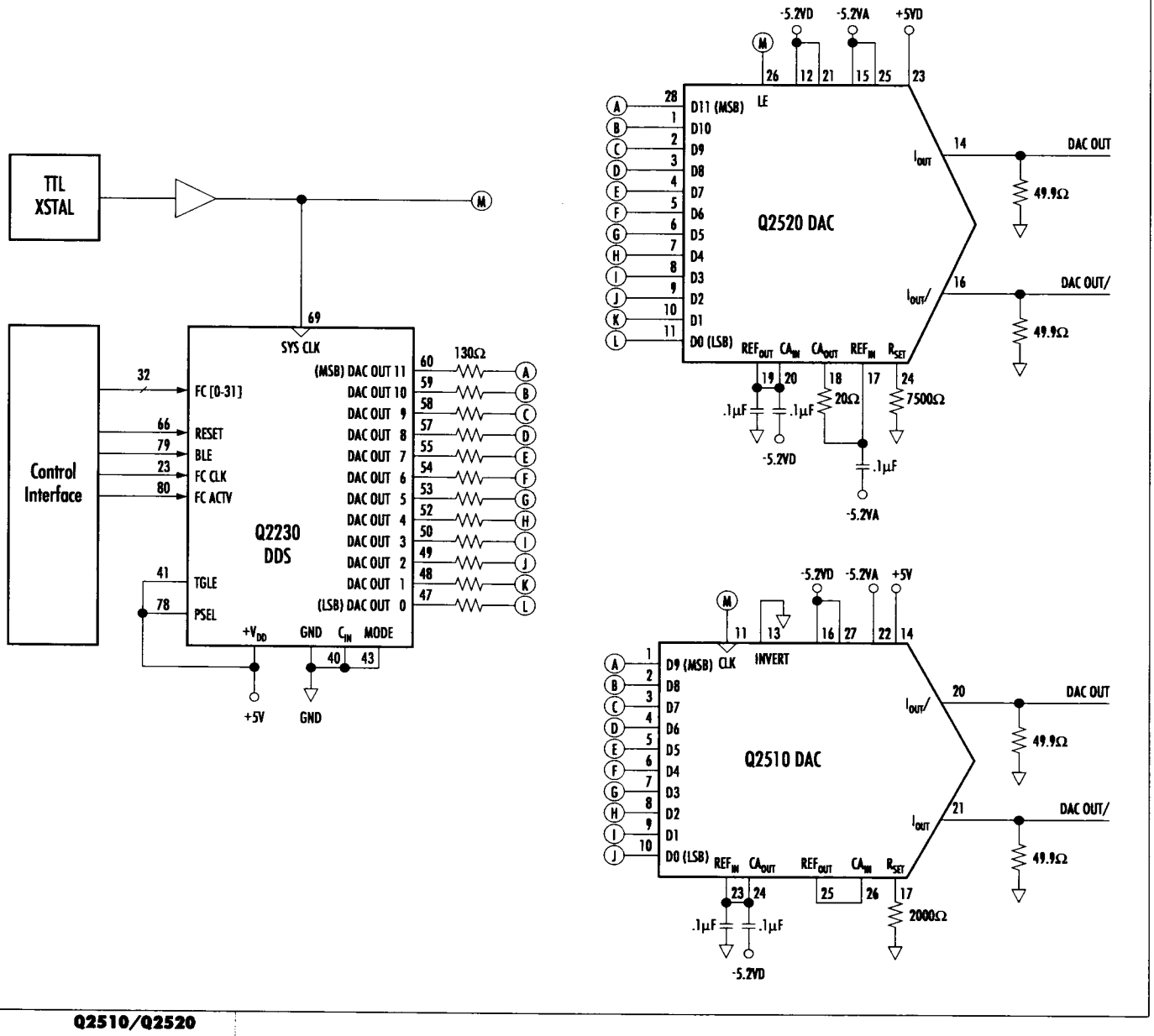

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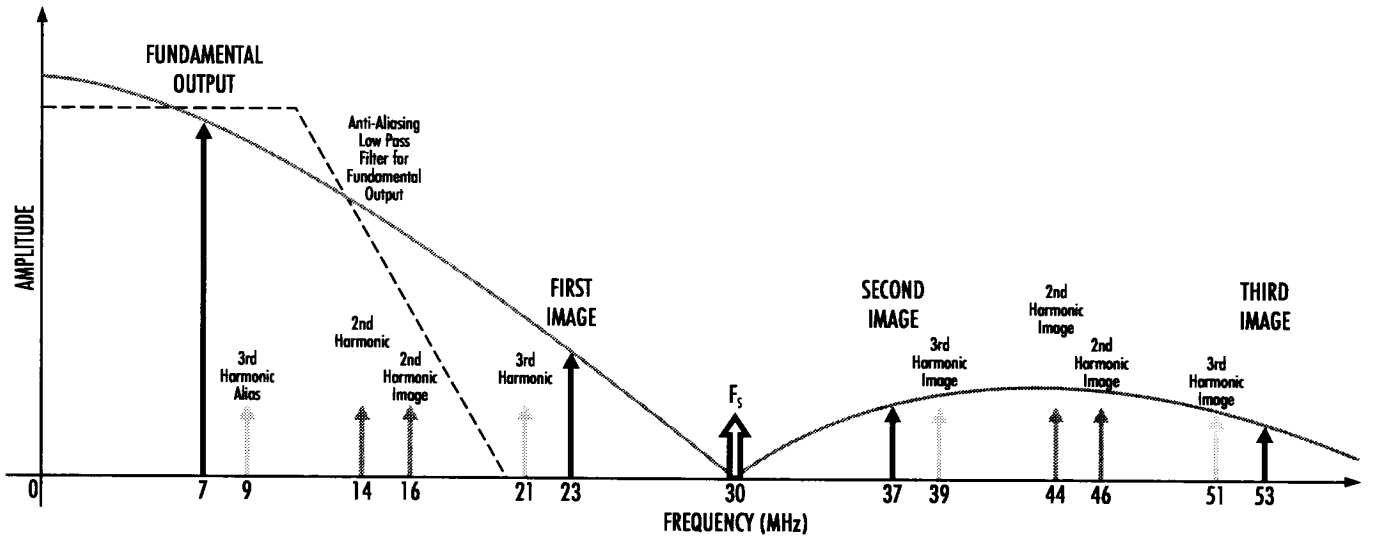
Figure 12 shows a typical frequency spectrum output of a DDS synthesizer after it has been converted to the analog domain by the DAC. The figure shows a fundamental frequency output at 7 MHz using a SYS CLK of 30 MHz. The DDS produces image responses as (N * (SYS CLK) ± F_{OUT}) where N = 1, 2, 3... which must be filtered using a LPF or Band Pass Filter (BPF). Note that when $F_{OUT} \geq$ (SYS CLK)/2 the first image is not filterable from the fundamental. Also, note that harmonics of the fundamental also produce aliases that fall into the desired pass band. Harmonic and Harmonic Alias Spurious usually determine the worst-case spurious performance of a DDS Synthesizer.

Figure 12. DDS Output Showing Effect of DAC Non-Linearities



DAC/DDS SYNTHESIZER OUTPUT PERFORMANCE

Figures 13 and 14 show Output Spectral plots that were measured on the application circuit depicted in Figure 11. Each figure includes six plots for each DAC (Figure 13 - the Q2510 and Figure 14 - the Q2520). These plots show the output spurious performance of this DDS/DAC topology at various SYS CLK and output frequencies.

A LPF was not used in these measurements in order to clearly show the alias due to the fundamental. The image is usually filtered with a LPF.

If the designer needs the DDS Synthesizer to generate a narrow frequency range, then a Band Pass Filter (BPF) can replace the LPF for improved spurious rejection

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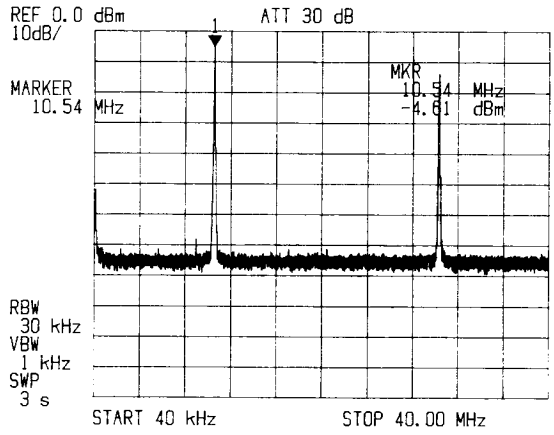
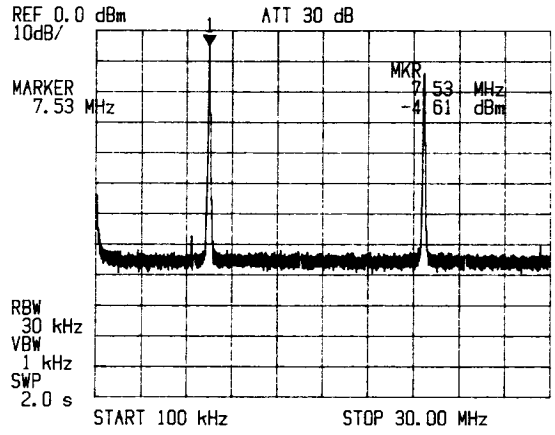
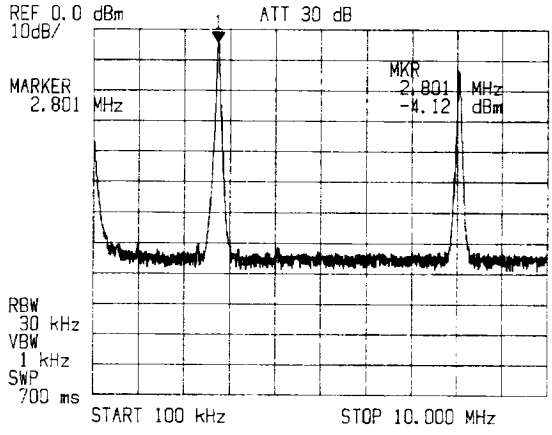
Figure 13. Q2510 Sample Plots



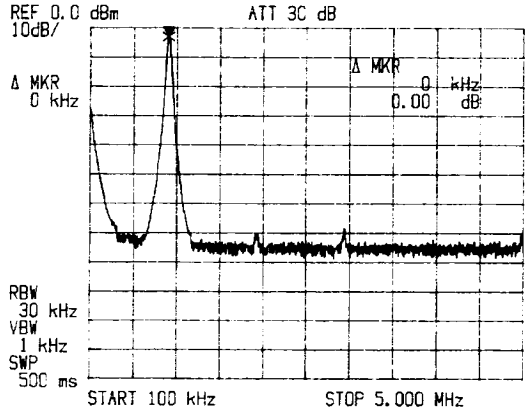
Using Q2510 DAC and Q2230 DDS, F_{CLK} = 40 MHz, F_{OUT} = 10.54 MHz



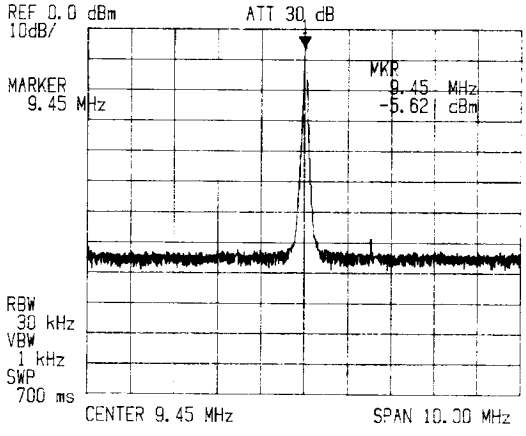
Using Q2510 DAC and Q2230 DDS, F_{CLK} = 30 MHz, F_{OUT} = 7.53 MHz



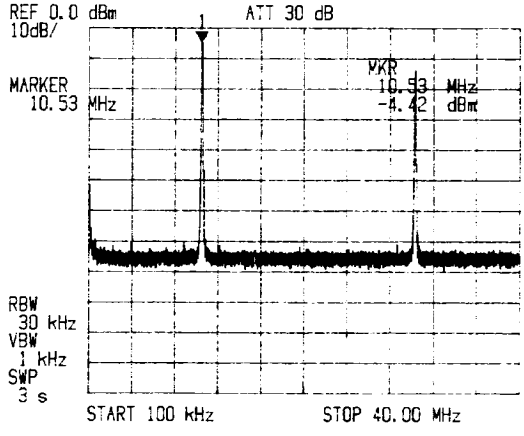
Using Q2510 DAC and Q2230 DDS, F_{CLK} = 10 MHz, F_{OUT} = 2.8 MHz



Using Q2510 DAC and Q2230 DDS, F_{CLK} = 20 MHz, F_{OUT} = 1 MHz



Using Q2510 DAC and Q2230 DDS, F_{CLK} = 30 MHz, F_{OUT} = 9.45 MHz



Using Q2510 DAC and Q2230 DDS, F_{CLK} = 40 MHz, F_{OUT} = 10.53 MHz

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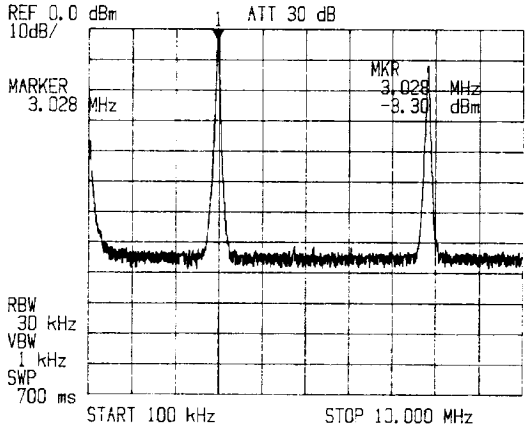
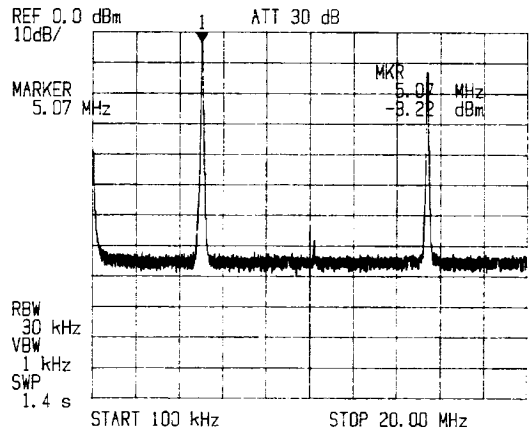
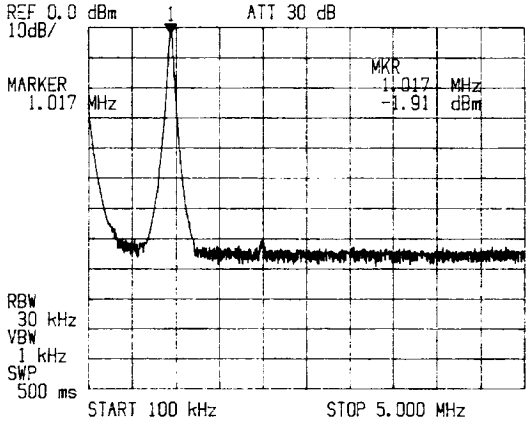
Figure 14. Q2520 Sample Plots



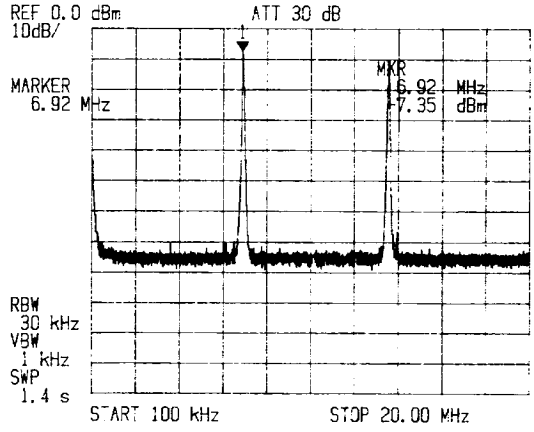
Using Q2520 DAC and Q2230 DDS, F_{CLK} = 10 MHz, F_{OUT} = 3.028 MHz



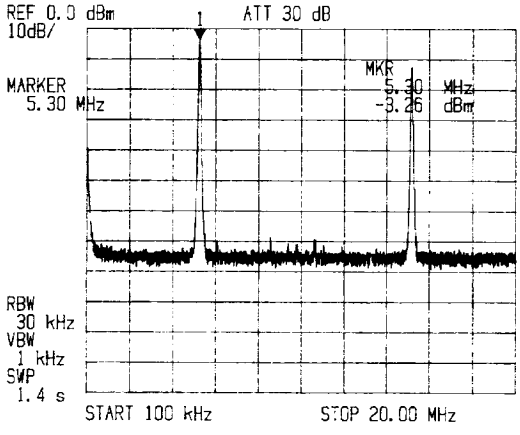
Using Q2520 DAC and Q2230 DDS, F_{CLK} = 20 MHz, F_{OUT} = 5 MHz



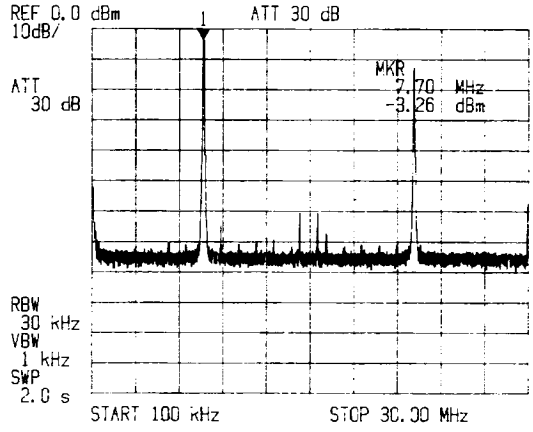
Using Q2520 DAC and Q2230 DDS, F_{CLK} = 20 MHz, F_{OUT} = 1 MHz



Using Q2520 DAC and Q2230 DDS, F_{CLK} = 20 MHz, F_{OUT} = 6.9 MHz



Using Q2520 DAC and Q2230 DDS, F_{CLK} = 20 MHz, F_{OUT} = 5.3 MHz



Using Q2520 DAC and Q2230 DDS, F_{CLK} = 30 MHz, F_{OUT} = 7.7 MHz

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PACKAGING

The Q2510 comes in two different package styles. The Q2510I-100P is a 28-pin Plastic DIP (PDIP) (See Figure 15.) and the Q2510I-100M is a 28-pin Small Outline Integrated Circuit (SOIC) (see Figure 16).

The Q2520 comes in two different package styles as well. The Q2520I-80P is also a 28-pin PDIP package (also, see Figure 15). The Q2520I-80N is a 28-pin Plastic Leaded Chip Carrier (PLCC) package (see Figure 17).

Figure 15. Q2510I-100P and Q2520I-80P - 28-pin PDIP Package Outline [Dimensions are in Inches (mm)]

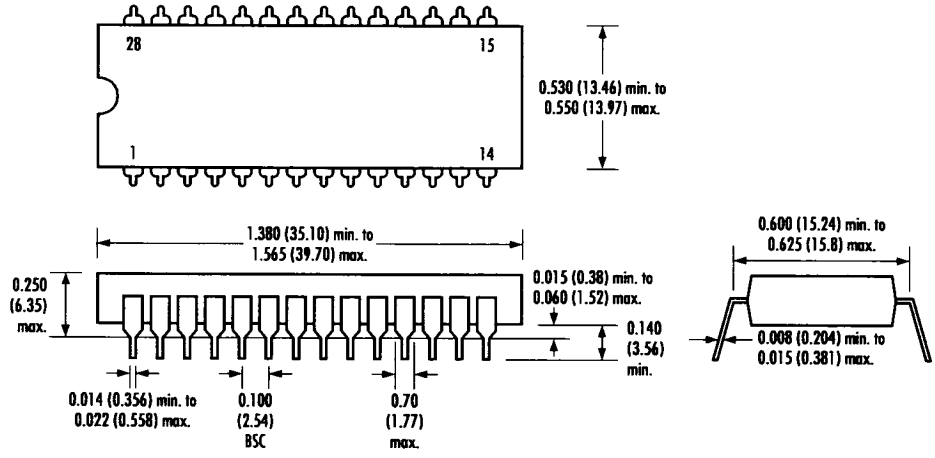

Figure 16. Q2520I-80N - 28-pin PLCC Package Outline [Dimensions are in Inches (mm)]

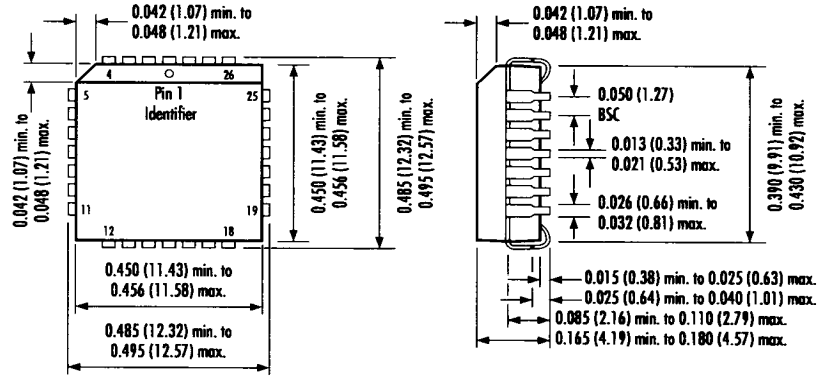

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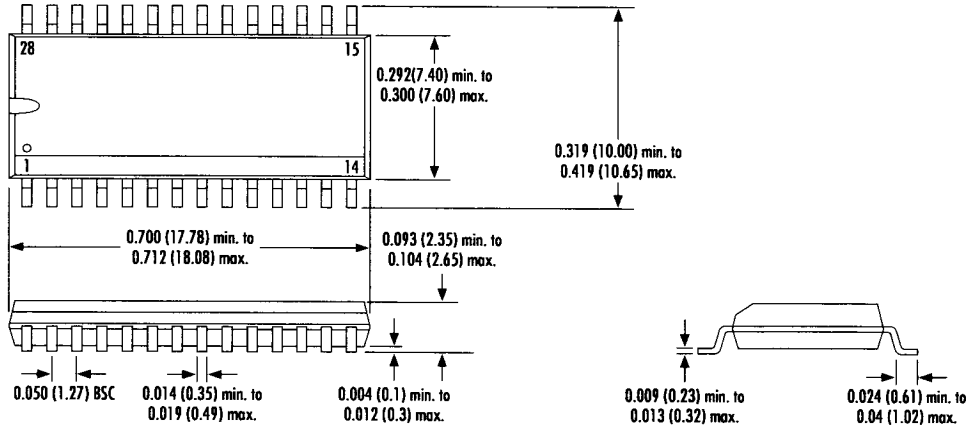
Figure 17. Q2510I-100N - 28-pin SOIC Package Outline [Dimensions are in Inches (mm)]



ORDERING INFORMATION

Table 6. Q2510/Q2520 Ordering Information

PRODUCT NUMBER	BIT RESOLUTION	PACKAGE	TEMPERATURE RANGE	NOTES
Q2510I-100P	10-bits	28-pin PDIP	-25°C to +85°C	1
Q2510I-100M	10-bits	28-pin SOIC	-25°C to +85°C	1
Q2520I-80P	12-bits	28-pin PDIP	-25°C to +85°C	1
Q2520I-80N	12-bits	28-pin PLCC	-25°C to +85°C	1

NOTE:
1. For more information, refer to "Technical Specifications", Page 11.

RELATED QUALCOMM LITERATURE

AN2334-3 "Direct Digital Synthesis, 21 Questions & Answers for RF Engineers," QUALCOMM, 1992.

AN2334-4 "Hybrid PLL/DDS Frequency Synthesizers," QUALCOMM, 1990.

Q2234 Dual Direct Digital Synthesizer Technical Data Sheet

Q2220 Direct Digital Synthesizer Technical Data Sheet

Q2230 Direct Digital Synthesizer Technical Data Sheet

GLOSSARY

BPF	Band Pass Filter
DAC	Digital-to-Analog Converter
DDS	Direct Digital Synthesizer
FC	Frequency Control
F_G	Generated Frequency
F_S	System Clock Frequency
HOP CLK	Hop Clock
LPF	Low Pass Filter
LSB	Least Significant Bit
MSB	Most Significant Bit
PDIP	Plastic DIP
PLCC	Plastic Leaded Chip Carrier
SOIC	Small Outline Integrated Circuit

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