



**N-Channel Enhancement-Mode
Vertical DMOS FETs**

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	V _{GS(th)} (max)	Order Number / Package
				TO-92
20V	1.3Ω	0.5A	1.0V	TN0702N3

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Features

- Low threshold — 1.0 volt max
- On resistance guaranteed at V_{GS} = 2, 3, and 5 volts
- High input impedance
- Low input capacitance —130pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

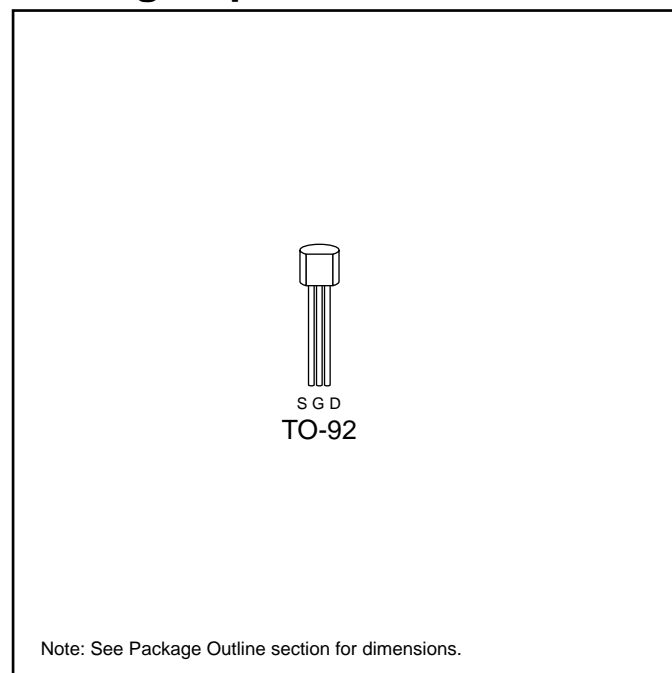
*Distance of 1.6 mm from case for 10 seconds maximum.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @ T _C = 25°C	θ _{jc} °C/W	θ _{ja} °C/W	I _{DR} *	I _{DRM}
TO-92	0.6A	1.0A	1W	125	170	0.6A	1.0A

* I_D (continuous) is limited by max rated T_J.

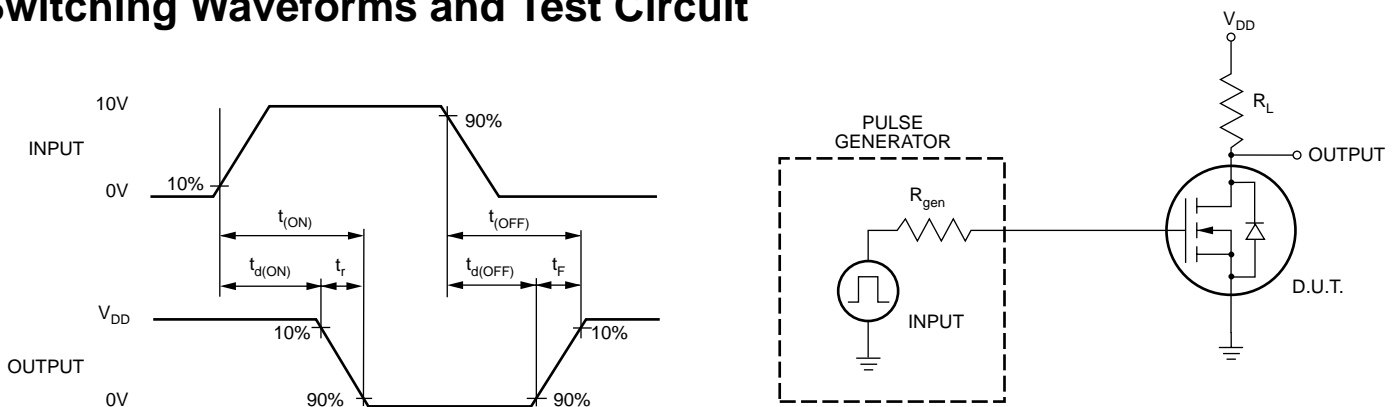
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	20			V	V _{GS} = 0V, I _D = 1mA
V _{GS(th)}	Gate Threshold Voltage	0.5	0.8	1.0	V	V _{GS} = V _{DS} , I _D = 1.0mA
ΔV _{GS(th)}	Change in V _{GS(th)} with Temperature			-4.0	mV/°C	V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate Body Leakage			100	nA	V _{GS} = ±20V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current			100	nA	V _{DS} = 20V, V _{GS} = 0V
				100	μA	V _{DS} = 0.8 Max Rating, V _{GS} = 0V, T _A = 125°C
I _{D(ON)}	ON-State Drain Current	0.5	1.0		A	V _{GS} = V _{DS} = 5V
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance		4.0	5.0	Ω	V _{GS} = 2V, I _D = 50mA
			1.9	2.5		V _{GS} = 3V, I _D = 200mA
			1.0	1.3		V _{GS} = 5V, I _D = 500mA
ΔR _{DS(ON)}	Change in R _{DS(ON)} with Temperature			0.75	%/°C	V _{GS} = 5V, I _D = 500mA
G _{FS}	Forward Transconductance	100	500		mΩ	V _{DS} = 5V, I _D = 500mA
C _{ISS}	Input Capacitance		130	200	pF	V _{GS} = 0V, V _{DS} = 20V, f = 1MHz
C _{OSS}	Common Source Output Capacitance		70	125		
C _{RSS}	Reverse Transfer Capacitance		30	60		
t _{d(ON)}	Turn-ON Delay Time			20	ns	V _{DD} = 20V, I _D = 0.5A, R _{GEN} = 25Ω
t _r	Rise Time			20		
t _{d(OFF)}	Turn-OFF Delay Time			30		
t _f	Fall Time			20		
V _{SD}	Diode Forward Voltage Drop			1.0	V	V _{GS} = 0V, I _{SD} = 0.5A

Notes:

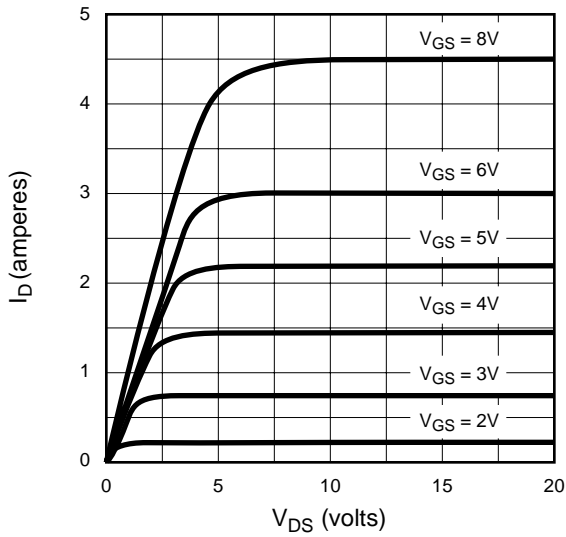
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

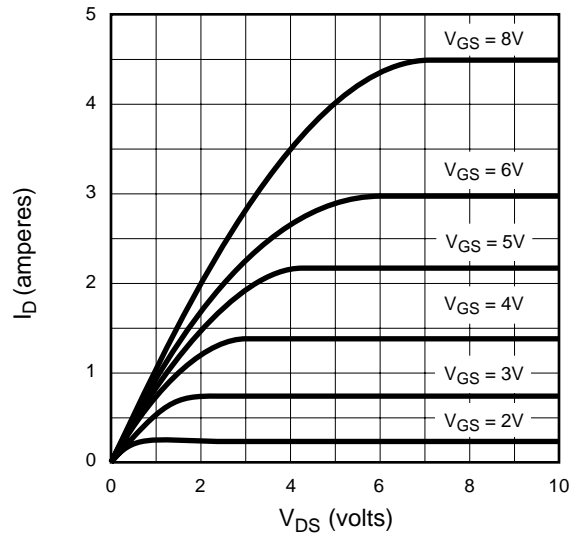


Typical Performance Curves

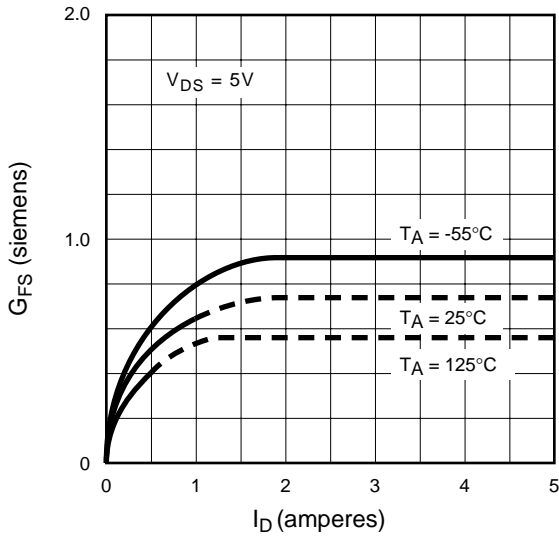
Output Characteristics



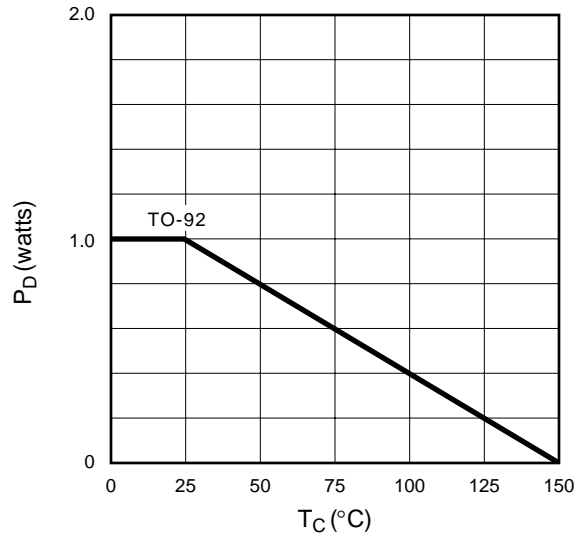
Saturation Characteristics



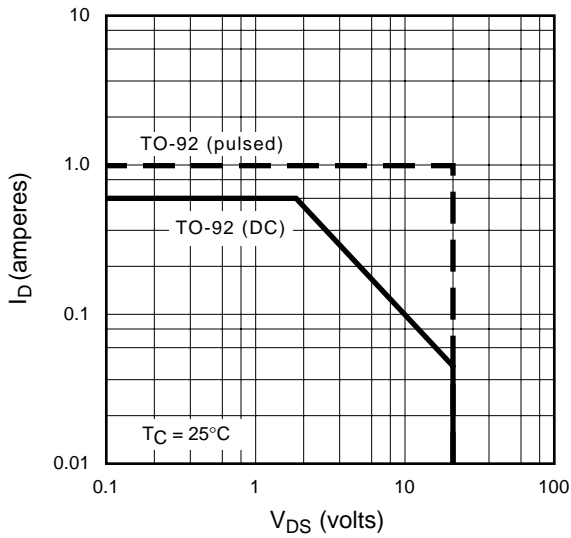
Transconductance vs. Drain Current



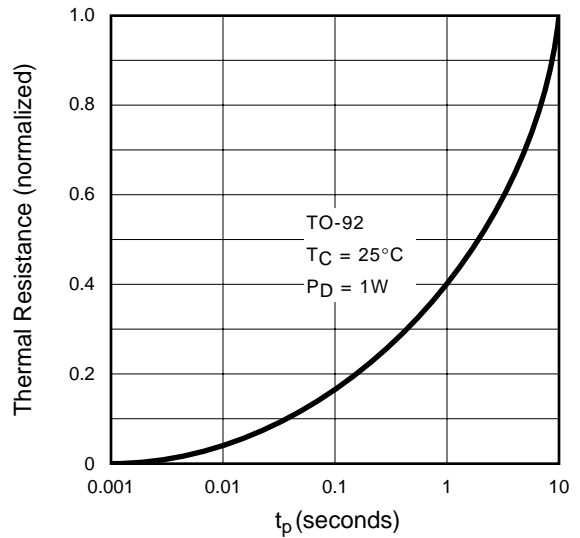
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

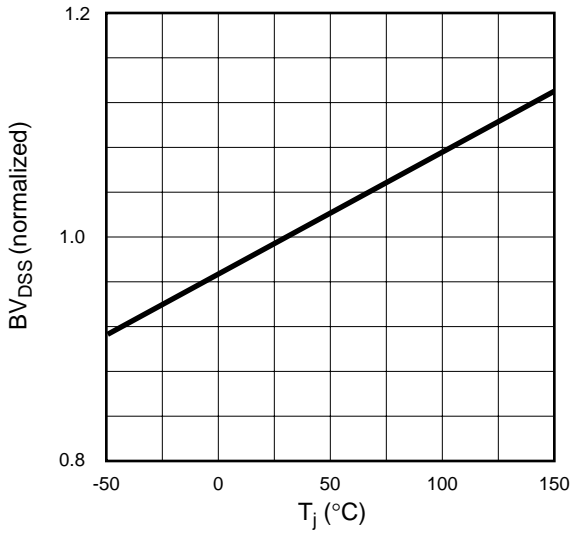


Thermal Response Characteristics

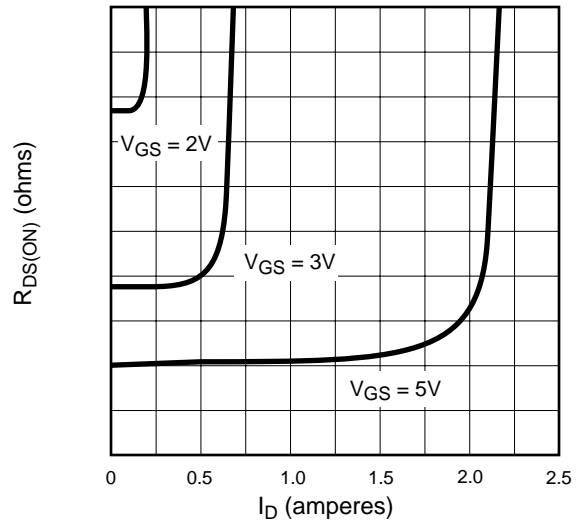


Typical Performance Curves

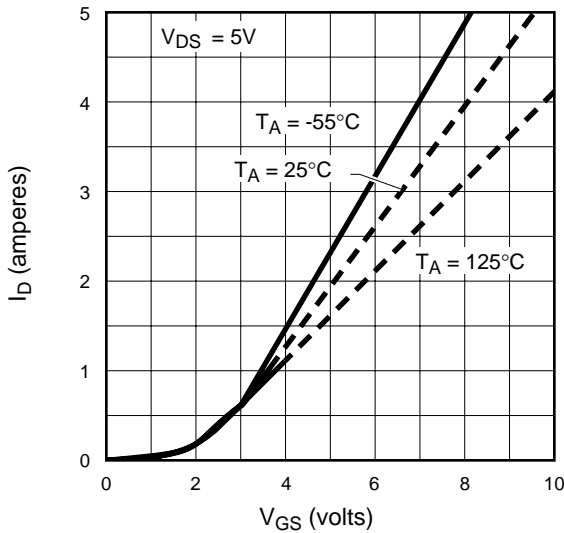
BV_{DSS} Variation with Temperature



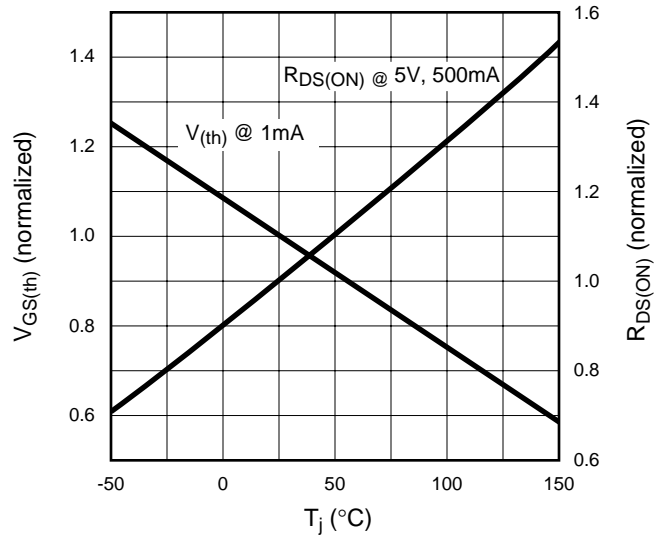
On-Resistance vs. Drain Current



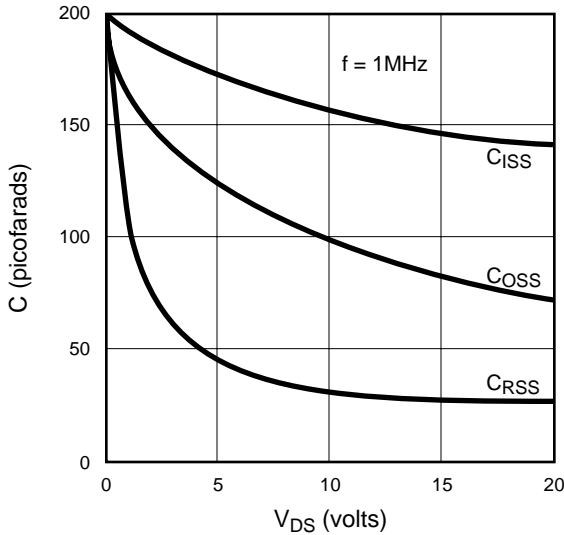
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

