

**4 Channel Simultaneous Track and Hold**

**Features**

- Completely Self-Contained  
Four Track-and-Hold Amplifiers  
On-Chip Hold Capacitors  
Two Output Buffer Amplifiers  
Microprocessor Interface
- 800ns Acquisition Time to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset Including Hold  
Pedestal: 2.8mV
- Low Droop Rate: 0.001uV/us
- Auto-Calibration Insures Accuracy Over  
Time and Temperature
- Low Power Dissipation: 250mW

**General Description**

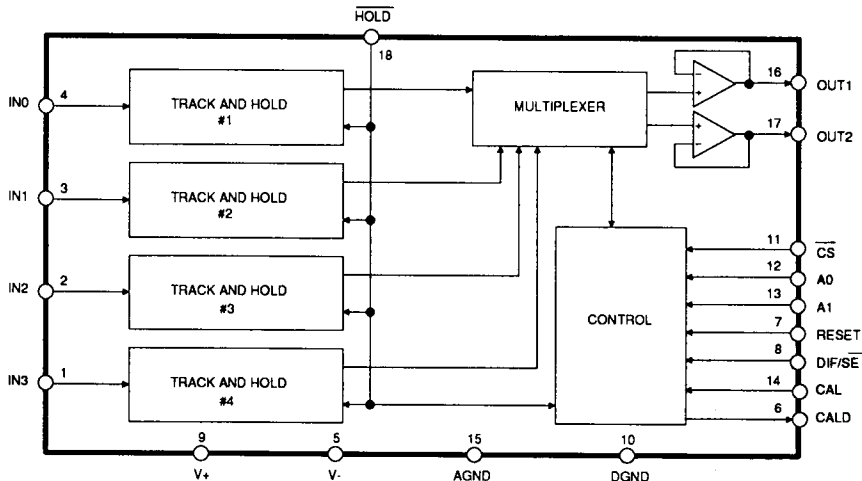
The CS31412 is a four-channel track and hold capable of processing four single-ended or two differential inputs with 12-bit linearity. It consists of four track-and-hold amplifiers, an analog multiplexer, two output buffers, and a microprocessor interface.

Controlled by a single  $\overline{\text{HOLD}}$  input, the four track-and-hold amplifiers can simultaneously hold their outputs with only 100ps of aperture jitter and later acquire their inputs within 800ns to 0.01%. On-chip hold capacitors limit droop to 0.001uV/us, and first order leakage compensation minimizes droop over temperature.

The CS31412 can be configured, controlled, and monitored through its microprocessor interface, or can be operated independently of intelligent control.

**ORDERING INFORMATION:**

Model	Acquisition Time	Temp. Range	Package
CS31412-KC2	2.0 $\mu\text{s}$	0 to 70°C	18-pin Ceramic SB DI
CS31412-KC1	1.0 $\mu\text{s}$	0 to 70°C	18-pin Ceramic SB DI
CS31412-BC1	1.0 $\mu\text{s}$	-40 to +85°C	18-pin Ceramic SB DI
CS31412-TC1	1.0 $\mu\text{s}$	-55 to +125°C	18-pin Ceramic SB DI



**ANALOG CHARACTERISTICS**

( $T_A = 25^\circ\text{C}$ ,  $V_+ = +5.0\text{V}$ ,  $V_- = -5.0\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , Analog Source Impedance =  $40\Omega$ , unless otherwise specified)

Parameter*	CS31412-K			CS31412-B			CS31412-T			Units	
	min	typ	max	min	typ	max	min	typ	max		
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			$^\circ\text{C}$	
<b>Accuracy</b>											
Total Offset (Note 1)	25 $^\circ\text{C}$	-2.8	$\pm 4.0$	-2.8	$\pm 4.0$	-2.8	$\pm 4.0$	mV			
	$T_{\min}$ to $T_{\max}$		$\pm 4.5$		$\pm 5.0$		$\pm 5.0$	mV			
Total Offset Matching	$T_{\min}$ to $T_{\max}$	0.25		0.25		0.25		mV			
	Channels 0-2	1.00		1.00		1.00		mV			
Channels 0-3											
Offset Drift (Note 2)	$T_{\min}$ to $T_{\max}$	$\pm 0.020$			$\pm 0.025$			$\pm 0.030$			$\text{mV}/^\circ\text{C}$
Tracking Offset		$\pm 55$			$\pm 55$			$\pm 55$			mV
Nonlinearity (Note 3)	25 $^\circ\text{C}$		$\pm 1.4$		$\pm 1.4$		$\pm 1.4$	mV			
	$T_{\min}$ to $T_{\max}$	$\pm 0.5$		$\pm 0.5$		$\pm 0.5$		mV			
Gain Error (Note 3)	25 $^\circ\text{C}$	$\pm 0.05$			$\pm 0.05$			$\pm 0.05$			% FS
	$T_{\min}$ to $T_{\max}$	$\pm 0.05$			$\pm 0.05$			$\pm 0.05$			% FS
<b>Dynamic Characteristics</b>											
Acquisition Time											
(6V step to 0.01%)	-1	0.8	1.0	0.8	1.0	0.8	1.0	us			
	-2	1.6	2.0					us			
(6V step to 0.1%)	-1	0.6		0.6		0.6		us			
	-2	1.2						us			
Track to Hold Settling to 0.01%		0.5	0.8	0.5	0.8	0.5	0.8	us			
Mux Output Settling Time											
(6V step to 0.01%)	-1	1.3	1.5	1.3	1.5	1.3	1.5	us			
	-2	1.8	2.5					us			
(6V step to 0.1%)	-1	1.0		1.0		1.0		us			
	-2	1.5						us			
Aperture Time		20		20		20		ns			
Aperture Time Matching (Note 4)		2		2		2		ns			
Aperture Jitter		100		100		100		ps			
Interchannel Aperture Offset		100		100		100		ps			
Droop Rate	25 $^\circ\text{C}$	$\pm 0.001$	$\pm 0.1$	$\pm 0.001$	$\pm 0.1$	$\pm 0.001$	$\pm 0.1$	$\mu\text{V}/\text{us}$			
	$T_{\min}$ to $T_{\max}$		$\pm 0.6$		$\pm 1.0$		$\pm 5.0$	$\mu\text{V}/\text{us}$			

- Notes:
1. Applies after calibration at any temperature within the specified temperature range.
  2. Applies over specified temperature range without recalibration since calibration at 25 $^\circ\text{C}$ .
  3. Applies over the input voltage range of -3.0V to +3.0V.
  4. Part to part.

\* Refer to *Error Definitions* at the end of this data sheet.

### ANALOG CHARACTERISTICS (Continued)

Parameter*	CS31412-K			CS31412-B			CS31412-T			Units
	min	typ	max	min	typ	max	min	typ	max	
<b>Analog Input</b>										
Large Signal Bandwidth (6V p-p Input)	2			2			2			MHz
Small Signal Gain Bandwidth (60mV p-p Input)	2.5			2.5			2.5			MHz
Output Slew Rate	10			10			10			V/us
Interchannel Isolation (Note 5)	90			90			90			dB
Input Impedance (dc)	100			100			100			MΩ
Input Capacitance	4			4			4			pF
Input Bias Current	100			100			100			pA
<b>Analog Output</b>										
Noise										
Track Mode (Note 6)	50			50			50			$\mu\text{V}_{\text{rms}}$
Hold Mode (Note 7)	33			33			33			$\mu\text{V}_{\text{rms}}$
Output Impedance at dc (Hold Mode) (Note 8)	0.1			0.1			0.1			Ω
<b>Power Supplies</b>										
Power Supply Currents										
Positive	25 45			25 45			25 45			mA
Negative	- 25 - 45			- 25 - 45			25 - 45			mA
Power Supply Rejection Ratio										
Positive (Note 9)	75			75			75			dB
Negative (Note 10)	60			60			60			dB

- Notes:
5. With a 100kHz input signal.
  6. Total noise from dc to 1MHz.
  7. Total noise from dc to 1MHz.
  8. Applies over the input voltage range of -3V to +3V.
  9. With 300mV p-p, 1kHz ripple applied to V+.
  10. With 300mV p-p, 1kHz ripple applied to V-.

Specifications are subject to change without notice.

**SWITCHING CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_+ = 5V \pm 10\%$ ;  $V_- = -5V \pm 10\%$ )

Parameter	Symbol	Min	Typ	Max	Units
A0, A1, DIF/SE, CAL to $\overline{CS}$ Setup Time	$t_{su}$	20	5	-	ns
$\overline{CS}$ to A0, A1, DIF/SE, CAL Hold Time	$t_h$	20	5	-	ns
$\overline{CS}$ Pulse Width	$t_{pw}$	100	50	-	ns
$\overline{CS}$ Low and CAL High to CALD High	$t_{cal}$	-	500	-	ms

**DIGITAL CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_+ = 5V \pm 10\%$ ;  $V_- = -5V \pm 10\%$ )

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	2.0	1.7	-	V
Low-Level Input Voltage	$V_{IL}$	-	1.6	0.8	V
High-Level Output Voltage (Note 11)	$V_{OH}$	$V_+ - 1.0V$	-	-	V
Low-Level Output Voltage $I_{out} = 1.6mA$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-	-	10	$\mu A$

 Note: 11.  $I_{out} = -100\mu A$ . This specification guarantees TTL compatibility ( $V_{OH} = 2.4V @ I_{out} = -40\mu A$ ).

**RECOMMENDED OPERATION CONDITIONS** ( $AGND, DGND = 0V$ , see note 12).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	$V_+$	4.5	5.0	5.5	V
Negative	$V_-$	-4.5	-5.0	-5.5	V
Analog Input Voltage:	$V_{IN}$	-3.0	-	3.0	V

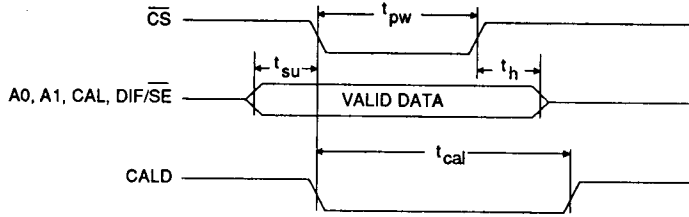
Note: 12. All voltages with respect to ground.

**ABSOLUTE MAXIMUM RATINGS** ( $AGND, DGND = 0V$ , All voltages with respect to ground)

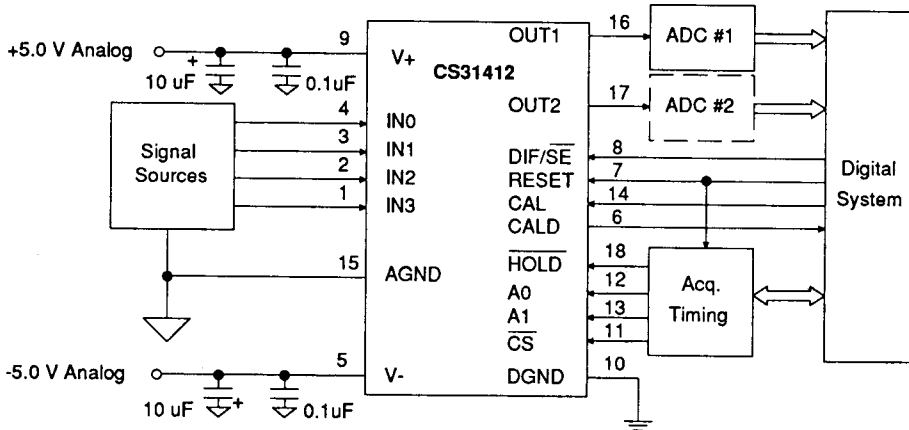
Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	$V_+$	- 0.3	6.0	V
Negative	$V_-$	0.3	- 6.0	V
Input Current, Any Pin Except Supplies (Note 13)	$I_{in}$	-	$\pm 10$	mA
Analog Input Voltage	$V_{INA}$	$V_- - 0.3$	$V_+ + 0.3$	V
Digital Input Voltage	$V_{IND}$	- 0.3	$V_+ + 0.3$	V
Ambient Operating Temperature	$T_A$	- 55	125	$^{\circ}C$
Storage Temperature	$T_{stg}$	- 65	150	$^{\circ}C$

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

 Note: 13. Transient currents of up to 100mA will not cause SCR latch-up. Maximum power supply pin current is  $\pm 100$  mA.



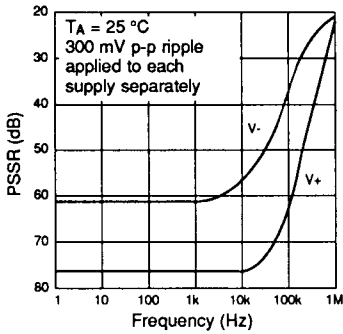
**Timing Diagram**



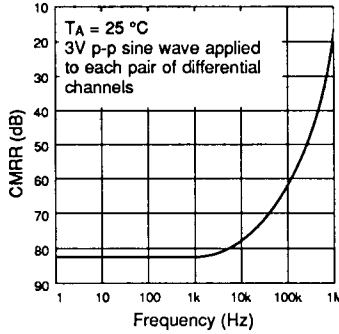
**System Connection Diagram**

**TYPICAL PERFORMANCE CHARACTERISTICS**

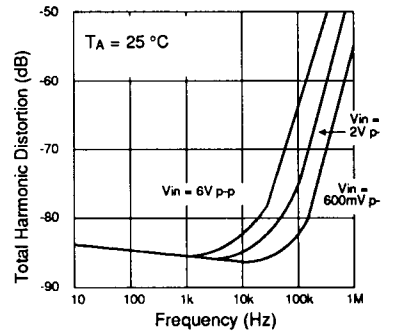
(V+ = +5.0V, V- = -5.0V)



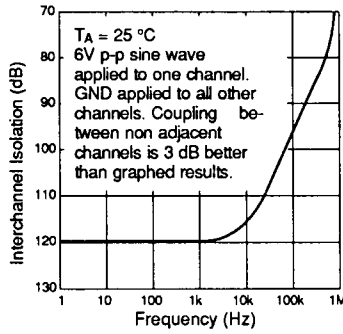
**PSRR vs. Frequency**



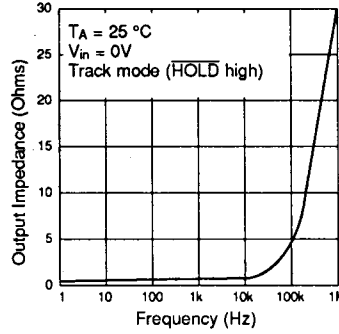
**Differential Mode CMRR vs. Frequency**



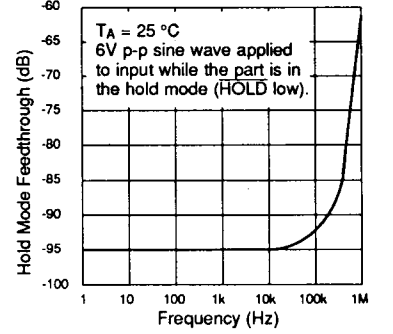
**Distortion vs. Frequency**



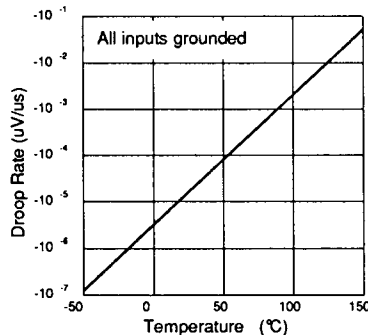
**Interchannel Isolation vs. Frequency**



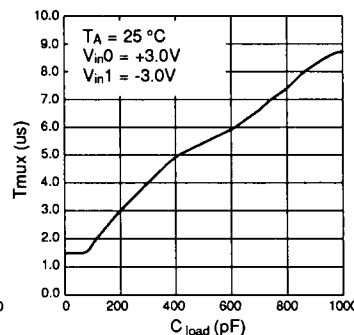
**Output Impedance vs. Frequency**



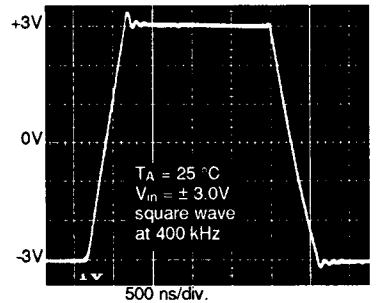
**Hold Mode Feedthrough vs. Frequency**



**Droop Rate vs. Temperature**



**Output MUX Settling Time vs. Load Capacitance**



**Full Scale Acquisition**

### GENERAL DESCRIPTION

The CS31412 consists of four track-and-hold amplifiers with on-chip hold capacitors, an analog multiplexer, and two output buffers. The CS31412 requires no external components or manual trims, and thus eliminates the task of error budgeting several components with complex (and often hidden) error sources.

The CS31412 can handle either four single-ended or two differential analog signals. The device is controlled through its on-board microprocessor interface, or it can be operated independently of intelligent control. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output for each channel.

#### Analog Multiplexer

The analog multiplexer takes the outputs of the four track-and-hold amplifiers and passes the selected outputs to the OUT1 and OUT2 pins. When DIF/SE is low, the multiplexer is configured as a four-to-one multiplexer and each amplifier is treated as a single-ended analog input referenced to AGND. When DIF/SE is high, the multiplexer is configured as dual two-to-one multiplexers and the track-and-hold amplifiers are treated as two groups of two amplifiers which al-

lows the CS31412 to process differential signals. This option can also be used to increase system throughput by using the CS31412 with two A/D converters (see System Throughput). Table 1 shows the multiplexer and buffer amplifier configurations as determined by the DIF/SE pin and the address pins, A0 and A1. In the differential mode, the A0 input should be tied low to avoid floating the output buffer amplifiers. In addition, the buffer amplifier at OUT2 in the single-ended mode does not float; its output remains within 50mV of AGND and must remain unconnected.

#### Calibration

The CS31412 features on-chip digital intelligence and measurement circuitry capable of calibrating all four input channels. For each channel, the device internally deselects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. In the calibration mode, the CS31412 uses an internal microcontroller and special nulling circuitry to reduce all errors at the OUT1 and OUT2 pins. Thus, all internal errors including dc offsets and dynamic errors due to charge injection (hold pedestal) are trimmed. The output of the CS31412 is only corrected for offset during the hold mode (HOLD low). During tracking, each channel may have up to  $\pm 55\text{mV}$  of offset.

The user must initiate a calibration to initially calibrate the device. This is achieved by bringing the CAL input high and CS low. Calibration can be similarly initiated during operation at any time thus insuring accuracy under any conditions. During the calibration cycle (which takes about 500 ms to complete) the CALD pin remains low. During this period, any load on OUT1 and OUT2 must remain constant; otherwise, errors could be introduced which might affect accuracy. If a new calibration is initiated before the current calibration is finished, the CS31412 will complete the current calibration before initiating the new one. CALD will go high when calibration is finished.

DIF/SE	A1	A0	OUT1	OUT2
0	0	0	IN0	0V*
0	0	1	IN1	0V*
0	1	0	IN2	0V*
0	1	1	IN3	0V*
1	0	0	IN0	IN1
1	0	1	N/A**	N/A**
1	1	0	IN2	IN3
1	1	1	N/A**	N/A**

\* AGND  $\pm 50\text{mV}$

\*\* Indeterminate Output: A0 should be tied low in differential mode

Table 1. Truth Table of MUX Configurations

The DIF/ $\overline{SE}$  input to the CS31412 must be in the correct state when initiating a calibration since the offsets of the analog output buffers are also calibrated. If the part is switched between the single ended and differential modes during operation, a new calibration must be initiated to guarantee that the Total Offset specification is met.

### Digital Interface

The CS31412 includes a digital interface designed for maximum flexibility. The digital inputs, A0, A1, CAL, and DIF/ $\overline{SE}$ , are internally gated with  $\overline{CS}$ . The input latches for the A0 and A1 inputs are level sensitive and latch on the rising edge of  $\overline{CS}$ . Any state changes on these pins while  $\overline{CS}$  is low appear at the output(s). In a microprocessor-controlled application, the  $\overline{CS}$  control input is usually derived from a decoded address as well as write and strobe signals off of the control bus (Figure 1a). Channel selection and calibration initiation thereby involve writing to the CS31412's address using data bits to control A0, A1, CAL, and DIF/ $\overline{SE}$ . For microprocessor-independent operation in single-ended mode,  $\overline{CS}$  is tied low and the digital inputs are controlled by externally-latched signals (Figure 1b).

The CS31412's CALD output can be used to generate an interrupt indicating the CS31412 has completed calibration. Alternatively, calibration

status can be polled in software by connecting CALD to the data bus via a 3-state buffer.

### Reset

The CS31412 must be reset after power up to ensure correct operation. The reset function is invoked by bringing the RESET pin high for at least 1  $\mu$ s. An RC network attached to the RESET pin will reset the part (See Figure 1b).

### System Throughput

Throughput of the CS31412 varies depending on the number of input signals used. System timing diagrams which enable the throughput of the CS31412 to be calculated are shown in Figure 2. Table 2 is a listing of throughput times for the number of input channels used. These times assume that no time is required for A/D conversion. When the part is used in the differential mode, throughput time will be equal to the two channel throughput time.

Since one of the four channels must be connected to the output buffer, the Track-to-Hold settling time ( $t_{th}$ ) is included in the first channel's settling time ( $t_1$ ). The address inputs A0, and A1 must be switched before the part is put in the hold mode ( $\overline{HOLD}$  low) so that the first channel's output is valid at time ( $t_1$ ). After the first output is settled,

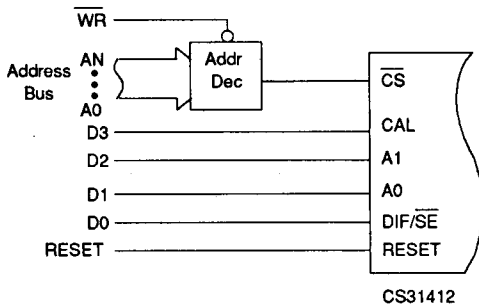


Figure 1a. CPU-Control

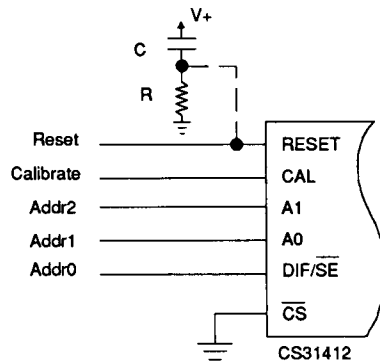


Figure 1b. CPU-Independent Control



the addresses can be used to mux each of the other three channels to the output.

When interfacing the CS31412 with an A/D converter which includes an integrated sample/hold, such as Crystal's CS501X series, additional reduction in throughput time can be obtained by pipelining settling times. As soon as the A/D has captured the output of the CS31412,  $\overline{\text{HOLD}}$  can be brought high and the CS31412 can acquire the new input signals and settle the first muxed channel while the A/D is converting. Likewise, output mux settling for all other other channels can be pipelined during conversion removing all of the CS31412's timing from the throughput equation. System throughput can therefore proceed at the ADC's maximum throughput. Using the CS31412 in the differential mode with two ADCs will reduce throughput time further because two channels can be converted simultaneously.

### Power Supplies and Input Connections

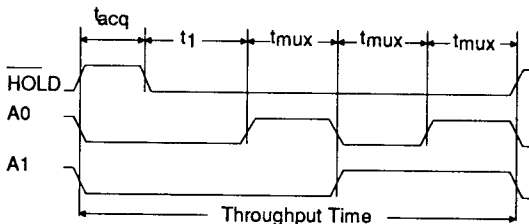
The CS31412 uses the analog ground voltage (AGND) only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on AGND relative to the system's analog ground plane will result in

Single Channel	Two Channels	Three Channels	Four Channels
2.70us	4.20us	5.71us	7.19us

**Table 2. Throughput Time**

offset errors. Therefore, the analog inputs should be referenced to the AGND pin which should be used as the entire system's analog ground. Decoupling should be performed between the V+, V- pins and AGND using 0.1uF ceramic capacitors. If significant low frequency noise is present on the supplies, 10uF tantalum capacitors are recommended in parallel with the 0.1uF capacitors. *The decoupling capacitors should be placed as close to the CS31412's power supply pins as possible.*

The signal source impedances which drive the four input channels of the CS31412 should be minimized as much as possible. Low source impedance reduces the sensitivity of the input pins to picking up capacitively-coupled energy from logic level transitions, such as  $\overline{\text{HOLD}}$  going low.

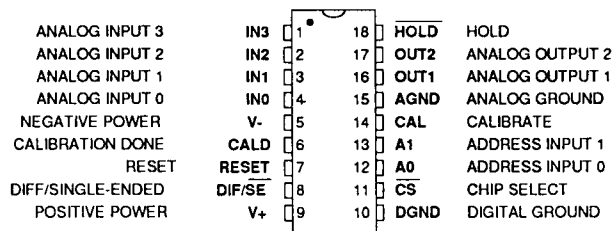


- $t_{acq}$ : Acquisition Time
- $t_{th}$ : Track to Hold Settling Time
- $t_{mux}$ : Mux Output Settling Time
- $t_1$ : First Channel Settling Time

$$t_1 = \sqrt{t_{th}^2 + t_{mux}^2}$$

**Figure 2. Four Channel Timing**

## PIN DESCRIPTIONS



### Power Supplies

#### V+ - Positive Power, PIN 9

Most positive supply voltage. Nominally +5 volts.

#### V- - Negative Power, PIN 5

Most negative supply voltage. Nominally -5 volts.

#### DGND - Digital Ground, PIN 10

Digital ground reference.

#### AGND - Analog Ground, PIN 15

Analog ground reference.

### Analog Inputs

#### IN0; IN1; IN2; IN3 - Analog Inputs 0;1;2;3, PINS 4,3,2,1

Analog inputs to the four track and hold amplifiers.

### Digital Inputs

#### CS - Chip Select, PIN 11

Enables the DIF/SE, A0, A1, and CAL digital inputs.

#### RESET - Reset, PIN 7

The CS31412 must be reset to ensure correct operation. Reset occurs when RESET is high.

**DIF/SE - Differential/Single-Ended Select, PIN 8**

Configures the output multiplexer in either a single-ended or differential mode. It is latched on the rising edge of  $\overline{CS}$ , but usually tied high or low. If set low, the four analog inputs are routed through OUT1. If set high, IN0 and IN1 are paired as one differential signal and IN2 and IN3 are paired as a second.

**A0; A1 - Address Input 0; Address Input 1, PINS 12, 13**

Select which amplifier or amplifier pair is output on the OUT1 and OUT2 pins. A0 should be held low when DIF/SE is high to avoid floating the outputs.

**CAL - Calibrate, PIN 14**

When taken high with  $\overline{CS}$  low, initiates a full internal calibration.

**HOLD - Hold, PIN 18**

A falling transition on this pin signals all four amplifiers to hold their inputs simultaneously. When brought high, the amplifiers acquire, and then track the input signal.

**Analog Outputs****OUT1; OUT2 - Analog Output 1; Analog Output 2, PINS 16, 17**

The buffered outputs from the multiplexer; OUT1 is always active and OUT2 is active only in the differential mode (DIF/SE high).

4

**Digital Outputs****CALD - Calibration Done, PIN 6**

Indicates calibration status. If CALD is high the device has finished calibration. If CALD is low the device is calibrating.

**ERROR DEFINITIONS**

**Total Offset** - The difference between the analog voltage applied to the analog input (A0, A1, A2, or A3) and the signal that appears at the appropriate output pin (OUT1 or OUT2) after the hold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

**Nonlinearity** - The deviation from a straight line on the plot of output vs input after offset error is accounted for. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

**Gain Error** - Calculated as the difference between the *Total Offsets* resulting from -3V and +3V dc input signals relative to a 6V input range. Units in percent of full scale.

**Acquisition Time** - The time required after the negation of the hold command ( $\overline{\text{HOLD}}$  high) for the track-and-hold amplifiers to reach their final values to within a specified error band ( $\pm 0.01\%$  or  $\pm 0.1\%$ ). Measured internally at the inputs to the multiplexer, it determines the minimum time allowed before reassertion of the hold command. Indicates nothing about the outputs as measured at OUT1 or OUT2. Units in microseconds.

**Track-to-Hold Settling** - The time required after the hold command is given for each track and hold to reach its final value to within a specified error band ( $\pm 0.01\%$ ). Includes switch delay (aperture) time but not multiplexer and output buffer settling. Units in microseconds.

**MUX Output Settling** - The time required after reconfiguring the multiplexer for the outputs at OUT1 and OUT2 to reach their final value to within a specified error band ( $\pm 0.01\%$  or  $\pm 0.1\%$ ). Measured from the falling edge of  $\overline{\text{CS}}$  with A0 and A1 valid. Units in microseconds.

**Aperture Time** - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

**Aperture Jitter** - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

**Interchannel Aperture Offset** - The range of variation in aperture time between the four track-and-hold amplifiers for a given hold command. A measure of simultaneity. Units in picoseconds.

**Droop Rate** - The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

**Large Signal Bandwidth** - The frequency at which the output amplitude while tracking a full scale 6Vp-p sine wave is 3dB below the input amplitude. Units in megahertz.

**Small Signal Gain Bandwidth** - The frequency at which the output amplitude while tracking a 60 mVp-p sine wave is 3dB below the input amplitude. Units in megahertz.

**Interchannel Isolation** - A measure of crosstalk between input channels while in the track mode. Units in decibels.