

# CS52015-1

## 1.5 A Adjustable Linear Regulator

The CS52015-1 linear regulator provides 1.5 A with an accuracy of  $\pm 1.0\%$ . The device uses two external resistors to set the output voltage within a 1.25 V to 5.5 V range.

The regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages less than 1.4 V at 1.5 A output current. Device protection includes overcurrent and thermal shutdown.

The CS52015-1 is pin compatible with the LT1086 family of linear regulators but has lower dropout voltage.

The regulator is available in TO-220, surface mount D<sup>2</sup>, and SOT-223 packages.

### Features

- Output Current to 1.5 A
- Output Accuracy to  $\pm 1.0\%$  Over Temperature
- Dropout Voltage (typical) 1.05 V @ 1.5 A
- Fast Transient Response
- Fault Protection
  - Current Limit
  - Thermal Shutdown

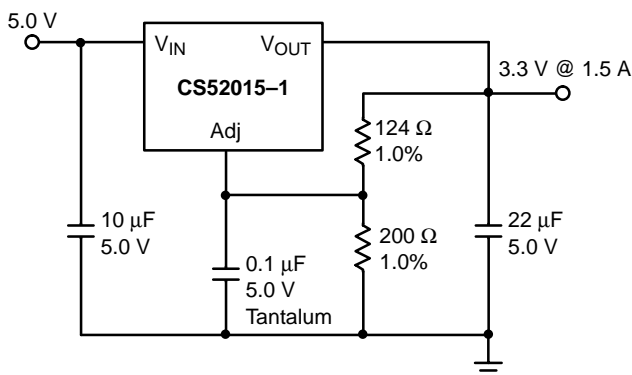
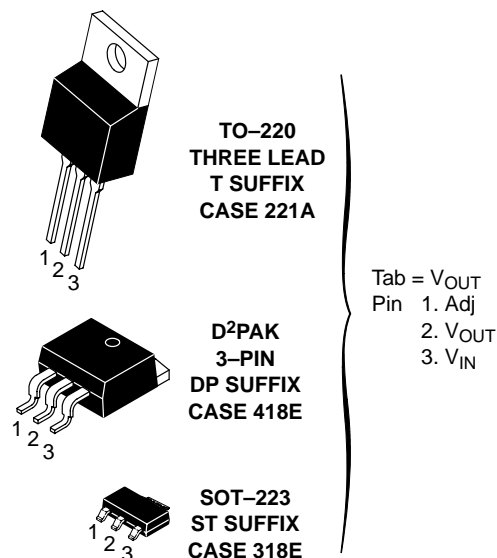


Figure 1. Application Diagram



ON Semiconductor™

<http://onsemi.com>



### ORDERING INFORMATION\*†

Device	Package	Shipping
CS52015-1GT3	TO-220‡	50 Units/Rail
CS52015-1GDP3	D <sup>2</sup> PAK‡	50 Units/Rail
CS52015-1GDPR3	D <sup>2</sup> PAK‡	750 Tape & Reel
CS52015-1GST3	SOT-223‡	80 Units/Rail
CS52015-1GSTR3	SOT-223‡	2500 Tape & Reel

\*Additional ordering information can be found on page 7 of this data sheet.

†Consult your local sales representative for fixed output voltage versions.

‡TO-220 are all 3-pin, straight leaded. D<sup>2</sup>PAK and SOT-223 are all 3-pin.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

**ABSOLUTE MAXIMUM RATINGS\***

Parameter	Value	Unit
Supply Voltage, $V_{CC}$	7.0	V
Operating Temperature Range	-40 to +70	°C
Junction Temperature	150	°C
Storage Temperature Range	-60 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) Note 1. Reflow (SMD styles only) Note 2.	260 Peak 230 Peak °C
ESD Damage Threshold	2.0	kV

1. 10 second maximum.

2. 60 second maximum above 183°C

\*The maximum package power dissipation must be observed.

**ELECTRICAL CHARACTERISTICS** ( $C_{IN} = 10 \mu F$ ,  $C_{OUT} = 22 \mu F$  Tantalum,  $V_{OUT} + V_{DROPOUT} < V_{IN} < 7.0 V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ ,  $T_J \leq +150^\circ C$ , unless otherwise specified,  $I_{full load} = 1.5 A$ )

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Adjustable Output Voltage</b>					
Reference Voltage (Notes 3. and 4.)	$V_{IN} - V_{OUT} = 1.5 V$ ; $V_{Adj} = 0 V$ $10 mA \leq I_{OUT} \leq 1.5 A$	1.241 (-1.0%)	1.254	1.266 (+1.0%)	V
Line Regulation	$1.5 V \leq V_{IN} - V_{OUT} \leq 5.75 V$ ; $I_{OUT} = 10 mA$	—	0.02	0.20	%
Load Regulation (Notes 3. and 4.)	$V_{IN} - V_{OUT} = 1.5 V$ ; $10 mA \leq I_{OUT} \leq 1.5 A$	—	0.04	0.4	%
Dropout Voltage (Note 5.)	$I_{OUT} = 1.5 A$	—	1.05	1.4	V
Current Limit	$V_{IN} - V_{OUT} = 3.0 V$ ; $T_J \geq 25^\circ C$	1.6	3.1	—	A
Minimum Load Current (Note 6.)	$V_{IN} = 7.0 V$ , $V_{Adj} = 0 V$	—	0.6	2.0	mA
Adjust Pin Current	$V_{IN} - V_{OUT} = 3.0 V$ ; $I_{OUT} = 10 mA$	—	50	100	$\mu A$
Thermal Regulation (Note 7.)	30 ms Pulse, $T_A = 25^\circ C$	—	0.002	0.020	%/W
Ripple Rejection (Note 7.)	$f = 120 Hz$ ; $I_{OUT} = 1.5 A$ ; $V_{IN} - V_{OUT} = 3.0 V$ ; $V_{RIPPLE} = 1.0 V_{PP}$	—	80	—	dB
Thermal Shutdown (Note 8.)	—	150	180	210	°C
Thermal Shutdown Hysteresis (Note 8.)	—	—	25	—	°C

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account separately.

4. Specifications apply for an external Kelvin sense connection at a point on the output pin 1/4" from the bottom of the package.

5. Dropout voltage is a measurement of the minimum input/output differential at full load.

6. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum requirement.

7. Guaranteed by design, not 100% tested in production.

8. Thermal shutdown is 100% functionally tested in production.

**PACKAGE PIN DESCRIPTION**

Package Pin Number			Pin Symbol	Function
TO-220	D <sup>2</sup> PAK	SOT-223		
1	1	1	Adj	Adjust pin (low side of the internal reference).
2	2	2	$V_{OUT}$	Regulated output voltage (case).
3	3	3	$V_{IN}$	Input voltage.

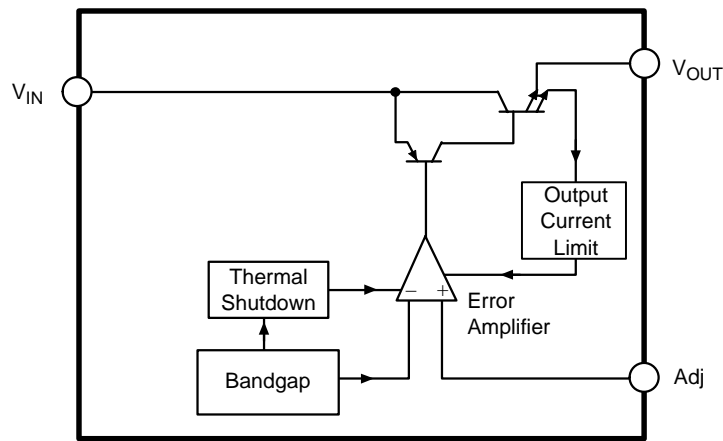


Figure 2. Block Diagram

### TYPICAL PERFORMANCE CHARACTERISTICS

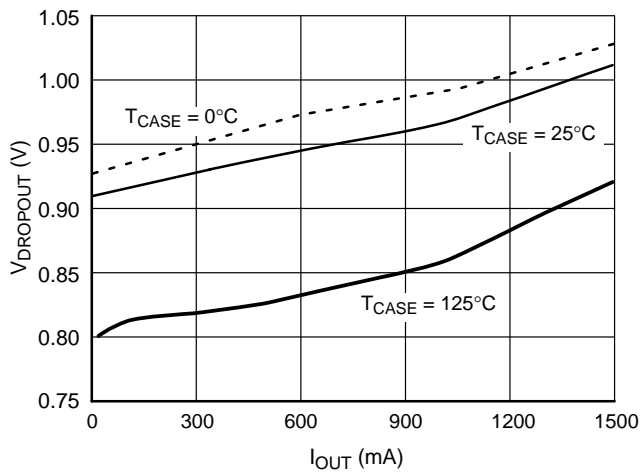


Figure 3. Dropout Voltage vs. Output Current

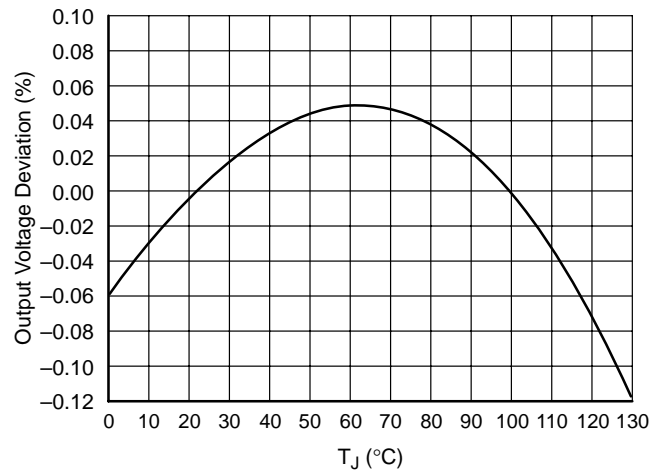


Figure 4. Reference Voltage vs. Temperature

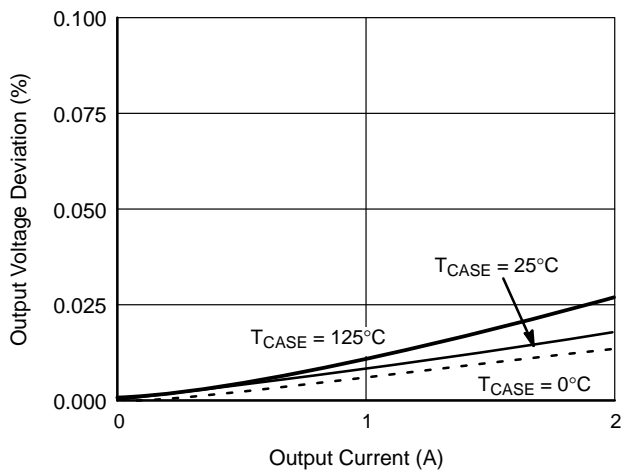


Figure 5. Load Regulation vs. Output Current

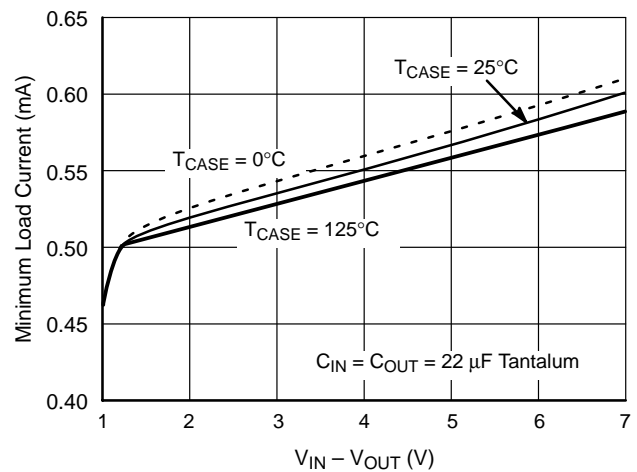
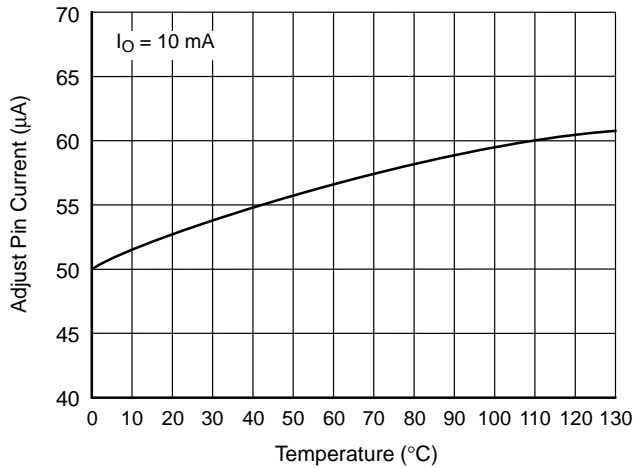
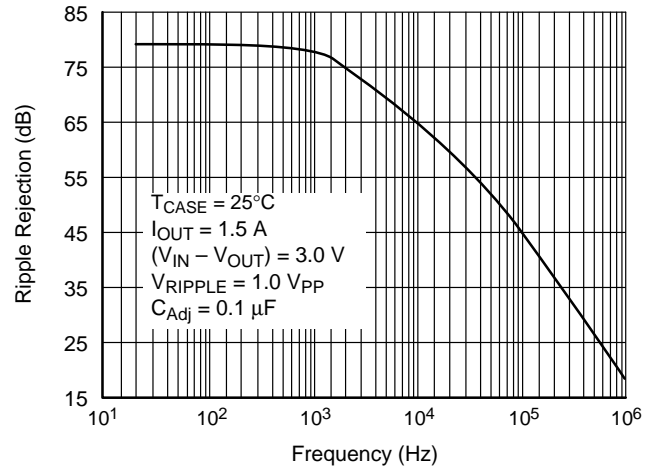


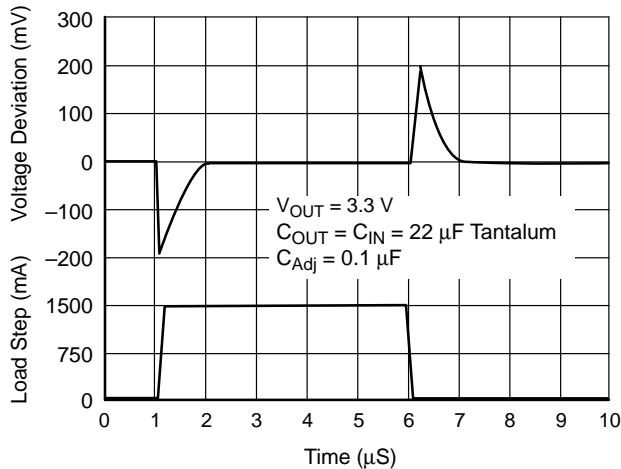
Figure 6. Minimum Load Current vs.  $V_{IN} - V_{OUT}$



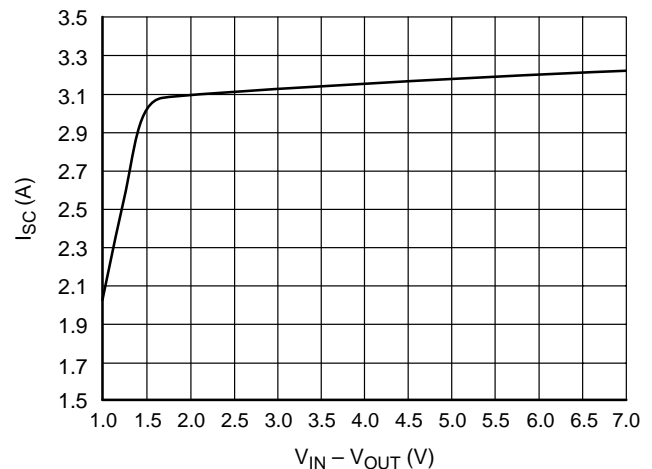
**Figure 7. Adjust Pin Current vs. Temperature**



**Figure 8. Ripple Rejection vs. Frequency**



**Figure 9. Transient Response**



**Figure 10. Short Circuit Current vs.  $V_{IN} - V_{OUT}$**

## APPLICATIONS INFORMATION

The CS52015-1 linear regulator provides adjustable voltages at currents up to 1.5 A. The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS52015-1 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

### Adjustable Operation

The CS52015-1 has an output voltage range of 1.25 V to 5.5 V. An external resistor divider sets the output voltage as shown in Figure 11. The regulator maintains a fixed 1.25V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R1 and sets the overall output voltage. The adjust pin current (typically 50 µA) also flows through R2 and adds a small error that should be taken into account if precise adjustment of  $V_{OUT}$  is necessary.

The output voltage is set according to the formula:

$$V_{OUT} = V_{REF} \times \left( \frac{R1 + R2}{R1} \right) + I_{Adj} \times R2$$

The term  $I_{Adj} \times R2$  represents the error added by the adjust pin current.

$R_1$  is chosen so that the minimum load current is at least 2.0 mA.  $R_1$  and  $R_2$  should be the same type, e.g. metal film for best tracking over temperature. While not required, a bypass capacitor from the adjust pin to ground will improve ripple rejection and transient response. A 0.1  $\mu\text{F}$  tantalum capacitor is recommended for “first cut” design. Type and value may be varied to obtain optimum performance vs. price.

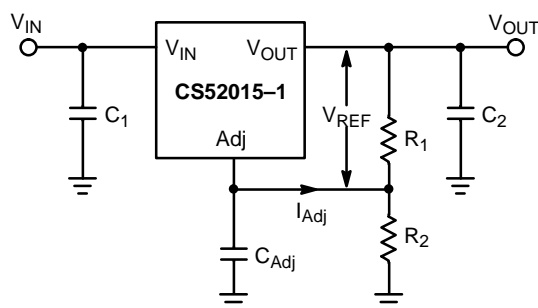


Figure 11. Resistor Divider Scheme

### Short Circuit Protection

The CS52015-1 linear regulator has an absolute maximum specification of 7.0 V for the voltage difference between  $V_{IN}$  and  $V_{OUT}$ . However, the IC may be used to regulate voltages in excess of 7.0 V. The main considerations in such a design are power-up and short circuit capability.

In most applications, ramp-up of the power supply to  $V_{IN}$  is fairly slow, typically on the order of several tens of milliseconds, while the regulator responds in less than one microsecond. In this case, the linear regulator begins charging the load as soon as the  $V_{IN}$  to  $V_{OUT}$  differential is large enough that the pass transistor conducts current. The load at this point is essentially at ground, and the supply voltage is on the order of several hundred millivolts, with the result that the pass transistor is in dropout. As the supply to  $V_{IN}$  increases, the pass transistor will remain in dropout, and current is passed to the load until  $V_{OUT}$  reaches the point at which the IC is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. The result is that the output voltage follows the power supply ramp-up, staying in dropout until the regulation point is reached. In this manner, any output voltage may be regulated. There is no theoretical limit to the regulated voltage as long as the  $V_{IN}$  to  $V_{OUT}$  differential of 7.0 V is not exceeded.

However, the possibility of destroying the IC in a short circuit condition is very real for this type of design. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Over-voltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the  $V_{IN}$  to  $V_{OUT}$  differential to less than 7.0 V if failsafe operation is required. One possible clamp circuit is

illustrated in Figure 12; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.

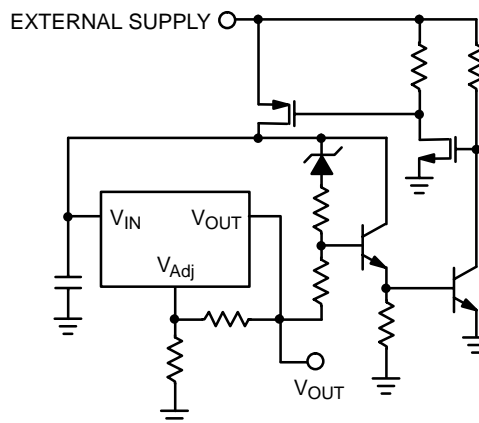


Figure 12. Short Circuit Protection Circuit for High Voltage Application.

### Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

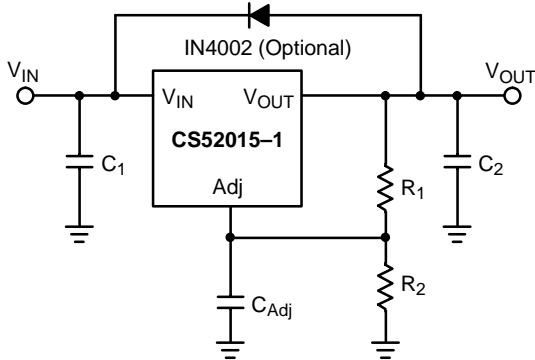
A 22  $\mu\text{F}$  tantalum capacitor will work for most applications, but with high current regulators such as the CS52015-1 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$\Delta V = \Delta I \times \text{ESR}$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close as possible to the load for the best results.

### Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which  $V_{IN}$  drops. In the CS52015-1 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 13 is recommended.



**Figure 13. Protection Diode for Large Output Capacitors**

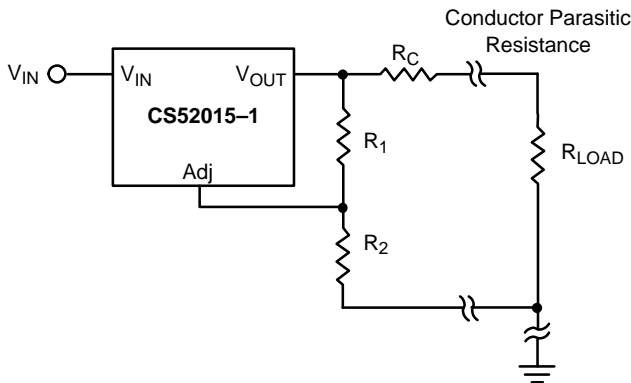
### Output Voltage Sensing

Since the CS52015-1 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.

For the adjustable regulator, the best load regulation occurs when  $R_1$  is connected directly to the output pin of the regulator as shown in Figure 14. If  $R_1$  is connected to the load,  $R_C$  is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes.

$$R_C \times \left( \frac{R_1 + R_2}{R_1} \right)$$

where  $R_C$  = conductor parasitic resistance.



**Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitic Resistance Effects**

### Calculating Power Dissipation and Heat Sink Requirements

The CS52015-1 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to  $V_{OUT}$  on the CS52015-1, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature  $T_A$  ( $^{\circ}\text{C}$ )
2. Power dissipation  $P_D$  (Watts)
3. Maximum junction temperature  $T_J$  ( $^{\circ}\text{C}$ )
4. Thermal resistance junction to ambient  $R_{\theta JA}$  ( $^{\circ}\text{C/W}$ )

These four are related by the equation

$$T_J = T_A + P_D \times R_{\theta JA} \quad (1)$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

$$P_{D(\max)} = \{V_{IN(\max)} - V_{OUT(\min)}\}I_{OUT(\max)} + V_{IN(\max)}I_Q \quad (2)$$

where:

$V_{IN(\max)}$  is the maximum input voltage,

$V_{OUT(\min)}$  is the minimum output voltage,

$I_{OUT(\max)}$  is the maximum output current, for the application

$I_Q$  is the maximum quiescent current at  $I_{OUT(\max)}$ .

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine  $R_{\theta JA}$ , the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case,  $R_{\theta JC}$  ( $^{\circ}\text{C/W}$ )
2. Thermal Resistance of the case to Heat Sink,  $R_{\theta CS}$  ( $^{\circ}\text{C/W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air,  $R_{\theta SA}$  ( $^{\circ}\text{C/W}$ )

These are connected by the equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

## CS52015–1

The value for  $R_{\theta JA}$  is calculated using equation (3) and the result can be substituted in equation (1).

The value for  $R_{\theta JC}$  is 3.5°C/W for a given package type based on an average die size. For a high current regulator such as the CS52015–1 the majority of the heat is generated in the power transistor section. The value for  $R_{\theta SA}$  depends on the heat sink type, while  $R_{\theta CS}$  depends on factors such as package type, heat sink interface (is an insulator and

thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of  $R_{\theta JA}$  can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note “Thermal Management for Linear Regulators,” document number SR006AN/D, available through the Literature Distribution Center or via our website at <http://onsemi.com>.

### ADDITIONAL ORDERING INFORMATION

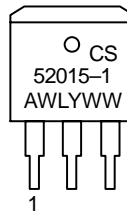
Orderable Part Number	Type	Description
CS52015–1GT3	1.5 A, Adj. Output	TO–220 THREE LEAD, STRAIGHT
CS52015–1GDP3	1.5 A, Adj. Output	D <sup>2</sup> PAK 3–PIN
CS52015–1GDPR3	1.5 A, Adj. Output	D <sup>2</sup> PAK 3–PIN (Tape & Reel)
CS52015–1GST3	1.5 A, Adj. Output	SOT–223
CS52015–1GSTR3	1.5 A, Adj. Output	SOT–223 (Tape & Reel)

### MARKING DIAGRAMS

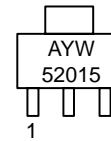
**TO–220  
THREE LEAD  
T SUFFIX  
CASE 221A**



**D<sup>2</sup>PAK  
3–PIN  
DP SUFFIX  
CASE 418E**



**SOT–223  
ST SUFFIX  
CASE 318E**

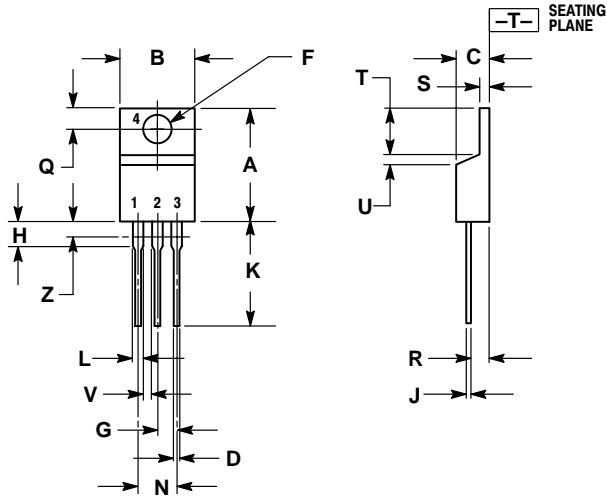


A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week

# CS52015-1

## PACKAGE DIMENSIONS

TO-220  
THREE LEAD  
T SUFFIX  
CASE 221A-09  
ISSUE AA

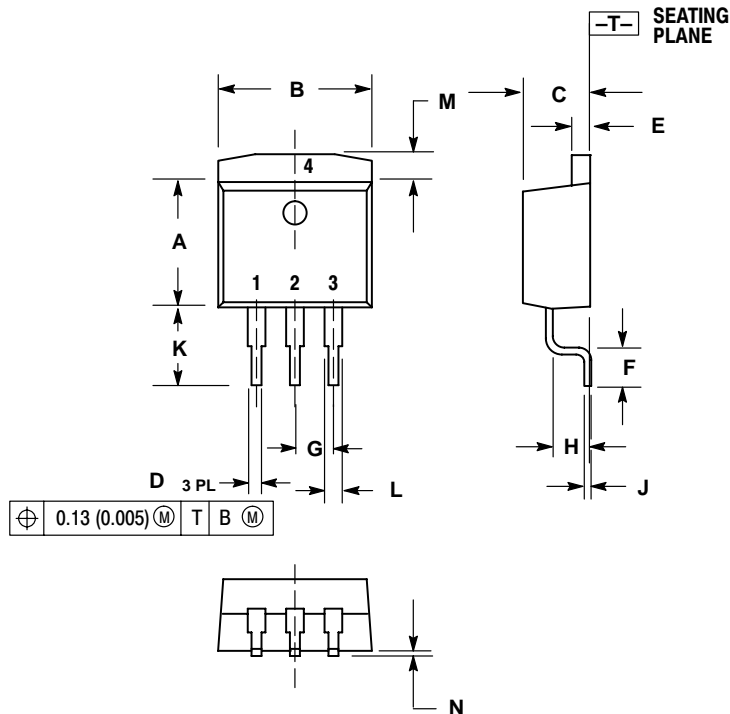


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

D<sup>2</sup>PAK  
3-PIN  
DP SUFFIX  
CASE 418E-01  
ISSUE O



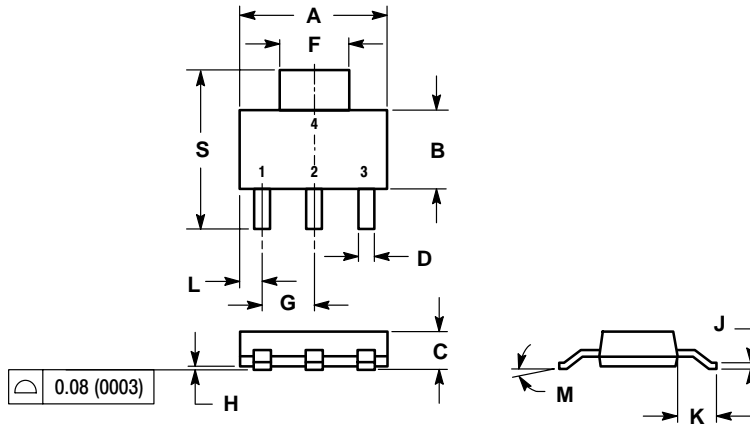
### NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.100 BSC		2.54 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
L	0.045	0.055	1.14	1.40
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

# CS52015-1

**SOT-223**  
**ST SUFFIX**  
CASE 318E-04  
ISSUE K



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0°	10°	0°	10°
S	0.264	0.287	6.70	7.30


## PACKAGE THERMAL DATA

Parameter		TO-220 THREE LEAD	D <sup>2</sup> PAK 3-PIN	SOT-223	Unit
R <sub>θJC</sub>	Typical	3.5	3.5	15	°C/W
R <sub>θJA</sub>	Typical	50	10-50*	156	°C/W

\* Depending on thermal properties of substrate.  $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

## **Notes**

## **Notes**

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
**Email:** ONlit-german@hibbertco.com

**French Phone:** (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
**Email:** ONlit-french@hibbertco.com

**English Phone:** (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, UK, Ireland

### CENTRAL/SOUTH AMERICA:

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
**Toll Free** from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2745

**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.