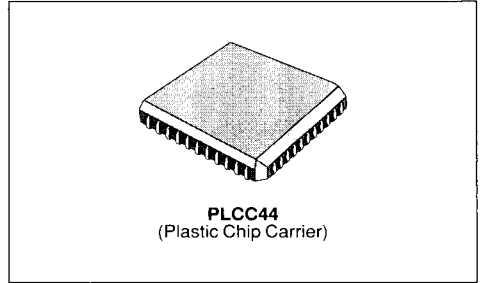




## 2-D DISCRETE COSINE TRANSFORM IMAGE PROCESSOR

- 8 X 8 TRANSFORM SIZE.
- 8 X 8 DCT CALCULATION TIME = 3.2μs.
- DC TO 20 MHZ PIXEL RATE.
- 9-BIT ADD/SUBTRACT INPUT.
- 12-BIT INPUT/OUTPUT.
- 14-BIT FIXED COEFFICIENTS.
- MULTIFUNCTION CAPABILITY (DCT, IDCT, FILTER).
- FULL INTERNAL PRECISION, FOR EACH DIMENSION.
- FULLY SYNCHRONOUS INTERFACE.
- HIGH SPEED CMOS IMPLEMENTATION.
- TTL COMPATIBLE.
- SINGLE +5V ± 10%.
- POWER DISSIPATION < 1.5 WATT.
- 44 PIN PLASTIC PACKAGE.



### ORDERING INFORMATION

Designation	Package	Clock speed
IMS A121-J20S	PLCC44	20MHz

A121-01.TBL

### DESCRIPTION

The IMS A121 is a device for computing the Discrete Cosine Transform (DCT & IDCT). It will also function as a 2-D linear filter or perform matrix transposition. These 4 functions operate on blocks of data with a fixed size of 64 samples (8 × 8). The IMS A121 has other functions aimed specifically at the implementation of video codecs; on-chip subtraction and addition functions may be selected to reduce system chip count.

The main computation is performed by two identical multiplication arrays, each of which perform an 8 × 8 matrix multiplication in 64 cycles, with no internal rounding. The DCT/filter coefficients (14-bit) are stored in 4 banks of fixed ROM. The intermediate 8 × 8 matrix result is rounded to 16 bits and stored in the transposition RAM between each multiplication array. The device is fully pipelined with data sampled on the input at the clock frequency and the resultant output appearing 128 clock cycles later.

### PIN CONNECTIONS

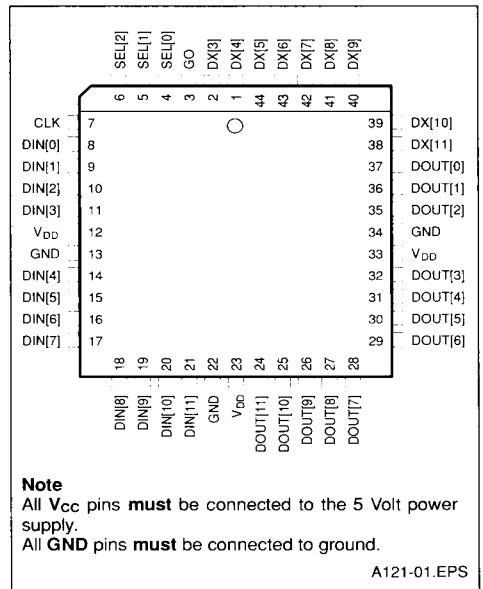
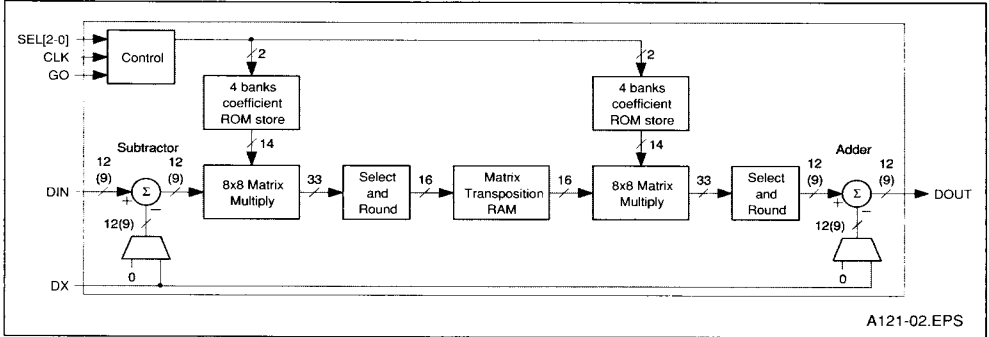


Figure 1



A121-02.EPS

**1. OVERALL DEVICE OPERATION**

The IMS A121 is a device for computing the Discrete Cosine Transform (DCT) and the Inverse Discrete Cosine Transform (IDCT). It can also perform a simple low-pass filter operation.

The IMS A121 processes blocks of data which are 64 samples long and represent an 8 x 8 matrix. Data is sampled on the **Din** port every cycle and data is output every cycle on the **Dout** port.

The **GO** signal is used to indicate the start of a block. When it is sampled high the data on the **Din** port is the first sample of the block. The mode select signals **SEL[2-0]** are sampled at the same time. The remainder of the block of data is sampled on the **Din** port for the subsequent 63 cycles and during this time the **GO** signal and the **SEL** port are ignored. Each consecutive group of eight samples is treated as a column, eight such columns making a block.

The computation is in two stages, between which the block of 64 intermediate samples is stored in the transposition RAM. The transposition RAM serves a dual function of storing the intermediate results and transposing the data from column order into row order. This permits the two matrix computation elements to be identical although the first stage does the column computations and the second stage does the row computations.

Data is output on the **Dout** port in blocks of 64 samples. However, each consecutive group of eight samples now represents a row because of the internal transposition of data. The first sample of the block is output on the **Dout** port 128 cycles after the first sample of the block was sampled on the **Din** port.

An auxiliary port, **Dx** is provided. The data on the **Dx** port is optionally subtracted from the data on

the **Din** port (DCT mode) or added to the output (IDCT mode).

The IMS A121 views input data in column order and (because of the internal transposition) output data in row order. However, this convention is only used to define the arithmetic which the IMS A121 performs. The system in which the IMS A121 is a component may well view the data going into the IMS A121 in row order and the data coming out in column order.

**1.1 The fixed ROM coefficients**

There are four sets of fixed ROM coefficients, each corresponding to one of the four possible functions the device can perform. The two main functions which the device can perform are the DCT and the IDCT. The other two functions provide assistance for the implementation of a video codec. The filter function is provided at very little overhead because the device is essentially a 2-D filter. The transposition function which is a unity multiplication, enables a simple method of switching out the filter without any external logic.

**1.2 Number formats**

All numbers input to the IMS A121 are signed integers. The **Din** and **Dout** ports use 12 bit signed integers, while the **Dx** port uses 9 bit signed integers. In both cases the number format is twos complement binary. Little Endian format is assumed throughout, so that, for example, **Din[0]** is the least significant bit of the **Din** port and **Din[11]** the most significant (sign) bit. When a nine bit number is transferred over one of the 12 bit ports the most significant nine bits are used. The lowest three bits of the **Din** port are ignored and the lowest three bits of the **Dout** port will be zero.

### 1.3 Internal Bit-field Selectors and Rounding

The transforms are implemented by a matrix multiplication with no truncation or rounding. This yields a 33 bit result, with bit-field selectors provided to select the parts of the result which are of interest. 16 bits are selected from the output of the first matrix multiplication, which are stored in the matrix transposition RAM. Either 9 bits or 12 bits are selected from the output of the second matrix multiplication (depending on the selected mode).

Bits below the selected range are discarded although the result is rounded not truncated. This is a simple round towards  $+\infty$ ; if the most significant bit of those bits which have been discarded is set then one is added to the bits which are retained.

### 1.4 Overflow, Saturation and Clipping

Overflow can occur in the subtraction unit, the two bit-field selectors or the addition unit. Overflow occurs whenever there are insufficient bits in the result to represent the number. When overflow occurs the result is replaced by the most positive or the most negative number which can be represented (depending on the sign of the correct result). The device will normally be used in a feedback system. If either positive or negative overflow occurs, then inaccuracies have been introduced. However, the system will remain stable.

In some of the IDCT modes the output is clipped so that all results are positive and all negative numbers are replaced by zero. This ensures that the output is a valid (8-bit) pixel, between 0 and 255.

### 1.5 Subtraction with the DCT function

When the IMS A121 is used to perform the DCT, it is possible to enable the on-chip subtraction unit, so that before the DCT the data on the **Dx** port is subtracted from the data on the **Din** port. The data is presented to the **Dx** port at exactly the same time as to the **Din** port.

In DCT mode the data on the **Din** port is a nine bit number (the lowest 3 of 12 bits are ignored). The result of the subtraction is saturated to nine bits before being passed to the matrix multiplier.

### 1.6 Addition with the IDCT function

When the IMS A121 is used to perform the IDCT, it is possible to enable the on-chip addition unit, so that after the IDCT of the data has been done, the

result may be added to the data on the **Dx** port. The timing requires careful consideration because of the latency of the device (128 cycles). The first sample of a block must be presented on the **Dx** port 124 cycles after the first sample was presented to **Din**. The data presented to the **Dx** port should be transposed and is thus in the same order as it will come out of **Dout** four cycles later.

The result of the addition is saturated to nine bits and then clipped so that all negative numbers are replaced by zero. The nine bit result is presented on **Dout[11-3]**, while **Dout[2-0]** will be zero. **Dout[11]** will be zero because all the numbers are positive.

Two modes are provided which perform the IDCT without addition. One of these modes disables the adder completely so that nine bit signed results appear on **Dout**. The other mode does NOT add on the value on the **Dx** port but still clips the result so that only positive values appear on **Dout**.

### 1.7 Resetting

The IMS A121 does not have a reset pin. At power-on the internal state will be undefined and as a result the first three blocks processed are not guaranteed correct. **GO** must be held low for at least 191 cycles to ensure that when it does go high it is interpreted as the start of a block.

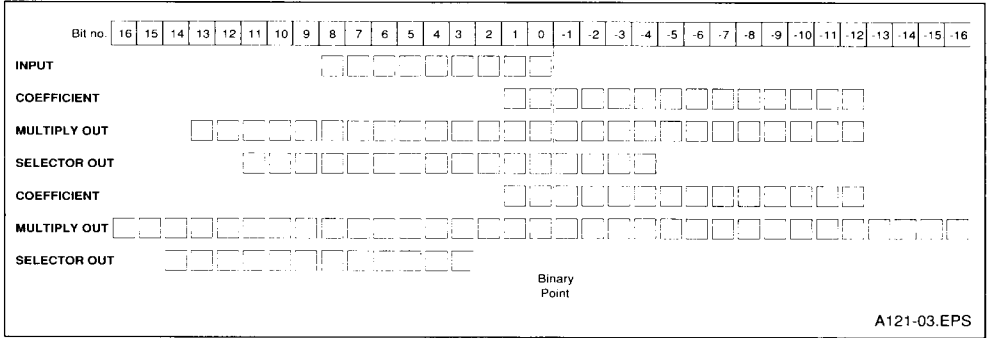
## 2. DCT FUNCTION

The DCT function is selected when **SEL[2-0]=000** or 100 (mode 0 or 4).

### 2.1 Internal number format

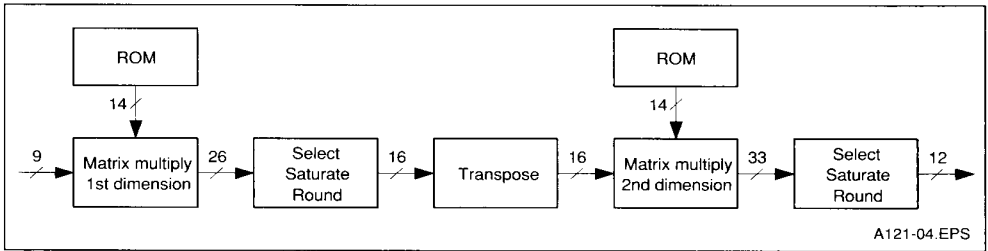
The input for the DCT is a 9 bit signed integer in the range -256 to +255. This is either an external input or the output of the on-chip subtractor depending on **SEL[2-0]**. The input is multiplied in the matrix multiplication array by 14 bit signed fixed point numbers in the range -2 to  $(2 \cdot 2^{-12})$ . The accumulated result of 8 multiply operations is a 26 bit signed integer, the bottom 8 bits of which are rounded (see section 1.3) and the top 2 bits used to saturate the output (see section 1.4). The result of the first matrix multiply is stored as a 16 bit signed integer and the second matrix multiply performed in exactly the same manner, yielding 33 bit results. The output rounds the bottom 19 bits, saturates the top 2 bits giving a 12 bit signed integer in the range -2048 to +2047.

Figure 2 : DCT Internal Number Format



2.2 Internal data flow

Figure 3 : Internal Data Flow



2.3 The mathematical basis for the DCT

The 1 dimensional equation for the DCT is as follows:

$$X(k) = \sqrt{\frac{2}{N}} \alpha(k) \sum_{m=0}^{N-1} x(m) \cos \left[ \frac{(2m+1)k\pi}{2N} \right] \quad k=0,1,\dots,N-1$$

**Forward transform**

where

$$\alpha(k) = \begin{cases} 1 & \text{for } k=0 \\ \sqrt{2} & \text{for } k=1 \dots N-1 \end{cases}$$

where x(m) represent the input samples and X(k) is the resulting output. The special case for the

IMSA121 is with N=8 and the actual filter coefficients are then calculated. The following equation is used to calculate the actual filter coefficients.

$$\text{Coeff}_{km} = \sqrt{2} \alpha(k) \cos \left[ \frac{(2m+1)k\pi}{2N} \right]$$

**DCT coefficients**

It should be noticed that the coefficients are  $2\sqrt{2}$  times bigger than in the forward transform equation. This means that the output after the 2 dimensional DCT is 8 times too big (The 1 dimensional transform is applied twice giving  $(2\sqrt{2})^2$  magnitude increase). This is in accordance with the 3 bit shift of the output data necessary to give the correct 12 bit signed output.

**DCT coefficients**

1.0000	1.0000	1.0000	1.0000	1.0000	1.0000	1.0000	1.0000
1.3870	1.1759	0.7857	0.2759	-0.2759	-0.7857	-1.1759	-1.3870
1.3066	0.5412	-0.5412	-1.3066	-1.3066	-0.5412	0.5412	1.3066
1.1759	-0.2759	-1.3870	-0.7857	0.7857	1.3870	0.2759	-1.1759
1.0000	-1.0000	-1.0000	1.0000	1.0000	-1.0000	-1.0000	1.0000
0.7857	-1.3870	0.2759	1.1759	-1.1759	-0.2759	1.3870	-0.7857
0.5412	-1.3066	1.3066	-0.5412	-0.5412	1.3066	-1.3066	0.5412
0.2759	-0.7857	1.1759	-1.3870	1.3870	-1.1759	0.7857	-0.2759

**DCT coefficients (14 bit signed integers)**

4096	4096	4096	4096	4096	4096	4096	4096
5681	4816	3218	1130	-1130	-3218	-4816	-5681
5352	2217	-2217	-5352	-5352	-2217	2217	5352
4816	-1130	-5681	-3218	3218	5681	1130	-4816
4096	-4096	-4096	4096	4096	-4096	-4096	4096
3218	-5681	1130	4816	-4816	-1130	5681	-3218
2217	-5352	5352	-2217	-2217	5352	-5352	2217
1130	-3218	4816	-5681	5681	-4816	3218	-1130

**3. IDCT FUNCTION**

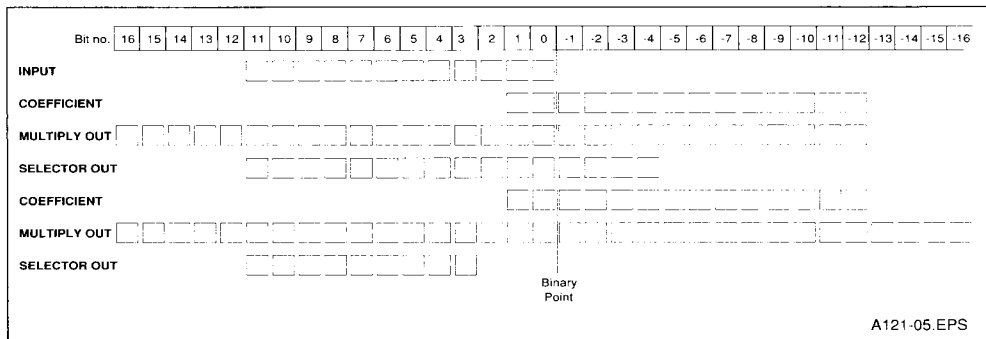
The IDCT function is selected when **SEL[2-0]=001**, 101 or 111 (modes 1, 5 or 7).

**3.1 Internal number format**

The input for the IDCT is a 12 bit signed integer in the range -2048 to +2047. The input is multiplied in the matrix multiplication array by 14 bit signed fixed point numbers in the range -2 to 2-2<sup>12</sup>. The accu-

mulated result of 8 multiply operations is a 29 bit signed integer, the bottom 8 bits of which are rounded (see section 1.3) and the top 5 bits used to saturate the output (see section 1.4). The result of the first matrix multiply is stored as a 16 bit signed integer and the second matrix multiply performed in exactly the same manner, yielding 33 bit results. The output rounds the bottom 19 bits, saturates the top 5 bits giving a 9 bit signed integer in the range -256 to +255

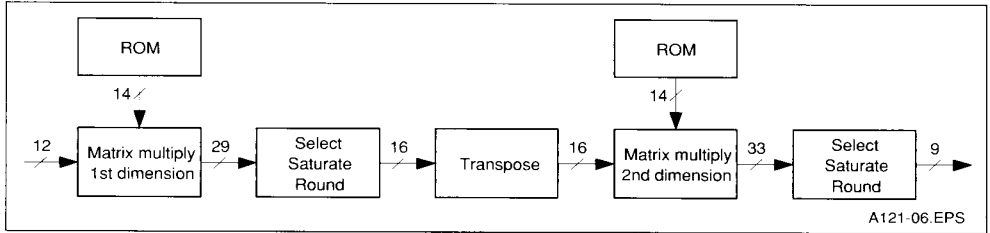
**Figure 4 : IDCT Internal Number Format**



A121-05.EPS

3.2 Internal data flow

Figure 5 : Internal Data Flow



3.3 The mathematical basis for the IDCT

The 1 dimensional equation for the IDCT is as follows:

$$x(m) = \sqrt{\frac{2}{N}} \sum_{k=0}^{N-1} X(k) \alpha(k) \cos \left[ \frac{(2m+1)k\pi}{2N} \right] \quad m=0,1,\dots,N-1$$

**Inverse transform**

**where**

$$\alpha(k) = \begin{cases} \frac{1}{\sqrt{2}} & \text{for } k=0 \\ 1 & \text{for } k=1\dots N-1 \end{cases}$$

where x(m) represent the output samples and X(k)

is the input. The special case for the IMS A121 is for N=8 and the actual filter coefficients are then calculated. The following equation is used to calculate the actual filter coefficients.

$$\text{Coeff}_{mk} = \sqrt{2} \alpha(k) \cos \left[ \frac{(2m+1)k\pi}{2N} \right]$$

**IDCT coefficients**

It should be noticed that the coefficients are  $2\sqrt{2}$  times bigger than in the inverse transform equation. This means that the output after the 2 dimensional IDCT is 8 times too big (The 1 dimensional transform is applied twice giving  $(2\sqrt{2})^2$  magnitude increase). This is in accordance with the 3 bit shift of the output data necessary to give the correct result.

IDCT coefficients

1.0000	1.3870	1.3066	1.1759	1.0000	0.7857	0.5412	0.2759
1.0000	1.1759	0.5412	-0.2759	-1.0000	-1.3870	-1.3066	-0.7857
1.0000	0.7857	-0.5412	-1.3870	-1.0000	0.2759	1.3066	1.1759
1.0000	0.2759	-1.3066	-0.7857	1.0000	1.1759	-0.5412	-1.3870
1.0000	-0.2759	-1.3066	0.7857	1.0000	-1.1759	-0.5412	1.3870
1.0000	-0.7857	-0.5412	1.3870	-1.0000	-0.2759	1.3066	-1.1759
1.0000	-1.1759	0.5412	0.2759	-1.0000	1.3870	-1.3066	0.7857
1.0000	-1.3870	1.3066	-1.1759	1.0000	-0.7857	0.5412	-0.2759

IDCT coefficients (14 bit signed integers)

4096	5681	5352	4816	4096	3218	2217	1130
4096	4816	2217	-1130	-4096	-5681	-5352	-3218
4096	3218	-2217	-5681	-4096	1130	5352	4816
4096	1130	-5352	-3218	4096	4816	-2217	-5681
4096	-1130	-5352	3218	4096	-4816	-2217	5681
4096	-3218	-2217	5681	-4096	-1130	5352	-4816
4096	-4816	2217	1130	-4096	5681	-5352	3218
4096	-5681	5352	-4816	4096	-3218	2217	-1130

4. FILTER FUNCTION

The filter function is selected with **SEL[2-0]=010**. (mode 2)

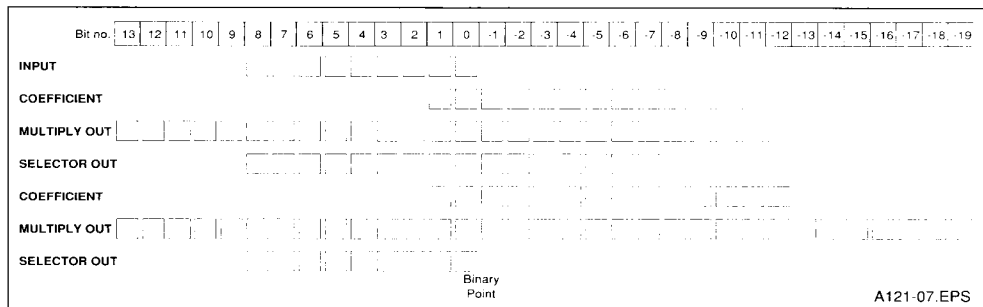
This filter is intended to be used for image data, taking 9 bit signed input data and giving a 9 bit signed result.

### 4.1 Internal number format

The input to the filter is a 9 bit signed integer in the range -256 to +255. The input is multiplied in the matrix multiplication array by 14 bit signed fixed-point numbers in the range -2 to 2·2<sup>-12</sup>. The accumulated result of 8 multiply operations is a 26 bit signed integer, the bottom 5 bits of which are rounded (see section 1.3) and the top 5 bits are

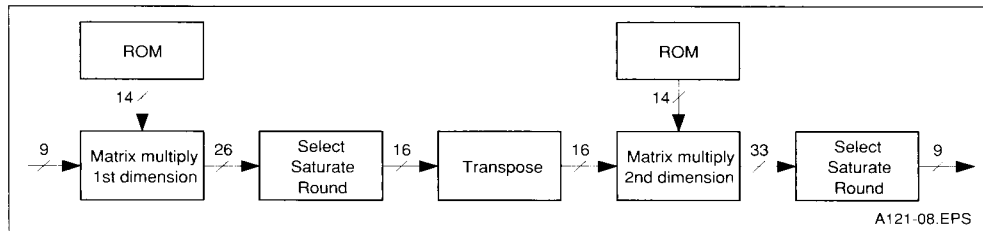
used to saturate the output (see section 1.4). The result of the first matrix multiply is stored as a 16 bit signed integer and the second matrix multiply performed in exactly the same manner, yielding 33 bit results. The output rounds the bottom 19 bits, saturates the top 5 bits giving a 9 bit signed integer in the range -256 to +255.

Figure 6 : Internal Number Format



### 4.2 Internal data flow

Figure 7 : Internal Data Flow



### 4.3 Definition of filter

The filter is a simple  $\frac{1}{4} - \frac{1}{2} - \frac{1}{4}$  filter applied in both dimensions which means that the overall filter kernel is:

$$\frac{1}{16} \begin{bmatrix} 1 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 1 \end{bmatrix}$$

i.e. an output pixel is calculated from the corresponding pixel in the input field and its eight closest neighbours by evaluating

$$\frac{1}{16} (4 \times \text{pixel} + 2 \times (\sum \text{four adjacent pixels}) + 1 \times (\sum \text{four diagonal pixels}))$$

However, at the block edges, where some of the pixels would fall outside the block boundary, the filter is modified to 0--1--0 which means that along the edge the kernel would be:

$$\frac{1}{4} \begin{bmatrix} 0 & 0 & 0 \\ 1 & 2 & 1 \\ 0 & 0 & 0 \end{bmatrix} \text{ (rotated suit)}$$

and the corner pixels are passed through unmodified.

**Filter coefficients**

1.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
0.2500	0.5000	0.2500	0.0000	0.0000	0.0000	0.0000	0.0000
0.0000	0.2500	0.5000	0.2500	0.0000	0.0000	0.0000	0.0000
0.0000	0.0000	0.2500	0.5000	0.2500	0.0000	0.0000	0.0000
0.0000	0.0000	0.0000	0.2500	0.5000	0.2500	0.0000	0.0000
0.0000	0.0000	0.0000	0.0000	0.2500	0.5000	0.2500	0.0000
0.0000	0.0000	0.0000	0.0000	0.0000	0.2500	0.5000	0.2500
0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	1.0000

**Filter coefficients (14 bit signed integers)**

4096	0	0	0	0	0	0	0
1024	2048	1024	0	0	0	0	0
0	1024	2048	1024	0	0	0	0
0	0	1024	2048	1024	0	0	0
0	0	0	1024	2048	1024	0	0
0	0	0	0	1024	2048	1024	0
0	0	0	0	0	1024	2048	1024
0	0	0	0	0	0	1024	2048
0	0	0	0	0	0	0	4096

**5. TRANSPOSER FUNCTION**

The transposition function is selected with

**SEL[2-0]=011.** (mode 3)

This is intended to be used for filtering image data, taking 9 bit signed input data and giving a 9 bit signed result. Data is passed through unmodified and is intended to be used in conjunction with the

filter function (**SEL[2-0]=010**), so that by toggling **SEL[0]** the filter can be switched in and out.

**5.1 Internal number format and data flow**

The internal number format and data flow for the transpose function are the same as for the filter function. Refer to sections 4.1 and 4.2.

**5.2 Transposition coefficients**

1.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
0.0000	1.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
0.0000	0.0000	1.0000	0.0000	0.0000	0.0000	0.0000	0.0000
0.0000	0.0000	0.0000	1.0000	0.0000	0.0000	0.0000	0.0000
0.0000	0.0000	0.0000	0.0000	1.0000	0.0000	0.0000	0.0000
0.0000	0.0000	0.0000	0.0000	0.0000	1.0000	0.0000	0.0000
0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	1.0000	0.0000
0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	1.0000

**5.3 Transposition coefficients (14 bit signed integers)**

4096	0	0	0	0	0	0	0
0	4096	0	0	0	0	0	0
0	0	4096	0	0	0	0	0
0	0	0	4096	0	0	0	0
0	0	0	0	4096	0	0	0
0	0	0	0	0	4096	0	0
0	0	0	0	0	0	4096	0
0	0	0	0	0	0	0	4096



## 6. PIN DESIGNATIONS

### System services

Pin	In/out	Function
V <sub>cc</sub> , GND		Power supply and return
CLK	In	Input clock

### Synchronous input/output

Pin	In/out	Function
GO	In	Initiate input/computation /output cycle
Din[11-0]	In	Data input port
Dout[11-0]	Out	Data output port
Dx[11-3]	In	Addition/subtraction port
SEL[2-0]	In	Mode select input port

### 6.1 System services

#### Power

Power is supplied to the device via the **V<sub>cc</sub>** and **GND** pins. Several of each are provided to minimize inductance within the package. All supply pins must be connected. The supply must be decoupled close to the chip by at least one 100nF low inductance (e.g. ceramic) capacitor between **V<sub>cc</sub>** and **GND**. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling.

Input voltages must not exceed specification with respect to **V<sub>cc</sub>** and **GND**.

#### CLK

The clock input signal **CLK** controls the timing of input and the output on the three dedicated interfaces, and controls the progress of data through the addition/subtraction units, multipliers and transposition RAM. Since the IMS A121 is fully static, the clock can be stopped in either phase without corrupting data.

### 6.2 Synchronous input/output

#### GO

The **GO** signal is active high and is sampled on the rising edge of the input clock. If the device is processing a previous block of data, the **GO** signal is ignored. Otherwise, the processing of a block of 64 pixels commences and the **GO** signal is ignored for a further 63 cycles. Data is always assumed to be valid for the 64 cycles from the start of a major cycle. Blocks of data may be processed at any time and with any spacing between the major blocks, by toggling the **GO** signal as necessary.

#### Din[11-0]

The data input port is sampled 64 times on successive clock cycles, commencing when **GO** is sampled high. Data must be valid on the rising edge of **CLK** for each of the 64 cycles. The block of data may be considered as an 8x8 matrix, where each group of 8 samples represents a column, and the 8 columns are sampled consecutively until the block is complete. The data is twos complement, Little Endian so that **Din[11]** gives sign information, and **Din[12-x]** is the least significant bit where x is the word width indicated by the selected mode.

#### Dout[11-0]

The data output port will be valid for periods spanning 64 clock cycles. The data will be valid on the rising edge of the clock, exactly 128 cycles (the latency) after the data was sampled on the input. This output data, which may be considered as an 8 x 8 matrix, is transposed with respect to the input data. The data is twos complement, Little Endian like the input data.

Blocks of data may follow directly after one-another so that the first data of a block is presented exactly 64 cycles after the first data of the preceding block. However, if there is a gap between blocks zero will appear on the data output port between blocks of data.

#### Dx[11-3]

The addition/subtraction port is sampled on each clock cycle in exactly the same way as the data input port. The data on this port will either be subtracted from the signal on the data input port before matrix multiplication, or, added to the result of matrix multiplication prior to output. The addition and subtraction functions can never be used together. The function selected is determined by the **SEL[2-0]** signals. The data is twos complement, Little Endian like the **Din/Dout** data. Note however, that although the **Dx** port has a different width, **Dx[10]** has the same bitwise significance as **Din[10]/Dout[10]**.

The timing of data on the **Dx** port is different depending on the selected mode.

In the case of subtraction in the DCT mode, **SEL[1-0]=00**, data is presented on the **Dx** port on the same cycle as the corresponding data (from which it will be subtracted) is presented on the **Din** port. In the case of addition in the IDCT mode, **SEL[1-0]=01**, data is presented on the **Dx** port exactly 4 cycles before the corresponding data (to which it will have been added) appears on the **Dout** port.

**SEL[2-0]**

The mode select input port is sampled on the rising edge of **CLK**, when **GO** is active, at the start of a block of data. This fixes the selected mode for the entire block of data.

SEL[2-0]	Mode	Function	PreSubtract	PostAdd	Clipping	Din width	Dout width
000	0	DCT	Disabled	Disabled	Disabled	9	12
001	1	IDCT	Disabled	Disabled	Disabled	12	9
010	2	Filter	Disabled	Disabled	Disabled	9	9
011	3	Transpose	Disabled	Disabled	Disabled	9	9
100	4	DCT	Enabled	Disabled	Disabled	9	12
101	5	IDCT	Disabled	Enabled	Enabled	12	9
110	6	Reserved—Do not use					
111	7	IDCT	Disabled	Disabled	Enabled	12	9

**7. ELECTRICAL SPECIFICATION**

**7.1 DC electrical characteristics**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Min	Typ.	Max	Units	Notes (1)
V <sub>CC</sub>	DC supply voltage	0		7.0	V	2
V <sub>I</sub> , V <sub>O</sub>	Voltage on input and output pins	-1.0		V <sub>CC</sub> +0.5	V	2
T <sub>A</sub>	Temperature under bias	-40		85	°C	2
T <sub>stg</sub>	Storage temperature	-65		150	°C	2
P <sub>Dmax</sub>	Power dissipation			1.5	W	2

**Notes**

- 1 All voltages are with respect to GND.
- 2 This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
V <sub>CC</sub>	DC supply Voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	Input Logic '1' Voltage	2.0		V <sub>CC</sub> +0.5	V	2
V <sub>IL</sub>	Input Logic '0' Voltage	-0.5		0.8	V	2
T <sub>A</sub>	Ambient Operating Temperature	0		70	°C	3

**Notes**

- 1 All voltages are with respect to GND. All **GND** pins must be connected to GND.
- 2 nput signal transients up to 10 ns wide, are permitted in the voltage ranges GND - 0.5 V to GND - 1.0 V and V<sub>CC</sub> + 0.5 V to V<sub>CC</sub> + 1.0 V.
- 3 400 linear ft/min transverse air flow.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2)
V <sub>OH</sub>	Output Logic '1' Voltage	2.4		V <sub>CC</sub>	V	I <sub>O</sub> ≤ -4.4mA
V <sub>OL</sub>	Output Logic '0' Voltage	0		0.4	V	I <sub>O</sub> ≤ 4.4mA
I <sub>IN</sub>	Input Leakage Current (any input)			±10	µA	3
I <sub>CC</sub>	Average Power Supply Current			300	mA	4

Notes

- 1 All voltages are with respect to GND. All GND pins must be connected to GND.
- 2 Under the conditions specified by the DC operating conditions.
- 3 V<sub>CC</sub> = V<sub>CC(max)</sub>, GND ≤ V<sub>IN</sub> ≤ V<sub>CC</sub>
- 4 This applies at 20 MHz and will be less at slower clock rates

7.2 A.C. timing characteristics

All timings are given for a load of 30pF unless otherwise stated.

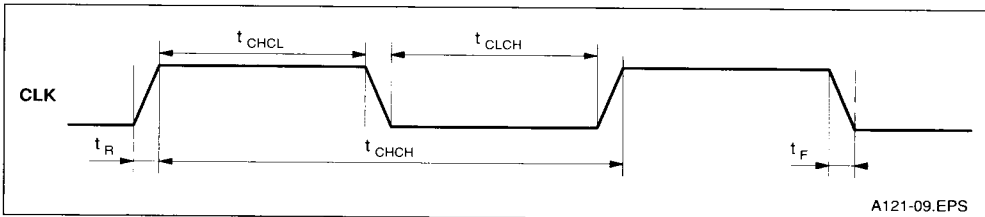
CLOCK REQUIREMENTS

Symbol	Parameter	Min	Typ.	Max	Units	Notes
t <sub>CHCL</sub>	Clock Pulse High Width	20			ns	
t <sub>CLCH</sub>	Clock Pulse Low Width	20			ns	
t <sub>CHCH</sub>	Clock Period	50			ns	
t <sub>R</sub>	Clock Rise Time	0		50	ns	1
t <sub>F</sub>	Clock Fall Time	0		50	ns	1

Notes

- 1 The clock edges should be monotonic between V<sub>IL</sub> and V<sub>IH</sub>.

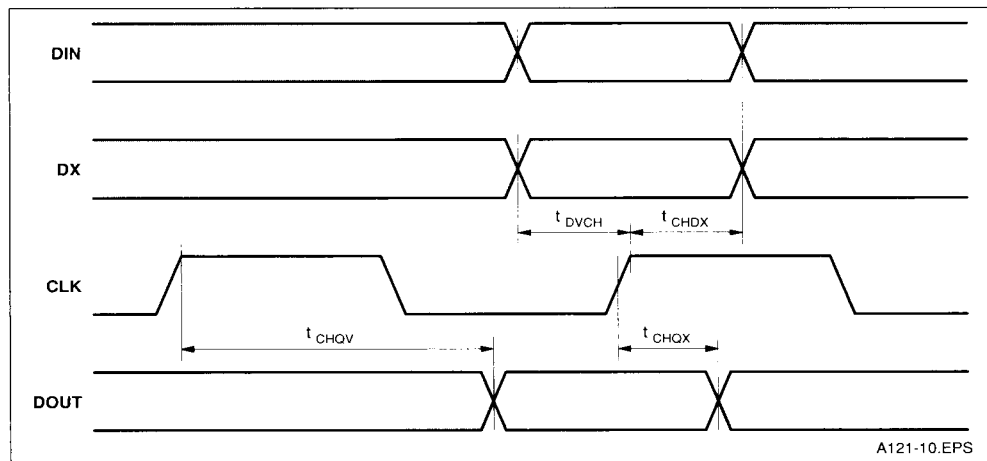
Figure 8



SYNCHRONOUS INPUT AND OUTPUT (Din, Dout, Dx)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
$t_{CHQV}$	CLK High to Dout Valid			38	ns	
$t_{CHQX}$	Dout Hold Time after CLK	2			ns	
$t_{DVCH}$	Din/Dx Setup Time to CLK High	10			ns	
$t_{CHDX}$	Din/Dx Hold Time to CLK High	0			ns	

Figure 9

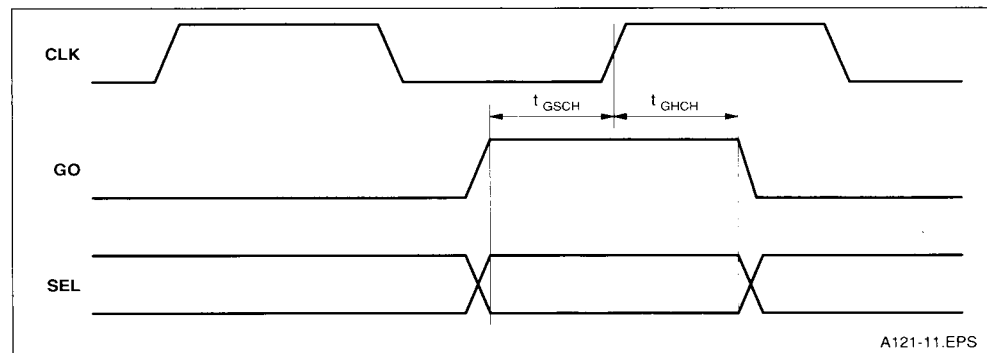


A121-10.EPS

Synchronous control (GO, SEL[2-0])

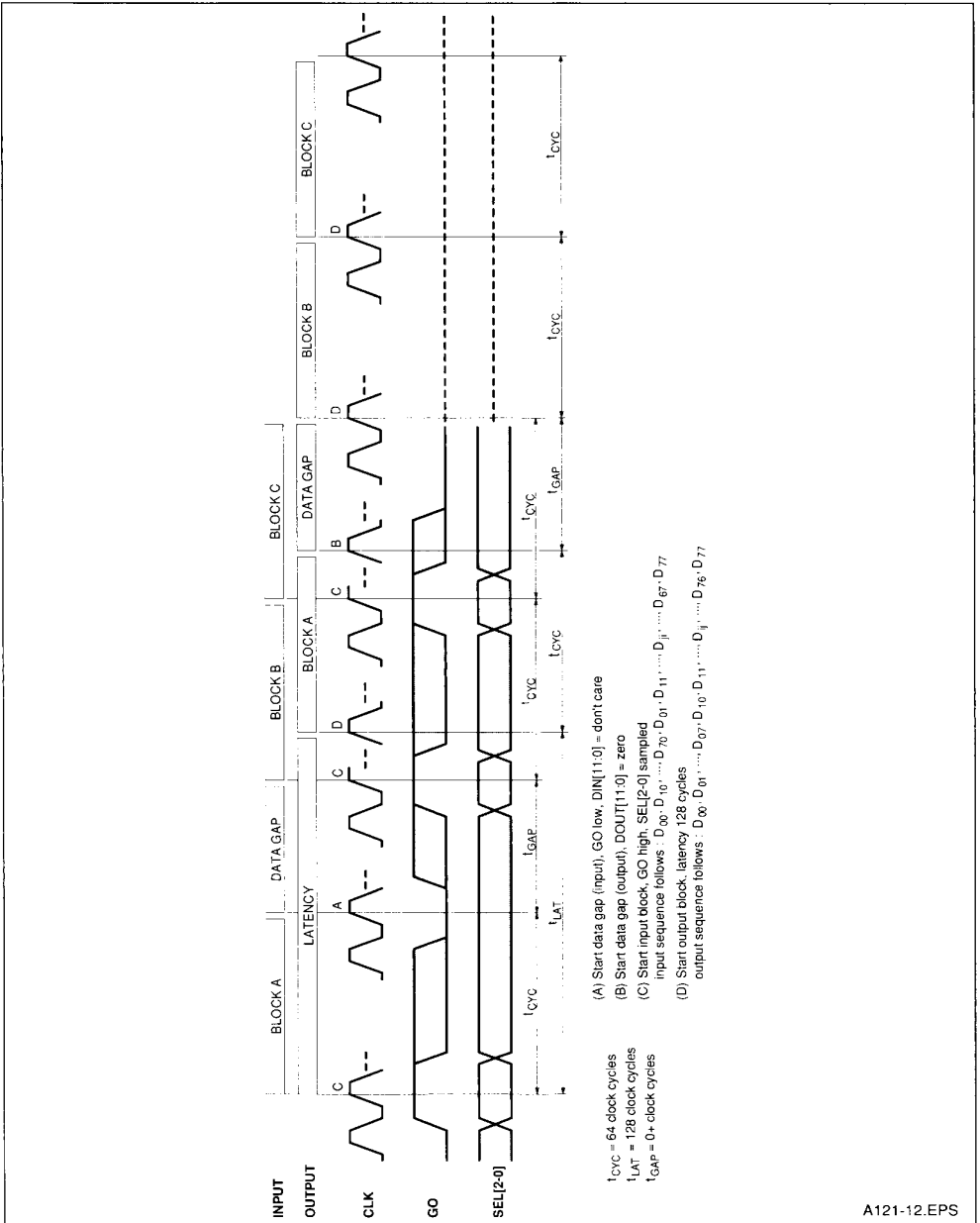
Symbol	Parameter	Min	Typ.	Max	Units	Notes
$t_{GHCH}$	GO/SEL hold to clock high	0			ns	
$t_{GSCH}$	GO/SEL setup to clock high	10			ns	

Figure 10



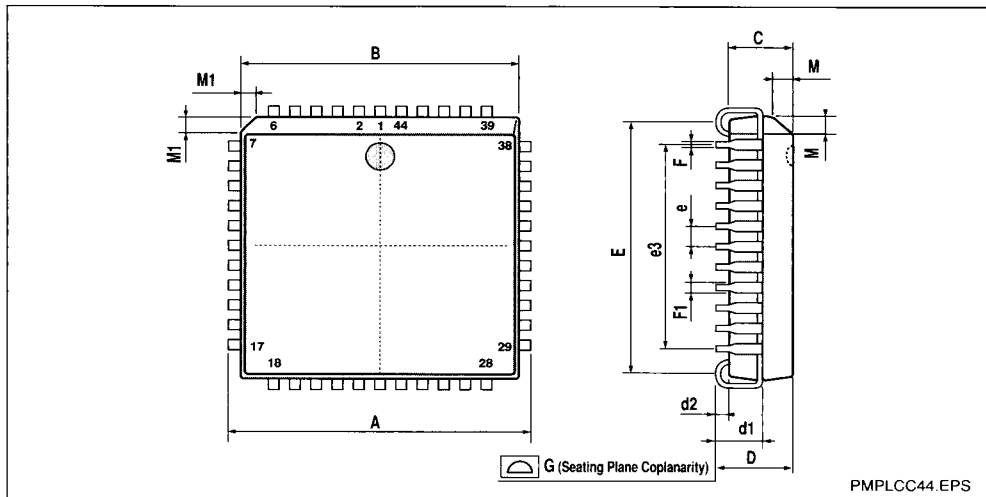
A121-11.EPS

Figure 11 : Overall Data Timing



A121-12.EPS

**PACKAGE MECHANICAL DATA**  
**44 PINS - PLASTIC CHIP CARRIER**



PMPGCC44.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		17.577			0.692	
B		16.612			0.654	
C		3.861			0.152	
D		4.369			0.172	
d1						
d2						
E						
e		1.270			0.050	
e3		12.70			0.500	
F						
F1		0.457			0.018	
G						
M						
M1		1.143			0.045	

PLCC44B.TBL