19-3656; Rev 1; 2/07

1A, 40V, MAXPower Step-Down DC-DC Converters

General Description

The MAX5080/MAX5081 are 250kHz PWM step-down DC-DC converters with an on-chip, 0.3Ω high-side switch. The input voltage range is 4.5V to 40V for the MAX5080 and 7.5V to 40V for the MAX5081. The output is adjustable from 1.23V to 32V and can deliver up to 1A of load current.

Both devices utilize a voltage-mode control scheme for good noise immunity in the high-voltage switching environment and offer external compensation allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The switching frequency is internally fixed at 250kHz and can be synchronized to an external clock signal through the SYNC input. Light load efficiency is improved by automatically switching to a pulse-skip mode.

All devices include programmable undervoltage lockout and soft-start. Protection features include cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown. Both devices are available in a space-saving, high-power (2.7W), 16-pin TQFN package and are rated for operation over the -40°C to +125°C temperature range.

Applications

FireWire® Power Supplies

Automotive

Distributed Power

Industrial

FireWire is a registered trademark of Apple Computer, Inc.

Features

- **4.5V to 40V (MAX5080) or 7.5V to 40V (MAX5081) Input Voltage Range**
- **1A Output Current**
- **V_{OUT} Range From 1.23V to 32V**
- **Internal High-Side Switch**
- **Fixed 250kHz Internal Oscillator**
- **Automatic Switchover to Pulse-Skip Mode at Light Loads**
- **External Frequency Synchronization**
- **Thermal Shutdown and Short-Circuit Protection**
- **Operates Over the -40°C to +125°C Temperature Range**
- **Space-Saving (5mm x 5mm) High-Power 16-Pin TQFN Package**

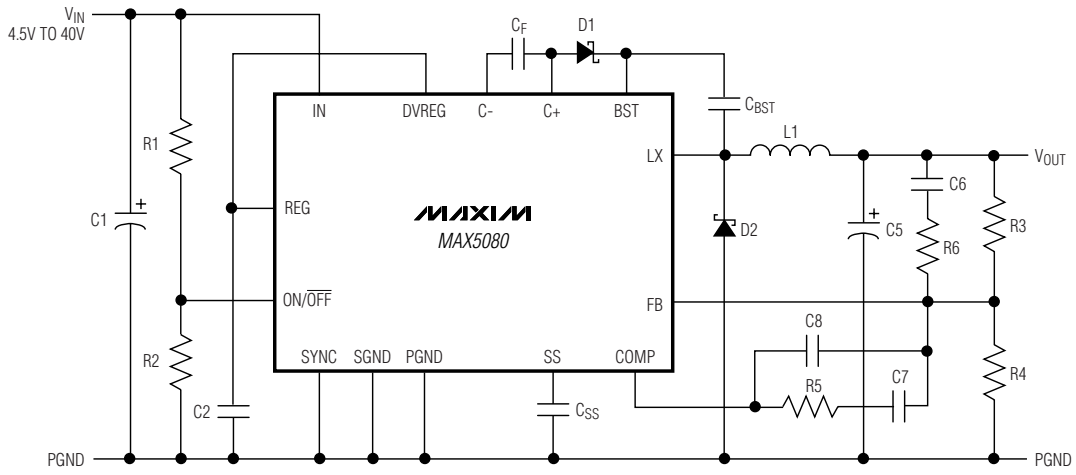
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5080ATE	-40°C to +125°C	16 TQFN-EP*	T1655-2
MAX5081ATE	-40°C to +125°C	16 TQFN-EP*	T1655-2

**EP = Exposed pad.*

Pin Configurations appear at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

1A, 40V, MAXPower Step-Down DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

IN, ON/$\overline{OFF}$ to SGND .....-0.3V to +45V
LX to SGND .....-0.3V to (V_{IN} + 0.3V)
BST to SGND .....-0.3V to (V_{IN} + 12V)
BST to LX .....-0.3V to +12V
PGND to SGND .....-0.3V to +0.3V
REG, DVREG, SYNC to SGND .....-0.3V to +12V
FB, COMP, SS to SGND .....-0.3V to (V_{REG} + 0.3V)
C+ to PGND (MAX5080 only) .....(V_{DVREG} - 0.3V) to +12V
C- to PGND (MAX5080 only) .....-0.3V to (V_{DVREG} + 0.3V)
Continuous current through internal power MOSFET (pins 11/12 connected together and pins 13/14 connected together)
T_J = +125°C 3A
T_J = +150°C 2A
Continuous Power Dissipation* (T_A = +70°C)
16-Pin TQFN (derate 33.3mW/°C above +70°C) ...2666.7mW
16-Pin TQFN (θ_{JA}) .....30°C/W
16-Pin TQFN (θ_{JC}) .....1.7°C/W
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
**As per JEDEC 51 Standard*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{ON/\overline{OFF}}$ = 12V, V_{REG} = V_{DVREG}, V_{SYNC} = PGND = SGND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A= + 25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	MAX5080	4.5		40	V
		MAX5081	7.5		40	
Undervoltage Lockout Threshold	UVLO	V_{IN} rising, MAX5080	3.9		4.2	V
		V_{IN} rising, MAX5081	6.8		7.3	
Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	MAX5080		0.4		V
		MAX5081		0.7		
Switching Supply Current (PWM Operation)	I_{SW}	V_{FB} = 0V, MAX5080		10.5		mA
		V_{FB} = 0V, MAX5081		9.5		
Efficiency		V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A		84		%
		V_{IN} = 4.5V, V_{OUT} = 3.3V, I_{OUT} = 1A (MAX5080)		88		
No-Load Supply Current (PFM Operation)		MAX5080		1.4	2.5	mA
		MAX5081		1.3	2.3	
Shutdown Current	I_{SHDN}	$V_{ON/\overline{OFF}}$ = 0V, V_{IN} = 40V		200	300	µA
ON/$\overline{OFF}$ CONTROL						
Input Voltage Threshold	$V_{ON/\overline{OFF}}$	$V_{ON/\overline{OFF}}$ rising	1.20	1.23	1.25	V
Input Voltage Hysteresis				0.12		V
Input Bias Current		$V_{ON/\overline{OFF}}$ = 0 to 40V	-250		+250	nA
ERROR AMPLIFIER/SOFT-START						
Soft-Start Current	I_{SS}		8	15	24	µA
Reference Voltage (Soft-Start)	V_{SS}		1.215	1.228	1.240	V
FB Regulation Voltage	V_{FB}	I_{COMP} = -500µA to +500µA	1.215	1.228	1.240	V
FB Input Range			0		1.5	V
FB Input Current			-250		+250	nA
COMP Voltage Range		I_{COMP} = -500µA to +500µA	0.25		4.50	V
Open-Loop Gain				80		dB
Unity-Gain Bandwidth				1.8		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{ON/\overline{OFF}}$ = 12V, V_{REG} = V_{DVREG}, V_{SYNC} = PGND = SGND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A= + 25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Offset Voltage		I_{COMP} = -500µA to +500µA	-5		+5	mV
OSCILLATOR						
Frequency	f_{SW}	V_{SYNC} = 0V	225	250	275	kHz
Maximum Duty Cycle	D_{MAX}	V_{SYNC} = 0V, V_{IN} = 4.5V, MAX5080	87			%
		V_{SYNC} = 0V, V_{IN} = 7.5V, MAX5081	87			
		V_{SYNC} = 0V, V_{IN} ≤ 40V	87			
SYNC High-Level Voltage			2.2			V
SYNC Low-Level Voltage					0.8	V
SYNC Frequency Range	f_{SYNC}		150		350	kHz
PWM Modulator Gain		f_{SYNC} = 150kHz to 350kHz		10		V/V
Ramp Level Shift (Valley)				0.3		V
POWER SWITCH						
Switch On-Resistance		V_{BST} - V_{LX} = 6V		0.3	0.6	Ω
Switch Gate Charge		V_{BST} - V_{LX} = 6V		6		nC
Switch Leakage Current		V_{IN} = 40V, V_{LX} = V_{BST} = 0V			10	µA
BST Leakage Current		V_{BST} = V_{LX} = V_{IN} = 40V			10	µA
CHARGE PUMP						
C- Output Voltage Low		MAX5080 only, sinking 10mA			0.1	V
C- Output Voltage High		MAX5080 only, relative to DVREG, sourcing 10mA			0.1	V
DVREG to C+ On-Resistance		MAX5080 only, sourcing 10mA			10	Ω
LX to PGND On-Resistance		Sinking 10mA			12	Ω
CURRENT-LIMIT COMPARATOR						
Pulse-Skip Threshold	I_{PFM}		100	200	300	mA
Cycle-by-Cycle Current Limit	I_{ILIM}		1.4	2	2.6	A
Number of Consecutive ILIM Events to Hiccup				7		
Hiccup Timeout				512		Clock periods
INTERNAL VOLTAGE REGULATOR						
Output Voltage	V_{REG}	MAX5080	4.75	5	5.25	V
		MAX5081	7.6	8	8.4	
Line Regulation		V_{IN} = 5.5V to 40V, MAX5080			1	mV/V
		V_{IN} = 9.0V to 40V, MAX5081			1	
Load Regulation		I_{REG} = 0 to 20mA			0.25	V
Dropout Voltage		V_{IN} = 4.5V, I_{REG} = 20mA, MAX5080			0.5	V
		V_{IN} = 7.5V, I_{REG} = 20mA, MAX5081			0.5	

1A, 40V, MAXPower Step-Down DC-DC Converters

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{ON/\overline{OFF}}$ = 12V, V_{REG} = V_{DVREG}, V_{SYNC} = PGND = SGND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A= + 25°C.) (Note 1)

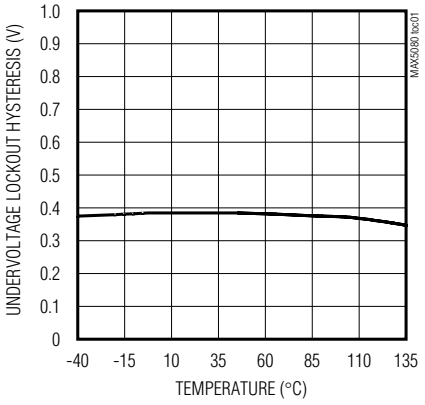
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		Temperature rising		+160		°C
Thermal Shutdown Hysteresis				20		°C

Note 1: 100% production tested at T_A = +25°C and T_A = T_J = +125°C. Limits at -40°C are guaranteed by design.

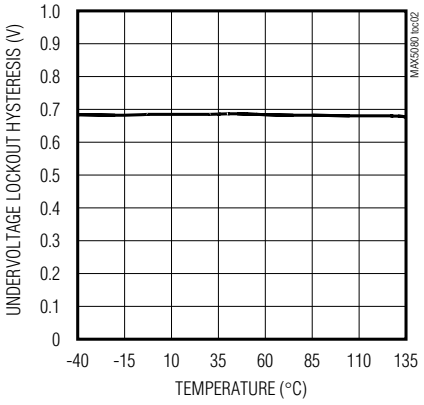
Typical Operating Characteristics

(V_{IN} = 12V, see Figure 5 (MAX5080) and Figure 6 (MAX5081), T_A = +25°C, unless otherwise noted.)

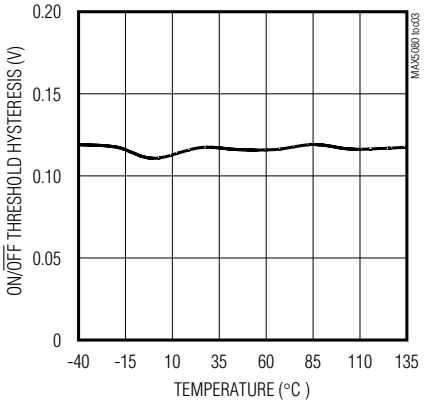
UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE (MAX5080)



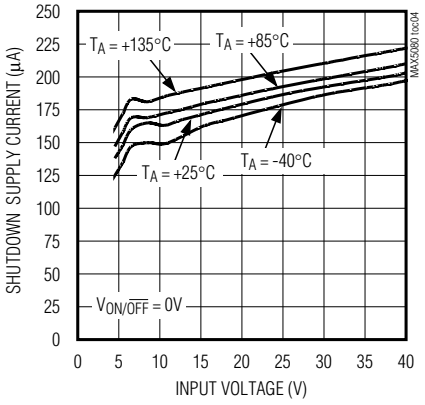
UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE (MAX5081)



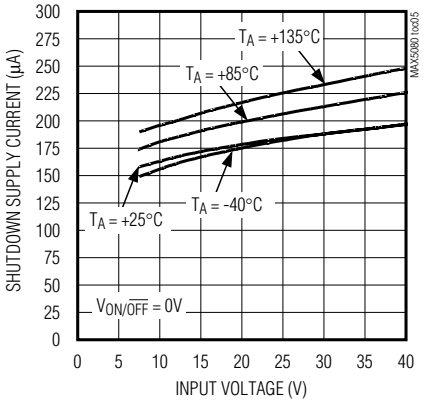
ON/$\overline{OFF}$ THRESHOLD HYSTERESIS vs. TEMPERATURE



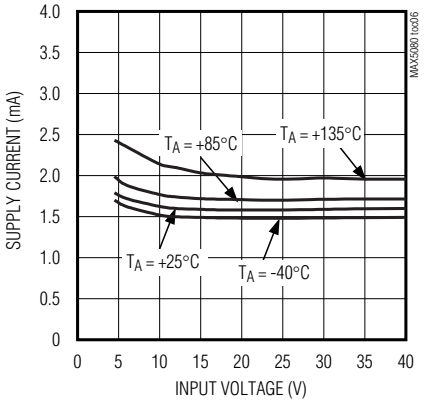
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5080)



SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5081)



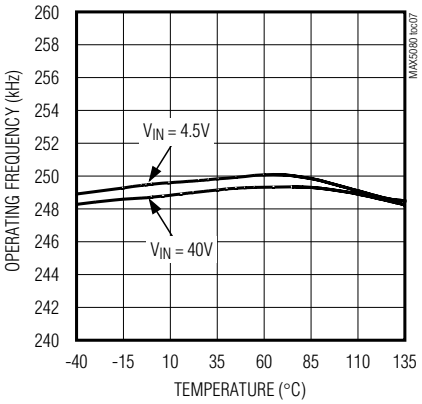
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5080)



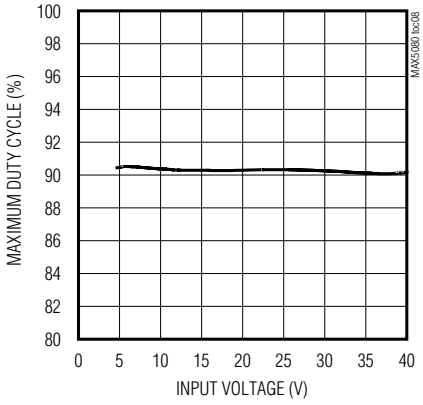
Typical Operating Characteristics (continued)

(V_{IN} = 12V, see Figure 5 (MAX5080) and Figure 6 (MAX5081), T_A = +25°C, unless otherwise noted.)

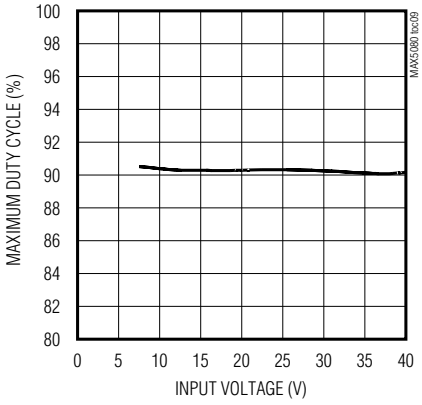
OPERATING FREQUENCY vs. TEMPERATURE



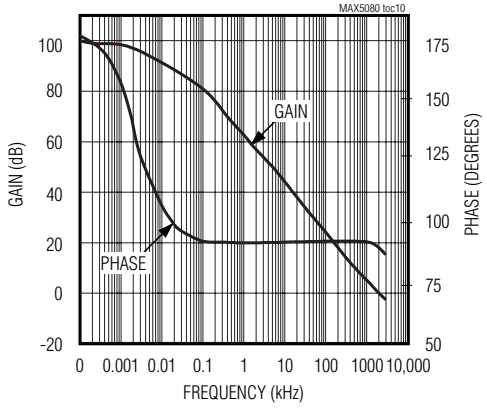
MAXIMUM DUTY CYCLE vs. INPUT VOLTAGE (MAX5080)



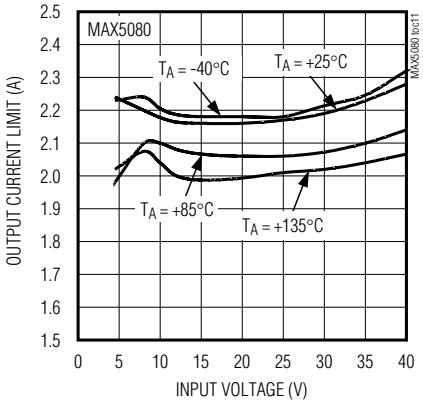
MAXIMUM DUTY CYCLE vs. INPUT VOLTAGE (MAX5081)



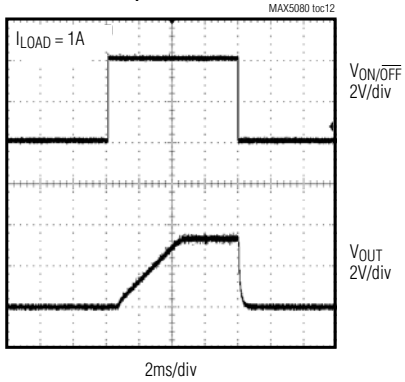
OPEN-LOOP GAIN/PHASE vs. FREQUENCY



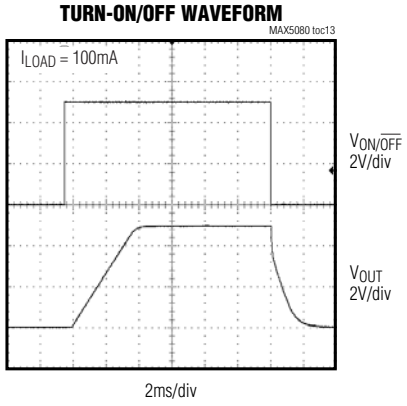
OUTPUT CURRENT LIMIT vs. INPUT VOLTAGE



TURN-ON/OFF WAVEFORM



TURN-ON/OFF WAVEFORM

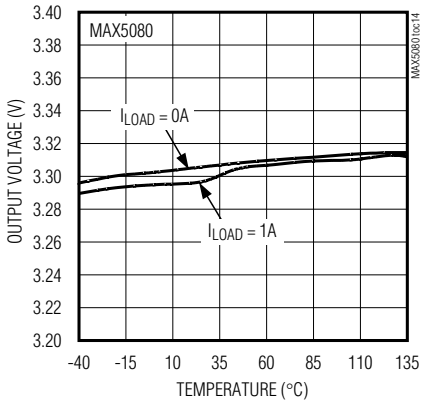


1A, 40V, MAXPower Step-Down DC-DC Converters

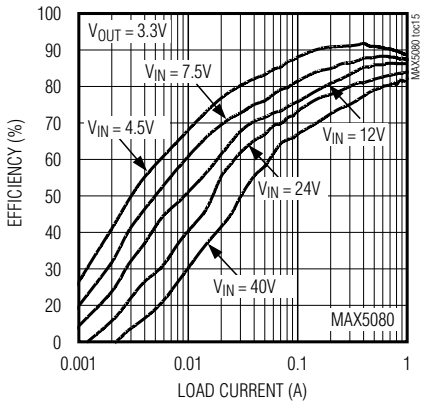
Typical Operating Characteristics (continued)

(V_{IN} = 12V, see Figure 5 (MAX5080) and Figure 6 (MAX5081), T_A = +25°C, unless otherwise noted.)

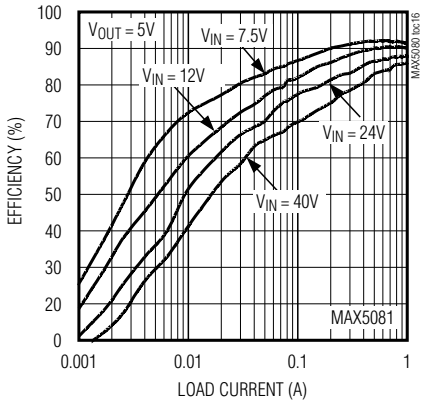
OUTPUT VOLTAGE vs. TEMPERATURE



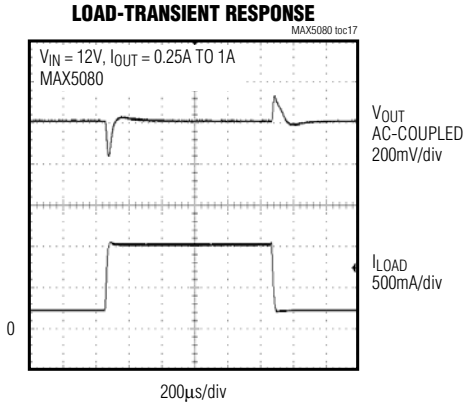
EFFICIENCY vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT



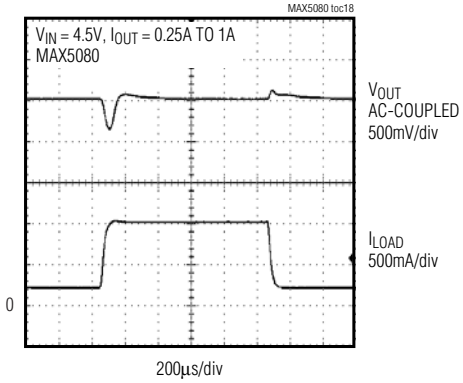
LOAD-TRANSIENT RESPONSE



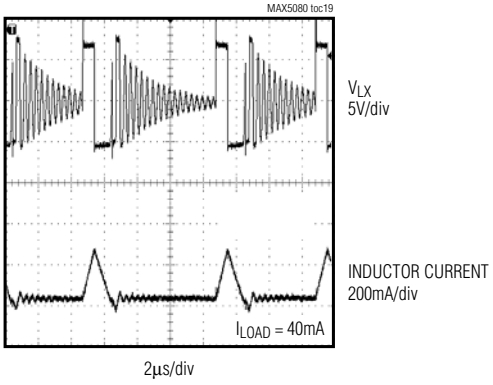
Typical Operating Characteristics (continued)

(V_{IN} = 12V, see Figure 5 (MAX5080) and Figure 6 (MAX5081), T_A = +25°C, unless otherwise noted.)

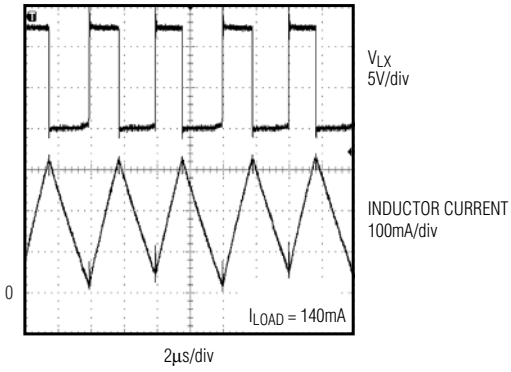
LOAD-TRANSIENT RESPONSE



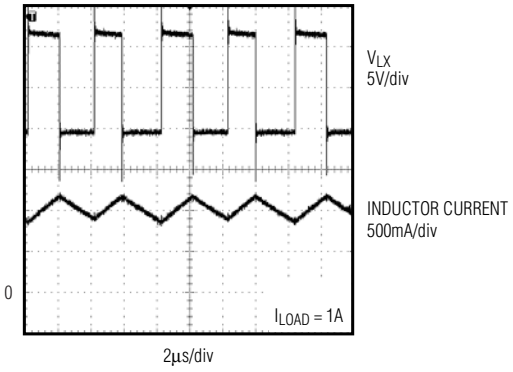
LX VOLTAGE AND INDUCTOR CURRENT



LX VOLTAGE AND INDUCTOR CURRENT



LX VOLTAGE AND INDUCTOR CURRENT



1A, 40V, MAXPower Step-Down DC-DC Converters

Pin Description

PIN		NAME	FUNCTION
MAX5080	MAX5081		
1	1	COMP	Error Amplifier Output. Connect COMP to the compensation feedback network.
2	2	FB	Feedback Regulation Point. Connect to the center tap of a resistive divider from converter output to SGND to set the output voltage. The FB voltage regulates to the voltage present at SS (1.23V).
3	3	ON/$\overline{OFF}$	ON/$\overline{OFF}$ and External UVLO Control. The ON/$\overline{OFF}$ rising threshold is set to approximately 1.23V. Connect to the center tap of a resistive divider from IN to SGND to set the UVLO (rising) threshold. Pull ON/$\overline{OFF}$ to SGND to shut down the device. ON/$\overline{OFF}$ can be used for power-supply sequencing. Connect to IN for always-on operation.
4	4	SS	Soft-Start and Reference Output. Connect a capacitor from SS to SGND to set the soft-start time. See the *Applications Information* section to calculate the value of the CSS capacitor.
5	5	SYNC	Oscillator Synchronization Input. SYNC can be driven by an external 150kHz to 350kHz clock to synchronize the MAX5080/MAX5081's switching frequency. Connect SYNC to SGND when not used.
6	6	DVREG	Gate Drive Supply for High-Side MOSFET Driver. Connect externally to REG for MAX5080. Connect to REG and the anode of the boost diode for MAX5081.
7	—	C+	Charge-Pump Flying Capacitor Positive Connection
8	—	C-	Charge-Pump Flying Capacitor Negative Connection
—	7, 8	N.C.	No Connection. Not internally connected. Can be left floating or connected to SGND.
9	9	PGND	Power Ground Connection. Connect the input filter capacitor's negative terminal, the anode of the freewheeling diode, and the output filter capacitor's return to PGND. Connect externally to SGND at a single point near the input capacitor's return terminal.
10	10	BST	High-Side Gate Driver Supply. Connect BST to the cathode of the boost diode and to the positive terminal of the boost capacitor.
11, 12	11, 12	LX	Source Connection of Internal High-Side Switch. Connect the inductor and rectifier diode's cathode to LX.
13, 14	13, 14	IN	Supply Input Connection. Connect to an external voltage source from 4.5V to 40V (MAX5080) or a 7.5V to 40V (MAX5081).
15	15	REG	Internal Regulator Output. 5V output for the MAX5080 and 8V output for the MAX5081. Bypass to SGND with at least a 1µF ceramic capacitor.
16	16	SGND	Signal Ground Connection. Solder the exposed pad to a large SGND plane. Connect SGND and PGND together at one point near the input bypass capacitor return terminal.
EP	EP	EP	Exposed Pad. Connect exposed pad to SGND.

Detailed Description

The MAX5080/MAX5081 are voltage-mode buck converters with internal 0.3Ω power MOSFET switches. The MAX5080 has a wide input voltage range of 4.5V to 40V. The MAX5081's input voltage range is 7.5V to 40V. The internal low R_{DS_ON} switch allows for up to 1A of output current. The 250kHz fixed switching frequency, external compensation, and voltage feed-forward simplify loop compensation design and allow for a variety of L and C filter components. Both devices offer an automatic switchover to pulse-skipping (PFM) mode, providing low quiescent current and high efficiency at light loads. Under no load, a PFM mode operation reduces the current consumption to only 1.4mA. In shutdown, the supply current falls to 200µA. Additional features include an externally programmable undervoltage lockout through the ON/$\overline{OFF}$ pin, a programmable soft-start, cycle-by-cycle current limit, hiccup mode output short-circuit protection, and thermal shutdown.

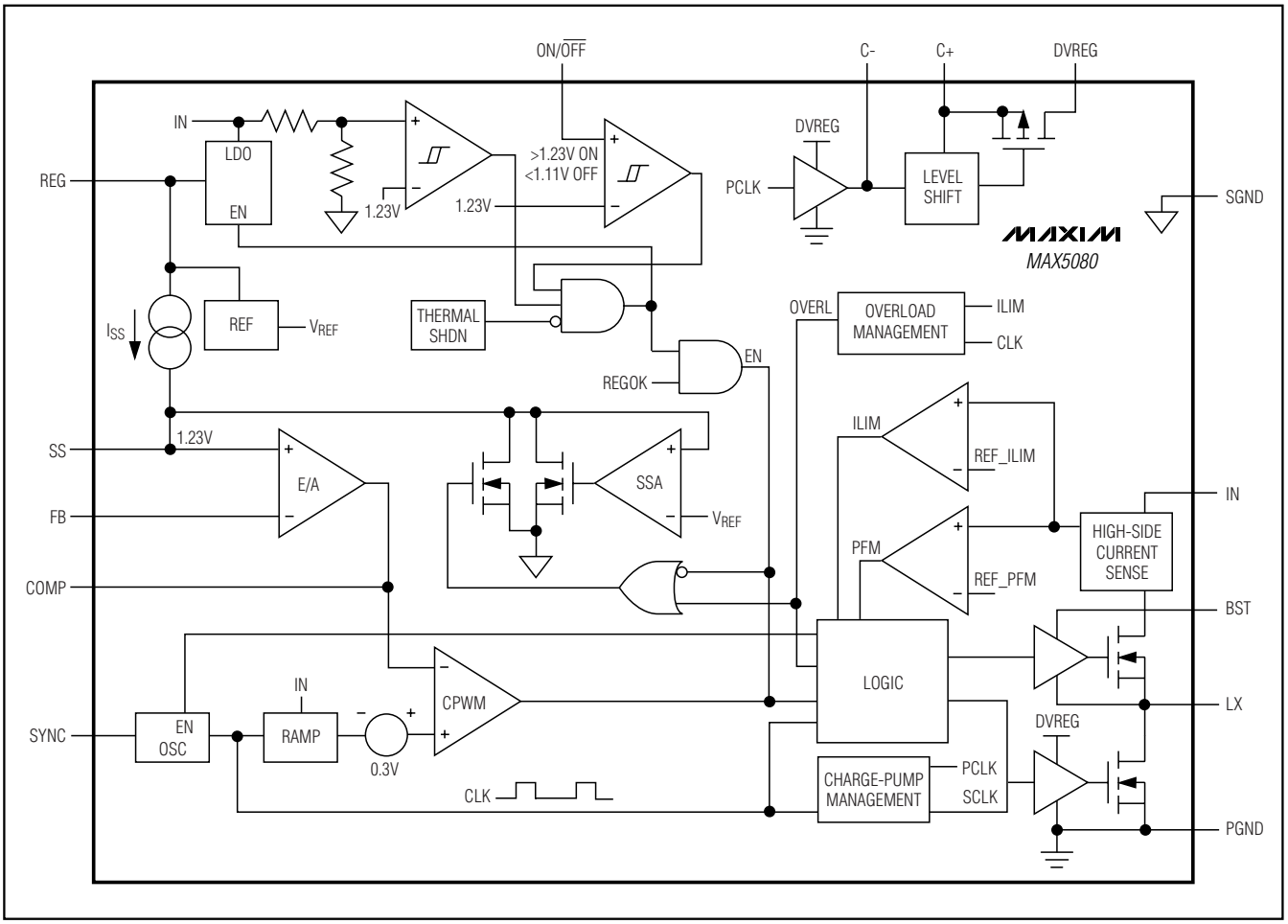


Figure 1. MAX5080 Simplified Block Diagram

Internal Linear Regulator (REG)

REG is the output terminal of a 5V (MAX5080), or 8V (MAX5081) LDO which is powered from IN and provides power to the IC. Connect REG externally to DVREG to provide power for the high-side MOSFET gate driver. Bypass REG to SGND with a ceramic capacitor of at least 1µF. Place the capacitor physically close to the MAX5080/MAX5081 to provide good bypassing. During normal operation, REG is intended for powering up only the internal circuitry and should not be used to supply power to external loads.

Internal UVLO/External UVLO

The MAX5080/MAX5081 provides two undervoltage lockouts (UVLOs). An internal UVLO looks at the input voltage (V_{IN}) and is fixed at 4.1V (MAX5080) or 7.1V (MAX5081). An external UVLO is sensed and programmed at the ON/$\overline{OFF}$ pin. The external UVLO overrides the internal UVLO when the external UVLO is higher than the internal UVLO. During startup, before any operation begins, the input voltage and the voltage at ON/$\overline{OFF}$ must exceed their respective UVLOs. The external UVLO has a rising threshold of 1.23V with 0.12V of hysteresis. Program the external UVLO by connecting a resistive divider from IN to ON/$\overline{OFF}$ to SGND. Connect ON/$\overline{OFF}$ to IN directly to disable the external UVLO.

Driving ON/$\overline{OFF}$ to ground places the MAX5080/MAX5081 in shutdown. When in shutdown the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to 200µA. Connect an RC network from ON/$\overline{OFF}$ to SGND to set a turn-on delay that can be used to sequence the output voltages of multiple devices.

1A, 40V, MAXPower Step-Down DC-DC Converters

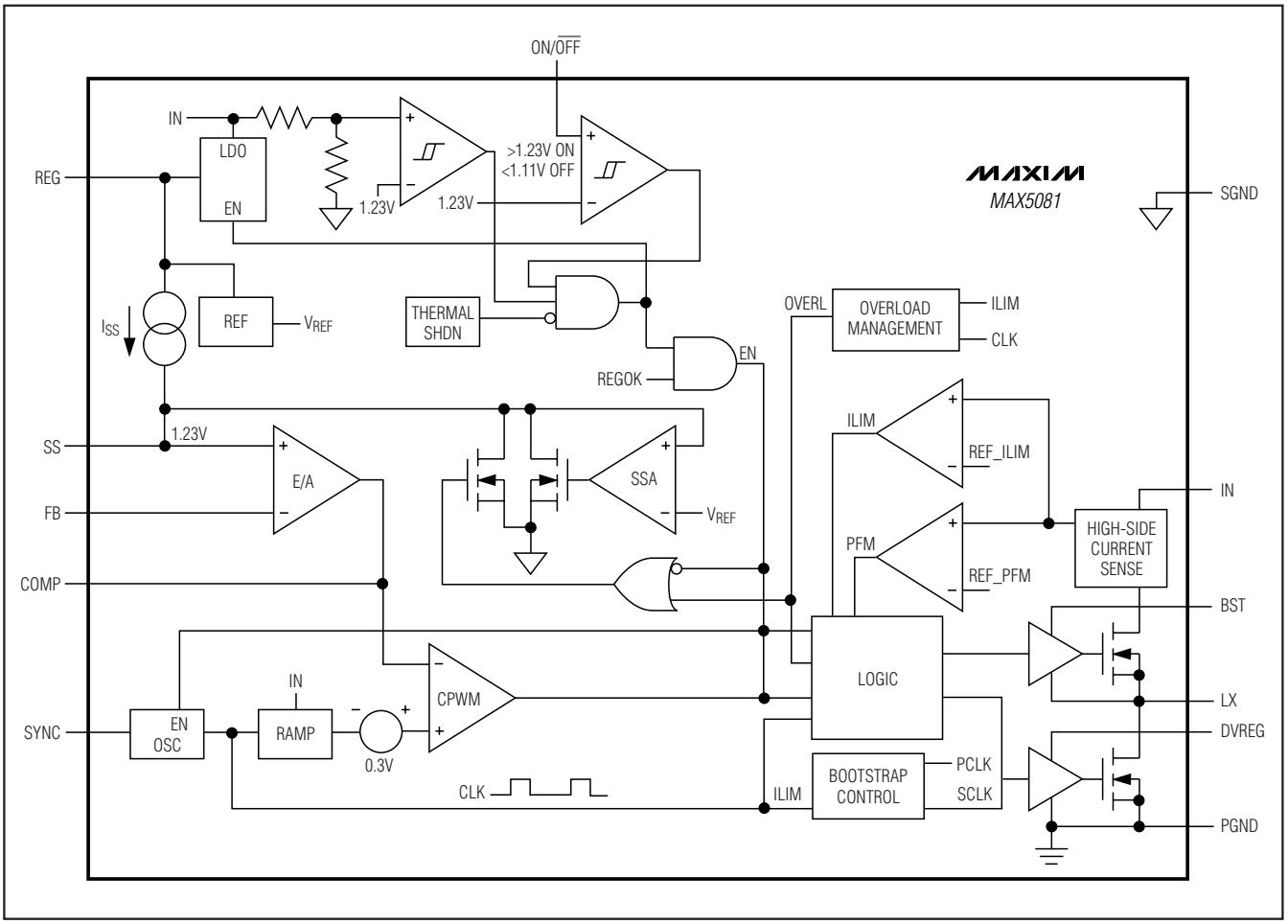


Figure 2. MAX5081 Simplified Block Diagram

Soft-Start and Reference (SS)

SS is the 1.23V reference bypass connection for the MAX5080/MAX5081 and also controls the soft-start period. At startup, after V_{IN} is applied and the internal and external UVLO thresholds are reached, the device enters soft-start. During soft-start, 15µA is sourced into the capacitor (C_{SS}) connected from SS to SGND causing the reference voltage to ramp up slowly. When V_{SS} reaches 1.23V the output becomes fully active. Set the soft-start time (t_{SS}) using following equation:

$$t_{SS} = \frac{1.23V \times C_{SS}}{15\mu A}$$

where t_{SS} is in seconds and C_{SS} is in Farads.

Internal Charge Pump (MAX5080)

The MAX5080 features an internal charge pump to enhance the turn-on of the internal MOSFET, allowing for operation with input voltages down to 4.5V. Connect a flying capacitor (C_F) between C+ and C-, a boost diode from C+ to BST, as well as a bootstrap capacitor (C_{BST}) between BST and LX to provide the gate drive voltage for the high-side n-channel DMOS switch. During the on-time, the flying capacitor is charged to V_{DVREG}. During the off-time, the positive terminal of the flying capacitor (C+) is pumped to two times V_{DVREG} and charge is dumped onto C_{BST} to provide twice the regulator voltage across the high-side DMOS driver. Use a ceramic capacitor of at least 0.1µF for C_{BST} and C_F located as close to the device as possible.

For applications that do not require a 4.5V minimum input, use the MAX5081. In this device the charge pump is omitted and the input voltage range is from 7.5V to 40V. In this situation the boost diode and the boost capacitor are still required (see the *MAX5081 Typical Operating Circuit*).

Gate Drive Supply (DVREG)

DVREG is the supply input for the internal high-side MOSFET driver. The power for DVREG is derived from the output of the internal regulator (REG). Connect DVREG to REG externally. We recommend the use of an RC filter (1Ω and 0.47µF) from REG to DVREG to filter the noise generated by the switching of the charge pump. In the MAX5080, the high-side drive supply is generated using the internal charge pump along with the bootstrap diode and capacitor. In the MAX5081, the high-side MOSFET driver supply is generated using only the bootstrap diode and capacitor.

Error Amplifier

The output of the internal error amplifier (COMP) is available for frequency compensation (see the *Compensation Design* section). The inverting input is FB, the noninverting input SS, and the output COMP. The error amplifier has an 80dB open-loop gain and a 1.8MHz GBW product. See the *Typical Operating Character-istics* for the Gain and Phase vs. Frequency graph.

Oscillator/Synchronization Input (SYNC)

With SYNC tied to SGND, the MAX5080/MAX5081 use their internal oscillator and switch at a fixed frequency of 250kHz. For external synchronization, drive SYNC with an external clock from 150kHz to 350kHz. When driven with an external clock, the device synchronizes to the rising edge of SYNC.

PWM Comparator/Voltage Feedforward

An internal 250kHz ramp generator is compared against the output of the error amplifier to generate the PWM signal. The maximum amplitude of the ramp (V_{RAMP}) automatically adjusts to compensate for input voltage and oscillator frequency changes. This causes the V_{IN}/V_{RAMP} to be a constant 10V/V across the input voltage range of 4.5V to 40V (MAX5080) or 7.5V to 40V (MAX5081) and the SYNC frequency range of 150kHz to 350kHz.

Output Short-Circuit Protection (Hiccup Mode)

The MAX5080/MAX5081 protects against an output short circuit by utilizing hiccup-mode protection. In hiccup mode, a series of sequential cycle-by-cycle current-limit events will cause the part to shut down and restart with a soft-start sequence. This allows the device to operate with a continuous output short circuit.

During normal operation, the current is monitored at the drain of the internal power MOSFET. When the current limit is exceeded, the internal power MOSFET turns off until the next on-cycle and a counter increments. If the counter counts seven consecutive current-limit events, the device discharges the soft-start capacitor and shuts down for 512 clock periods before restarting with a soft-start sequence. Each time the power MOSFET turns on and the device does not exceed the current limit, the counter is reset.

Thermal-Overload Protection

The MAX5080/MAX5081 feature an integrated thermal-overload protection. Thermal-overload protection limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C, an internal thermal sensor shuts down the part, turning off the power MOSFET and allowing the IC to cool. After the temperature falls by 20°C, the part will restart with a soft-start sequence.

Applications Information

Setting the Undervoltage Lockout

When the voltage at ON/$\overline{OFF}$ rises above 1.23V, the MAX5080/MAX5081 turns on. Connect a resistive divider from IN to ON/$\overline{OFF}$ to SGND to set the UVLO threshold (see Figure 5). First select the ON/$\overline{OFF}$ to the SGND resistor (R2) then calculate the resistor from IN to ON/$\overline{OFF}$ (R1) using the following equation:

$$R1 = R2 \times \left[\frac{V_{IN}}{V_{ON/\overline{OFF}}} - 1 \right]$$

where V_{IN} is the input voltage at which the converter turns on, $V_{ON/\overline{OFF}}$ = 1.23V and R2 is chosen to be less than 600kΩ.

If the external UVLO divider is not used, connect ON/$\overline{OFF}$ to IN directly. In this case, an internal undervoltage lockout feature monitors the supply voltage at IN and allows operation to start when IN rises above 4.1V (MAX5080) and 7.1V (MAX5081).

Setting the Output Voltage

Connect a resistive divider from OUT to FB to SGND to set the output voltage. First calculate the resistor from OUT to FB using the guidelines in the *Compensation Design* section. Once R3 is known, calculate R4 using the following equation:

$$R4 = \frac{R3}{\left[\frac{V_{OUT}}{V_{FB}} - 1\right]}$$

where V_{FB} = 1.23V.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5080/MAX5081: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value while a lower ΔI_{P-P} requires a higher inductor value. A lower inductor value minimizes size and cost and improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_{P-P} equal to 40% of the full load current. Calculate the inductor using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is fixed at 250kHz or can vary between 150kHz and 350kHz when synchronized to an external clock (see the *Oscillator/Synchronization Input (SYNC)* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturating current (I_{SAT}) is also important to avoid runaway current during continuous output short circuit. Select an inductor with an I_{SAT} specification higher than the maximum peak current limit of 2.6A.

Input Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents and therefore the input capacitor must be carefully chosen to keep the input voltage ripple within design requirements. The input voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{OUT\_MAX} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT\_MAX} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

I_{OUT_MAX} is the maximum output current, D is the duty cycle, and f_{SW} is the switching frequency.

The MAX5080/MAX5081 includes internal and external UVLO hysteresis and soft-start to avoid possible unintentional chattering during turn-on. However, use a bulk capacitor if the input source impedance is high. Use enough input capacitance at lower input voltages to avoid possible undershoot below the undervoltage lockout threshold during transient loading.

Output Capacitor Selection

The allowable output voltage ripple and the maximum deviation of the output voltage during load steps determine the output capacitance and its ESR. The output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the equivalent series resistance of the output capacitor). The equations for calculating the peak-to-peak output voltage ripple are:

$$\Delta V_Q = \frac{\Delta I_{PP}}{16 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = ESR \times \Delta I_{P-P}$$

Normally, a good approximation of the output voltage ripple is $\Delta V_{RIPPLE} \approx \Delta V_{ESR} + \Delta V_Q$. If using ceramic capacitors, assume the contribution to the output voltage ripple from ESR and the capacitor discharge to be

equal to 20% and 80%, respectively. ΔI_{P-P} is the peak-to-peak inductor current (see the *Input Capacitors Selection* section) and f_{SW} is the converter's switching frequency.

The allowable deviation of the output voltage during fast load transients also determines the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation Design* section). The resistive drop across the output capacitors ESR, the drop across the capacitors ESL (ΔV_{ESL}), and the capacitor discharge causes a voltage droop during the load-step. Use a combination of low-ESR tantalum/aluminum electrolyte and ceramic capacitors for better transient load and voltage ripple performance. Nonleaded capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output voltage deviation below the tolerable limits of the electronics being powered. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, and $t_{RESPONSE}$ is the response time of the controller.

Compensation Design

The MAX5080/MAX5081 use a voltage-mode control scheme that regulates the output voltage by comparing the error amplifier output (COMP) with an internal ramp to produce the required duty cycle. The output lowpass LC filter creates a double pole at the resonant frequency, which has a gain drop of -40dB/decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback divider, and a voltage error amplifier. The power modulator has a DC gain set by V_{IN}/V_{RAMP}, with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}) (C5 in the *Typical Application Circuit*) and its equivalent series resistance (ESR). The power modulator incorporates a voltage feed-forward feature, which automatically adjusts for variations in the input voltage resulting in a DC gain of 10. The following equations define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}} = 10$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

$$f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The switching frequency is internally set at 250kHz or can vary from 150kHz to 350kHz when driven with an external SYNC signal. The crossover frequency (f_C), which is the frequency when the closed-loop gain is equal to unity, should be set at 15kHz or below therefore:

$$f_C \le 15kHz$$

The error amplifier must provide a gain and phase bump to compensate for the rapid gain and phase loss from the LC double pole. This is accomplished by utilizing a type 3 compensator that introduces two zeroes and 3 poles into the control loop. The error amplifier has a low-frequency pole (f_{P1}) near the origin.

The two zeros are at:

$$f_{Z1} = \frac{1}{2\pi \times R5 \times C7} \text{ and } f_{Z2} = \frac{1}{2\pi \times (R6 + R3) \times C6}$$

and the higher frequency poles are at:

$$f_{P2} = \frac{1}{2\pi \times R6 \times C6} \text{ and } f_{P3} = \frac{1}{2\pi \times R5 \times \left(\frac{C7 \times C8}{C7 + C8}\right)}$$

Compensation When $f_C < f_{ZESR}$

Figure 3 shows the error amplifier feedback as well as its gain response for circuits that use low-ESR output capacitors (ceramic). In this case f_{ZESR} occurs after f_C.

f_{Z1} is set to 0.8 x $f_{LC(MOD)}$ and f_{Z2} is set to f_{LC} to compensate for the gain and phase loss due to the double pole. Choose the inductor (L) and output capacitor (C_{OUT}) as described in the *Inductor and Output Capacitor Selection* section.

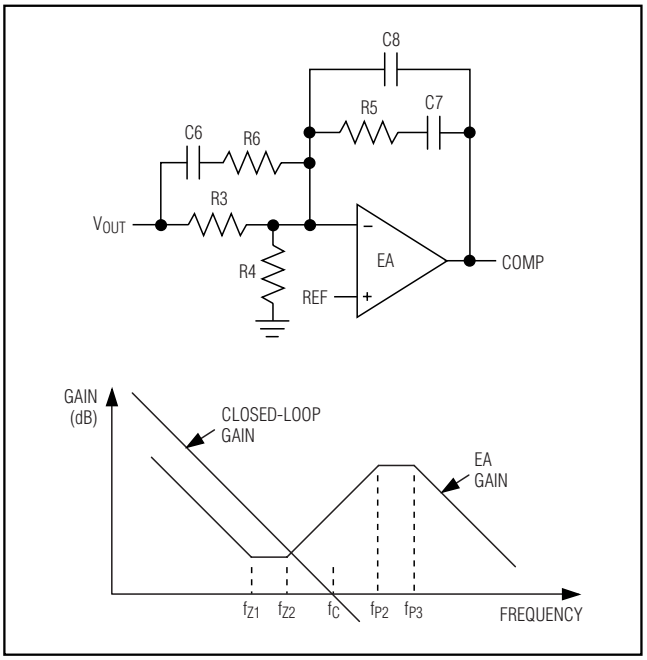


Figure 3. Error Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Ceramic Capacitors

Pick a value for the feedback resistor R5 in Figure 3 (values between 1kΩ and 10kΩ are adequate).

C7 is then calculated as:

$$C7 = \frac{1}{2\pi \times 0.8 \times f_{LC} \times R5}$$

f_C occurs between f_{Z2} and f_{P2}. The error-amplifier gain (G_{EA}) at f_C is due primarily to C6 and R5. Therefore, $G_{EA(fC)} = 2\pi \times f_C \times C6 \times R5$ and the modulator gain at f_C is:

$$G_{MOD(fC)} = \frac{G_{MOD(DC)}}{(2\pi)^2 \times L \times C_{OUT} \times f_C^2}$$

Since $G_{EA(fC)} \times G_{MOD(fC)} = 1$, C6 is calculated by:

$$C6 = \frac{f_C \times L \times C_{OUT} \times 2\pi}{R5 \times G_{MOD(DC)}}$$

f_{P2} is set at 1/2 the switching frequency (f_{SW}). R6 is then calculated by:

$$R6 = \frac{1}{2\pi \times C6 \times 0.5 \times f_{SW}}$$

Since R3 >> R6, R3 + R6 can be approximated as R3. R3 is then calculated as:

$$R3 \approx \frac{1}{2\pi \times f_{LC} \times C6}$$

f_{P3} is set at 5xf_C. Therefore C8 is calculated as:

$$C8 = \frac{C7}{(2\pi \times C7 \times R5 \times f_{P3} - 1)}$$

Compensation When $f_C > f_{ZESR}$

For larger ESR capacitors such as tantalum and aluminum electrolytic ones, f_{ZESR} can occur before f_C. If $f_{ZESR} < f_C$, then f_C occurs between f_{P2} and f_{P3}. f_{Z1} and f_{Z2} remain the same as before however, f_{P2} is now set equal to f_{ZESR}. The output capacitor's ESR zero frequency is higher than f_{LC} but lower than the closed-loop crossover frequency. The equations that define the error amplifier's poles and zeroes (f_{Z1}, f_{Z2}, f_{P1}, f_{P2}, and f_{P3}) are the same as before. However, f_{P2} is now lower than the closed-loop crossover frequency. Figure 4 shows the error amplifier feedback as well as its gain response for circuits that use higher-ESR output capacitors (tantalum or aluminum electrolytic).

Pick a value for the feedback resistor R5 in Figure 4 (values between 1kΩ and 10kΩ are adequate).

C7 is then calculated as:

$$C7 = \frac{1}{2\pi \times 0.8 \times f_{LC} \times R5}$$

The error amplifier gain between f_{P2} and f_{P3} is approximately equal to R5/R6 (given that R6 << R3). R6 can then be calculated as:

$$R6 \approx \frac{R5 \times 10 \times f_{LC}^2}{f_C^2}$$

C6 is then calculated as:

$$C6 = \frac{C_{OUT} \times ESR}{R6}$$

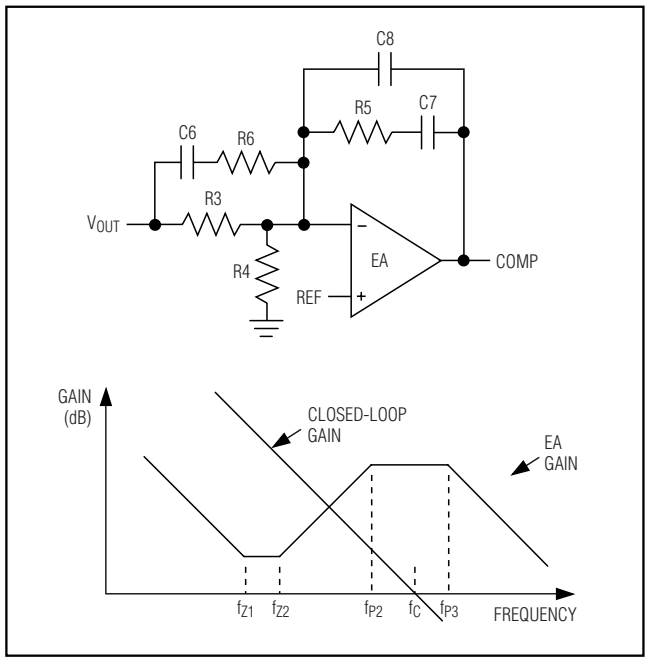


Figure 4. Error Amplifier Compensation Circuit (Closed-Loop and Error Amplifier Gain Plot) for Higher ESR Output Capacitors

Since R3 >> R6, R3 + R6 can be approximated as R3. R3 is then calculated as:

$$R3 \approx \frac{1}{2\pi \times f_{LC} \times C6}$$

f_{P3} is set at 5xf_C. Therefore, C8 is calculated as:

$$C8 = \frac{C7}{(2\pi \times C7 \times R5 \times f_{P3} - 1)}$$

Power Dissipation

The MAX5080/MAX5081 is available in a thermally enhanced package and can dissipate up to 2.7W at T_A = +70°C. When the die temperature reaches +160°C, the part shuts down and is allowed to cool. After the parts cool by 20°C, the device restarts with a soft-start.

The power dissipated in the device is the sum of the power dissipated from supply current (P_Q), transition losses due to switching the internal power MOSFET (P_{SW}), and the power dissipated due to the RMS current through the internal power MOSFET (P_{MOSFET}). The total power dissipated in the package must be limited such that the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature. Calculate the power lost in the MAX5080/MAX5081 using the following equations:

The power loss through the switch:

$$P_{MOSFET} = I_{RMS\_MOSFET}^2 \times R_{ON}$$

$$I_{RMS\_MOSFET} = \sqrt{\left[I^2_{PK} + (I_{PK} \times I_{DC}) + I^2_{DC}\right] \times \frac{D}{3}}$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_{P-P}}{2}$$

$$I_{DC} = I_{OUT} - \frac{\Delta I_{P-P}}{2}$$

R_{ON} is the on-resistance of the internal power MOSFET (see *Electrical Characteristics*).

The power loss due to switching the internal MOSFET:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_R \times t_F) \times f_{SW}}{4}$$

where t_R and t_F are the rise and fall times of the internal power MOSFET measured at LX.

The power loss due to the switching supply current (I_{SW}):

$$P_Q = V_{IN} \times I_{SW}$$

The total power dissipated in the device will be:

$$P_{TOTAL} = P_{MOSFET} + P_{SW} + P_Q$$

Chip Information

TRANSISTOR COUNT: 4300

PROCESS: BiCMOS/DMOS

Typical Application Circuits

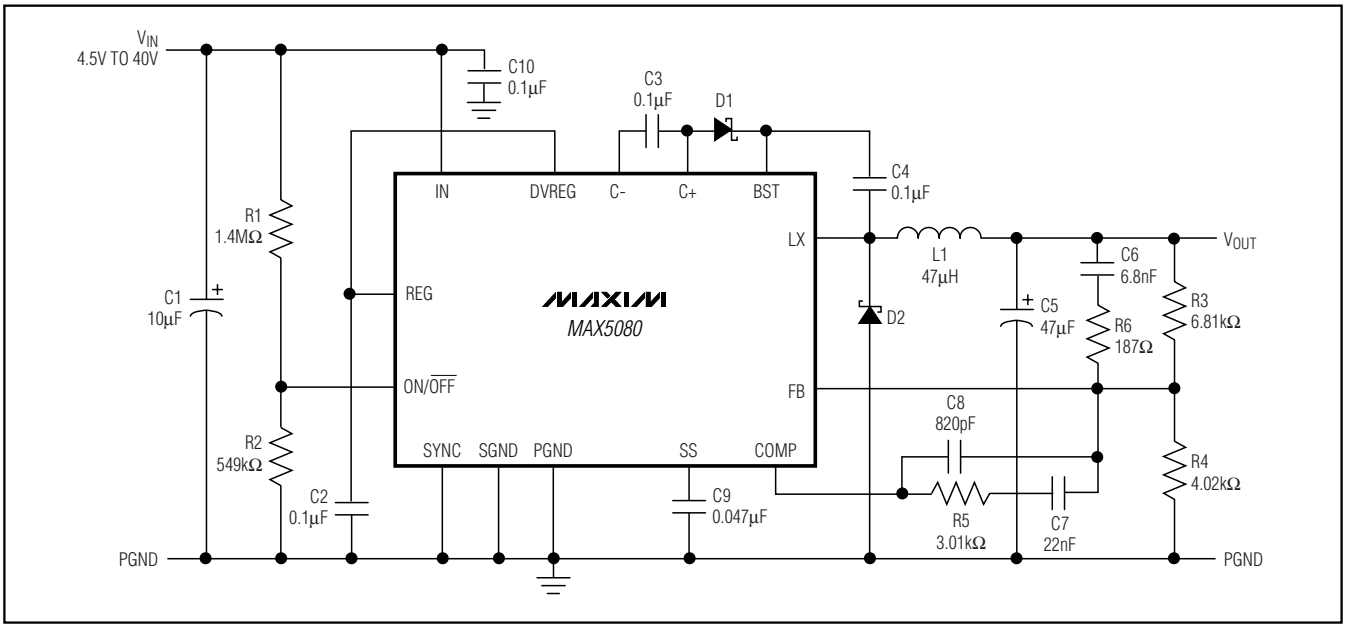


Figure 5. MAX5080 Typical Application Circuit

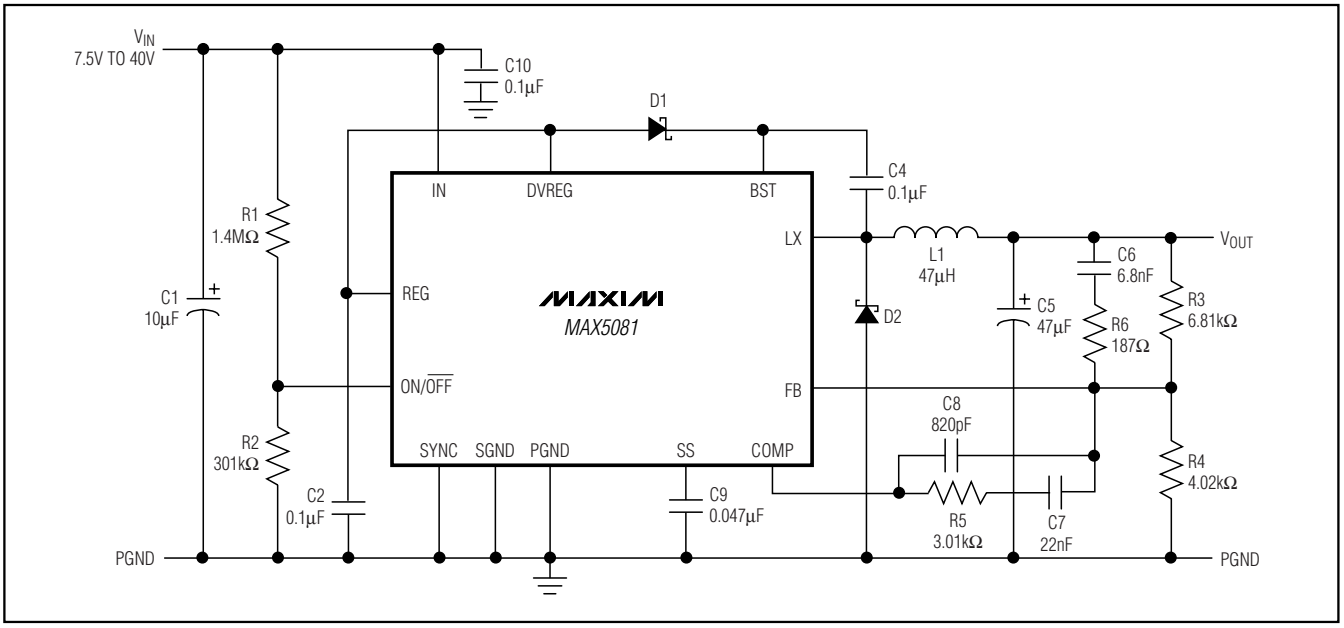
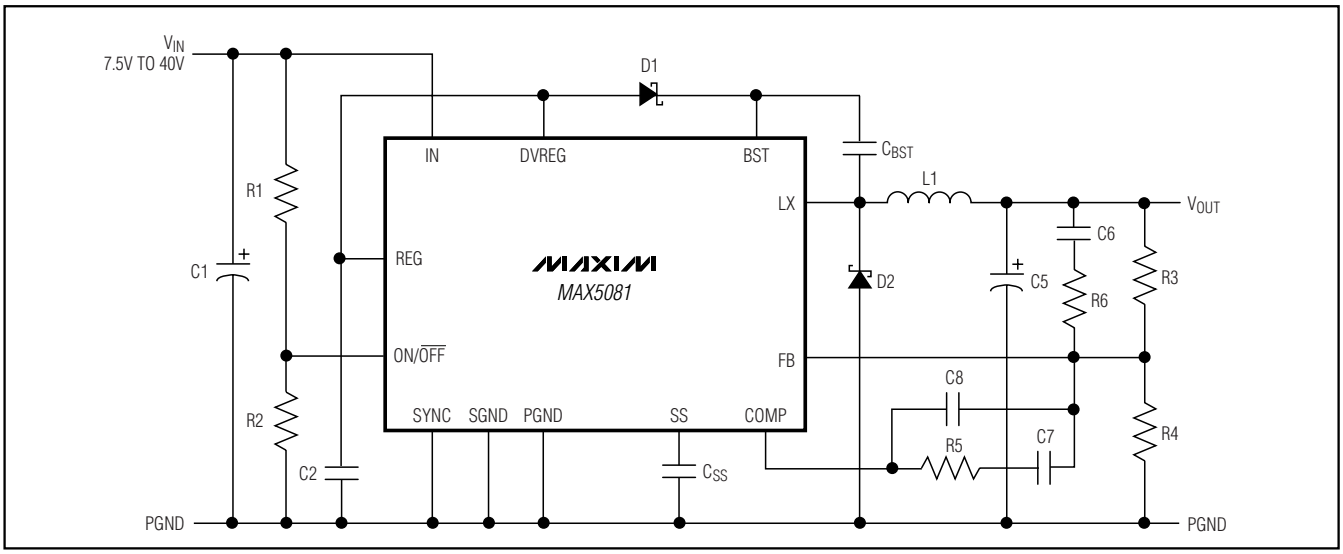
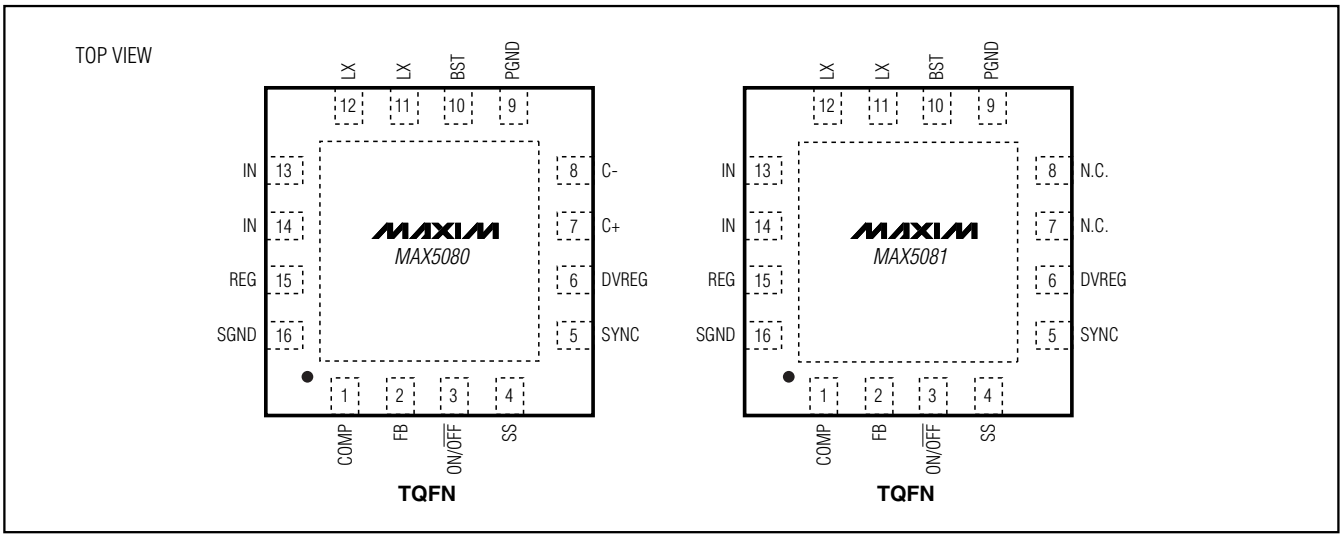


Figure 6. MAX5081 Typical Application Circuit

Typical Operating Circuits (continued)



Pin Configurations

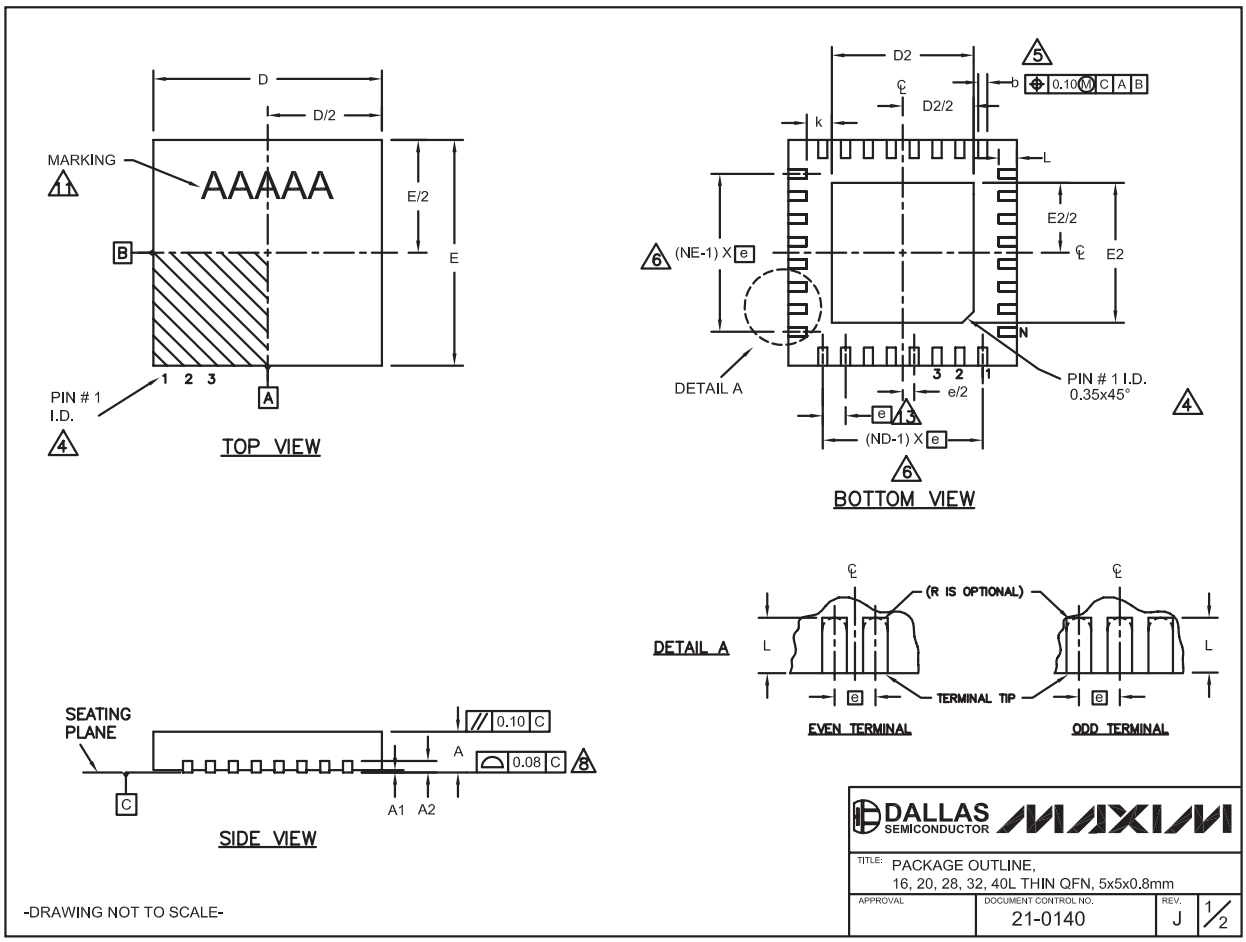


1A, 40V, MAXPower Step-Down DC-DC Converters

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			—			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	J	2/2

Revision History

Pages changed at Rev 1: 1, 8, 18, 19

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