QUALITY SEMICONDUCTOR, INC.

Low Skew PLL Clock Driver
TurboClock™ Jr.

QS59910
QS59920

FEATURES/BENEFITS

- 8 zero delay outputs
- Selectable positive or negative edge synchronization
- Synchronous output enable
- Output frequency: 15MHz to 110MHz
- QS599x0 family provides following products:
  QS59910: TTL outputs
  QS59920: CMOS outputs
- 3 skew grades:
  QS599x0-2: t_{SKEW0} < 250ps
  QS599x0-5: t_{SKEW0} < 500ps
  QS599x0-7: t_{SKEW0} < 750ps
- 3-level input for PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 46mA I_{OL} high drive outputs
- Low Jitter: < 200ps peak-to-peak
- Outputs drive 50Ω terminated lines
- Pin compatible with Cypress CY7B9910 and CY7B9920
- Industrial temperature range
- Available in SOIC (SO) package

DESCRIPTION

The QS59910 and QS59920 are high fanout phase lock loop clock drivers intended for high performance computing and data-communications applications. The QS59910 has 8 zero delay TTL outputs while the QS59920 has CMOS outputs.

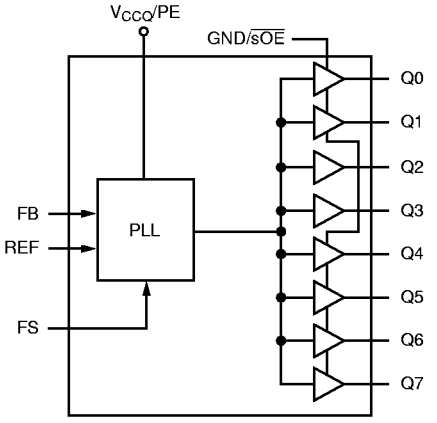
The QS599X0 family maintains Cypress CY7B99X0 compatibility while providing two additional features: Synchronous Output Enable (GND/$\overline{sOE}$), and Positive/Negative Edge Synchronization (V_{CCQ}/PE). When the GND/$\overline{sOE}$ pin is held low, all the outputs are synchronously enabled (CY7B99X compatibility). However, if GND/$\overline{sOE}$ is held high, all the outputs except Q2 and Q3 are synchronously disabled.

Furthermore, when the V_{CCQ}/PE is held high, all the outputs are synchronized with the positive edge of the REF clock input (CY7B99X0 compatibility). When V_{CCQ}/PE is held low, all the outputs are synchronized with the negative edge of REF.

The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

Figure 1. QS59910, QS59920: Logic Block Diagram



Fiure 2. Pin Configuration

(All Pins Top View)

SOIC

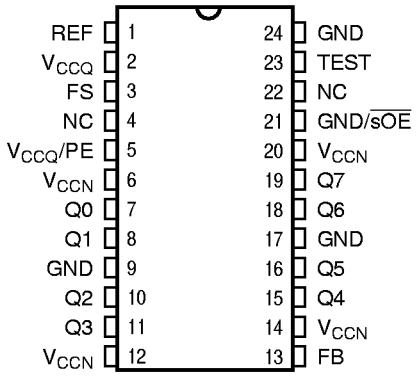


Table 1. Pin Definitions

Pin Name	Type	Definition
REF	IN	Reference clock input
FB	IN	Feedback input
TEST(1)	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Set LOW for normal operation.
GND/$\overline{sOE}$(1)	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except Q2 and Q3) in a LOW state - Q2 or Q3 may be used as the feedback signal to maintain phase lock. Set GND/$\overline{sOE}$ LOW for normal operation.
V_{CCQ}/PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
FS(2)	IN	Frequency range select. 3 level input. FS = GND: 15 to 35MHz. FS = Mid (or open) 25 to 60MHz. FS = V_{DD}: 40 to 100MHz
Q0 to Q7	OUT	8 clock output.
V_{CCN}	PWR	Power supply for output buffers.
V_{CCQ}	PWR	Power supply for phase locked loop and other internal circuitry.
GND	PWR	Ground

Note:
1. When TEST=MID and GND/$\overline{sOE}$ = HIGH, PLL remains active.
2. This input is wired to V_{CC}, GND or unconnected. Default is MID level. If it is switched in the real time mode, the outputs may glitch, and the PLL may require an additional lock time before all data sheet limits are achieved.

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Input Voltage V_I	–0.5V to 7.0V
Maximum Power Dissipation at T_A = 85°C, SOIC	530mW
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Recommended Operating Range

Symbol	Description	QS599x0-5,-7 (Industrial) Min	QS599x0-5,-7 (Industrial) Max	QS599x0-2 (Commercial) Min	QS599x0-2 (Commercial) Max	Units
V_{CC}	Power Supply Voltage	4.5	5.5	4.75	5.25	V
T_A	Ambient Operating Temperature	–40	85	0	70	°C

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

	SOIC Typ	SOIC Max	Units
C_{IN}	5	7	pF

Note: Capacitance applies to all inputs except TEST and FS. It is characterized but not tested.

Table 5. DC Characteristics Over Operating Range

Symbol	Parameter	Test Condition		9910 Min	9910 Max	9920 Min	9920 Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB inputs only)		2.0	—	V_{CC}–1.35	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB inputs only)		—	0.8	—	1.35	V
V_{IHH}	Input HIGH Voltage(1)	3-level inputs only		V_{CC} –1.0	— —	V_{CC} –1.0	— —	V
V_{IMM}	Input MID Voltage(1)	3-level inputs only		V_{CC}/2-0.5	V_{CC}/2+0.5	V_{CC}/2-0.5	V_{CC}/2+0.5	V
V_{ILL}	Input LOW Voltage(1)	3-level inputs only		—	1.0	—	1.0	V
$\|I_{IN}\|$	Input Leakage Current (REF, FB inputs only)	V_{IN} = V_{CC} or GND V_{CC} = Max.		—	5	—	5	µA
$\|I_3\|$	3-level Input DC Current (TEST, FS)	V_{IN} = V_{CC}	HIGH level	—	200	—	200	µA
		V_{IN} = V_{CC}/2	MID level	—	50	—	50	
		V_{IN} = GND	LOW level	—	200	—	200	
$\|I_{PU}\|$	Input Pull-up Current (V_{CCQ}/PE)	V_{CC} = Max., V_{IN} = GND		—	100	—	100	µA
$\|I_{PD}\|$	Input Pull-down Current (GND/$\overline{sOE}$)	V_{CC} = Max., V_{IN} = V_{CC}		—	100	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –16mA		2.4	—	—	—	V
		V_{CC} = Min., I_{OH} = –40mA		—	—	V_{CC}–0.75	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46mA		—	0.45	—	0.45	V
I_{OS}	Output Short Circuit Current(2)	V_{CC} = Max., V_O = GND,		—	–250	—	N/A	mA

Notes:
1. These inputs are normally wired to V_{CC}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{CC}/2. If these inputs are switched, the function and timing of the outputs may glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
2. QS59910 is to be measured at 25°C with 10:1 duty cycle, one output at a time, and one second maximum. QS59920 outputs are not to be shorted. Guaranteed by characterization but not production tested.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., TEST = Mid, REF = Low, GND/$\overline{sOE}$ = Low, All outputs unloaded	10	40	mA
ΔI_{CC}	Power Supply Current Per Input HIGH(1)	V_{CC} = Max., V_{IN}=3.4V	0.4	1.5	mA
I_{CCD}	Dynamic Power Supply Current Per Output(1)	V_{CC} = Max., C_L = 0pF	100	160	µA/ MHz
I_C	Total Power Supply Current(1)	V_{CC} = 5.0V, F_{REF} = 20MHz, C_L = 240pF(2)	43		mA
I_C	Total Power Supply Current(1)	V_{CC} = 5.0V, F_{REF} = 33MHz, C_L = 240pF(2)	63		mA
I_C	Total Power Supply Current(1)	V_{CC} = 5.0V, F_{REF} = 66MHz, C_L = 240pF(2)	117		mA

Notes:
1. Guaranteed by design and characterization but not production tested.
2. For 8 outputs each loaded with 30pF.

Table 7. Input Timing Requirements

Symbol	Description(1)	Min	Max	Units
t_R, t_F	Maximum input rise and fall times, 0.8V to 2.0V	—	10	ns/V
t_{PWC}	Input clock pulse, high or low	3	—	ns
D_H	Input duty cycle	10	90	%

Note:
1. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

Table 8. Switching Characteristics Over Operating Range

Symbol	Description		9910-2 Min	9910-2 Typ	9910-2 Max	9920-2 Min	9920-2 Typ	9920-2 Max	Unit
F_{REF}	REF frequency range	FS = LOW	15		35	15		35	MHz
		FS = MID	25		60	25		60	
		FS = HIGH	40		100	40		110	
t_{RPWH}	REF pulse width HIGH(1,7)		3.0	—	—	3.0	—	—	ns
t_{RPWL}	REF pulse width LOW(1,7)		3.0	—	—	3.0	—	—	ns
t_{SKEW}	Zero output skew (all outputs)(1,3)		—	0.1	0.25	—	0.1	0.25	ns
t_{DEV}	Device-to-device skew(1,2,4)		—	—	0.75	—	—	0.75	ns
t_{PD}	REF input to FB propagation delay(1,6)		–0.25	0	0.25	–0.25	0	0.25	ns
t_{ODCV}	Output duty cycle variation(1)		–1.2	0	1.2	–1.2	0	1.2	ns
t_{ORISE}	Output rise time(1)		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{OFALL}	Output fall time(1)		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{LOCK}	PLL lock time(5)		—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-cycle output jitter(1)	RMS	—	—	25	—	—	25	ps
		Peak-to-peak	—	—	200	—	—	200	

Notes:
1. All timing tolerances apply for $F_{NOM} \geq 25$MHz. Guaranteed by design and characterization, not subject to production testing.
2. Skew is the time between the earliest and the latest output transition among all outputs with the specified load.
3. t_{SKEW} is the skew between all outputs. See AC test loads at Figure 2.
4. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)
5. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
6. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
7. Refer to Table 7 for more detail.

Table 8. Switching Characteristics Over Operating Range (Cont'd)

Symbol	Description		9910-5 Min	9910-5 Typ	9910-5 Max	9920-5 Min	9920-5 Typ	9920-5 Max	Unit
F_{REF}	REF frequency range	FS = LOW	15		35	15		35	MHz
		FS = MID	25		60	25		60	
		FS = HIGH	40		100	40		100	
t_{RPWH}	REF pulse width HIGH(1,7)		3.0	—	—	3.0	—	—	ns
t_{RPWL}	REF pulse width LOW(1,7)		3.0	—	—	3.0	—	—	ns
t_{SKEW0}	Zero output skew (all outputs)(1,3)		—	0.25	0.5	—	0.25	0.5	ns
t_{DEV}	Device-to-device skew(1,2,4)		—	—	1.25	—	—	1.25	ns
t_{PD}	REF input to FB propagation delay(1,6)		–0.5	0	0.5	–0.5	0	0.5	ns
t_{ODCV}	Output duty cycle variation from 50%(1)		–1.2	0	1.2	–1.2	0	1.2	ns
t_{ORISE}	Output rise time(1)		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{OFALL}	Output fall time(1)		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{LOCK}	PLL lock time(5)		—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-cycle output jitter(1)	RMS	—	—	25	—	—	25	ps
		Peak-to-peak	—	—	200	—	—	200	

Symbol	Description		9910-7 Min	9910-7 Typ	9910-7 Max	9920-7 Min	9920-7 Typ	9920-7 Max	Unit
F_{REF}	REF frequency range	FS = LOW	15		35	15		35	MHz
		FS = MID	25		60	25		60	
		FS = HIGH	40		100	40		100	
t_{RPWH}	REF pulse width HIGH(1,7)		3.0	—	—	3.0	—	—	ns
t_{RPWL}	REF pulse width LOW(1,7)		3.0	—	—	3.0	—	—	ns
t_{SKEW0}	Zero output skew (all outputs)(1,3)		—	0.3	0.75	—	0.3	0.75	ns
t_{DEV}	Device-to-device skew(1,2,4)		—	—	1.65	—	—	1.65	ns
t_{PD}	REF input to FB propagation delay(1,6)		–0.7	0	0.7	–0.7	0	0.7	ns
t_{ODCV}	Output duty cycle variation from 50%(1)		–1.2	0	1.2	–1.5	0	1.5	ns
t_{ORISE}	Output rise time(1)		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output fall time(1)		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL lock time(5)		—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-cycle output jitter(1)	RMS	—	—	25	—	—	25	ps
		Peak-to-peak	—	—	200	—	—	200	

Notes:
1. All timing tolerances apply for $F_{NOM} \geq 25MHz$. Guaranteed by design and characterization, not subject to production testing.
2. Skew is the time between the earliest and the latest output transition among all outputs with the specified load.
3. t_{SKEW} is the skew between all outputs. See AC test loads at Figure 2.
4. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)
5. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
6. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
7. Refer to Table 7 for more detail.

Figure 3. AC Test Loads and Waveforms

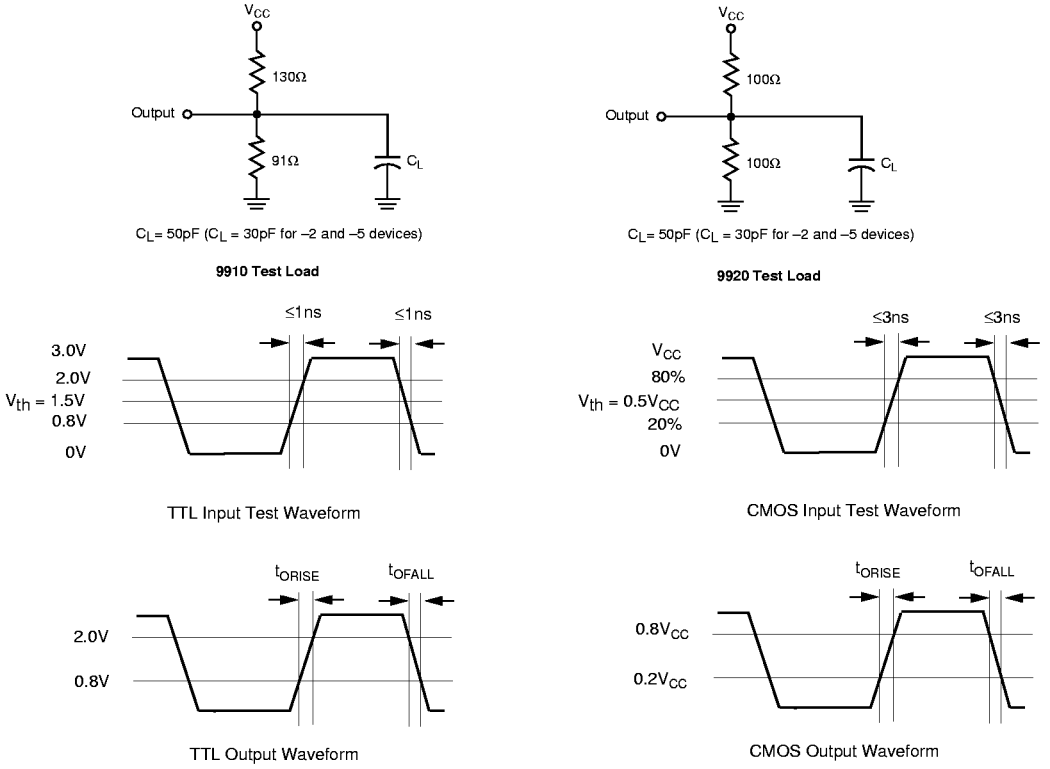
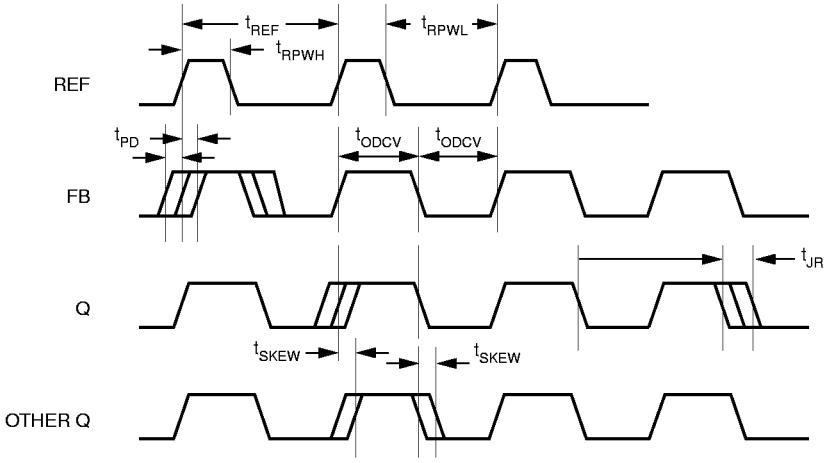


Figure 4. AC Timing Diagram



Notes:

Skew: The time between the earliest and the latest output transition among all outputs when all are loaded with 50pF (30pF for -2 and -5) and terminated with 50Ω to 2.06V (9910) or $V_{CC}/2$ (9920).

t_{SKEW}: The skew between all outputs.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle.

t_{ORISE} and t_{OFALL} are measured between 0.8V and 2.0V for 9910 and $0.2V_{CC}$ and $0.8V_{CC}$ for 9920.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Ordering Information